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A 0.13-μm 6 to 8-bit PBTN DEM Current Steering DAC

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Abstract:*This paper reports the design and simulation of an optimized 6-bit 1-MSB and 2-MSB Partial Binary Tree Network (PBTN) Dynamic Element Matching (DEM) current steering Digital-to-Analog (DAC). Then, the work of the 6-bit design is extended to implement an 8-bit DAC both for 1-MSB and 2-MSB respectively. From the simulation, results show that for 6-bit 1-MSB DAC, Differential Non-Linearity(DNL) of 0.00001895 LSB,Integral Non-Linearity(INL) of 0.0001457 LSB and power consumption of 2.806 mW (excluding load) are obtained. Meanwhile, for 6-bit 2-MSB DAC, DNL of -0.00928 LSB, INL of 0.008669 LSB and power consumption of 2.8mW (excluding load) are achieved. For 8-bit 1-MSB DAC, DNL of -0.00028287 LSB, INL of 0.000252 LSB and power consumption of 11.29mW (excluding load) are obtained while for 8-bit 2-MSB DAC, DNL of 0.001324 LSB, INL of 0.0007896 LSB and power consumption of 11.27 mW (excluding load) are acquired.The design and simulation of this work are based on 0.13-μm CMOS process technology.*

Keywords:*Partial Binary Tree Network, Dynamic Element Matching, current steering DAC, INL, DNL.*

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I. Introduction

Digital signals have an advantage over analog signals largely because digital signals are more immune to noise and imperfections, problems which greatly hinders the precision of analog signals.

A popular method to minimize component mismatch error is Dynamic Element Matching (DEM) [1]. This technique is a randomization technique to select one of the appropriate codes for each of the digital input value before entering the DAC block. Using this technique, the time averages of the equivalent components at each of the component positions are equal or nearly equal to reduce the effects of component mismatches in electronic circuits. This design technique can reduce the effects of component mismatches in electronic circuits. It also dynamically rearranges the interconnections between components so that the effects of component mismatches can be minimized. Since the virtual positions of the components are randomized, harmonic distortions caused by mismatched components can be converted into white noise [1].

However, the drawback of existing designs is that the design would suffer from excessive hardware complexity. A complicated encoding is usually necessary for conventional DEM encoders which will lead to a lot of switch transitions at the same time and it will cause glitches to the output signal [2].

Partial Binary Tree Network (PBTN) is a new DEM algorithm which possesses relatively lower hardware complexity [2]. The design of such a technique requires much fewer transmission gates compared to Binary Tree Network (BTN), hence it will have lower hardware complexity and reduced glitches.

Previous researches had designed and validated up until 6-bit 1-MSB PBTN DEM DAC and 2-MSB PBTN DEM DAC [3]. Both 1-MSB and 2-MSB achieved DNL error lower than 0.3632 LSB and INL error lower than 0.074 LSB. This leaves PBTN of higher bits to be designed and validated.

II. Backgrounds

A. Current Steering DAC

Shown in Fig. 1, this DAC architecture is made up of multiple current sources, each source connected to a switch controlled by the digital code inputs. The output is obtained by summing the current from all then-current sources [4].

Advantages:

- High performance in terms of INL and DNL.
- Suitable for generating high-frequency signals.

Disadvantage:

- High hardware complexity in higher resolutions.

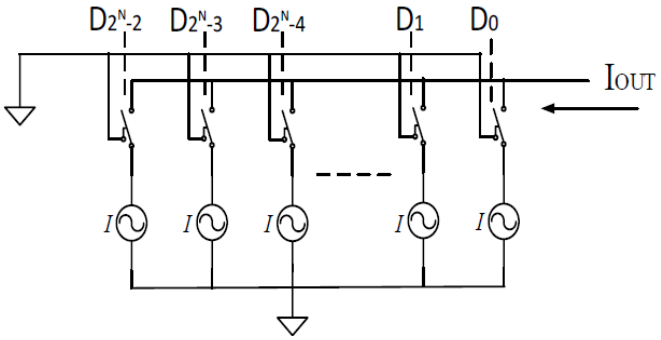


Figure1. Current Steering DAC [4]

Shown in Fig. 2, DEM DACs have enabled key performance enhancements over the years in oversampling data converters, pipelined ADCs, and high-resolution DACs. They effectively eliminate component mismatches as a performance-limiting source of error [5]. For the DACs without DEM, mismatches amongst duplicate circuit typically and unsurprisingly introduced during circuit fabrication produces unwanted distortion. Thus, if the scrambling pattern of the elements is used, DEM produces fewer errors resulting from mismatches[5].

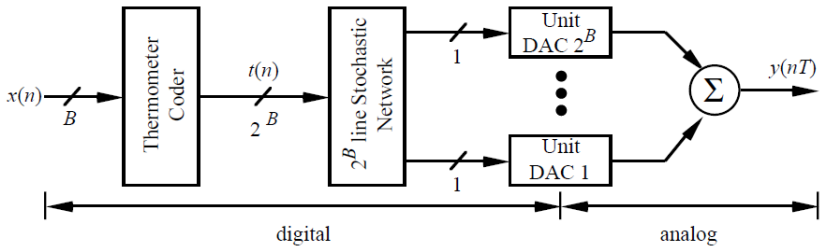
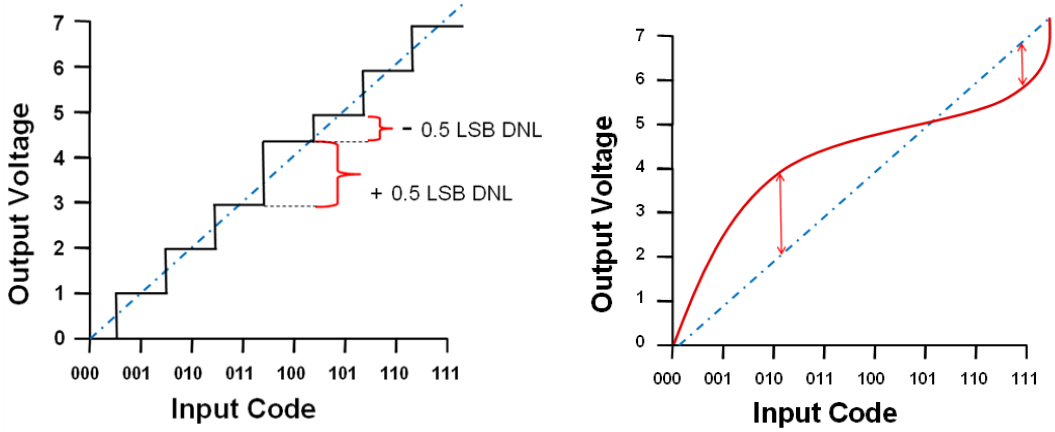


Figure 2. General topology of a B-bit stochastic DEM DAC [5].

B. DNL (Differential Non-Linearity) and INL (Integral Non-Linearity)

Shown in Figure 3(a), DNL measures the difference in step height of each step, concerning the ideal step size. Shown in Figure 3(b), INL measures the deviation of each step from the ideal straight line. Both DNL and INL can be expressed in positive or negative values respectively. Positive values show that the actual step is higher than the ideal value, whereas negative value shows otherwise [6].



(a) (b)

Figure 3.(a) Differential nonlinearity (DNL), (b) Integral nonlinearity (INL) [6]

III. Methodology

The goal of this research is to further improve on the performance of the 6-bit PBTN DEM DAC based on the work done in [2] and to increase the resolution from 6-bit to 8-bit using the same topology. Research on relevant and related topics is required before the designing phase of this research and is achieved by studying previous works. Previous DAC topologies and specifications were researched to determine the best configuration and design to proceed with. The following discusses the step by step of the design and implementation of the PBTN DEM DAC.

A. Partial Binary Tree Network (PBTN)

Fig. 4 shows a general k+1 bit 1-MSB PBTN. When the control signal, C_k is LOW, 2^k copies of MSB X_k will be sent to upper outputs. Input bit X_{k-1} would produce 2^{k-1} copies to lower outputs. This process was repeated until input bit X0 which only produces 1 copy to lower output. Vice versa, when the control signal is HIGH, these outputs will be exchanged; 2_k copies of X_k will be sent to lower outputs and input X_{k-1} until X0 will be sent to upper output [3].

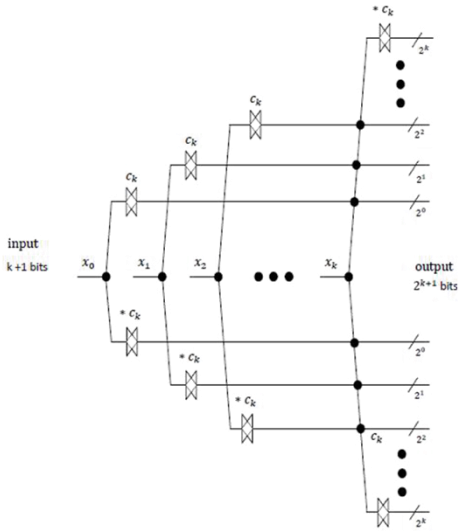


Figure 4. k+1 bit 1-MSB PBTN [3]

A general k+1 bit 2-MSB PBTN is shown in Fig. 5. For every new input bit, 6 transmission gates were added to the combination of the two k-bit 2-MSB PBTN networks or blocks, and their outputs were connected to the outputs of the k-bit 2-MSB PBTN network [3].

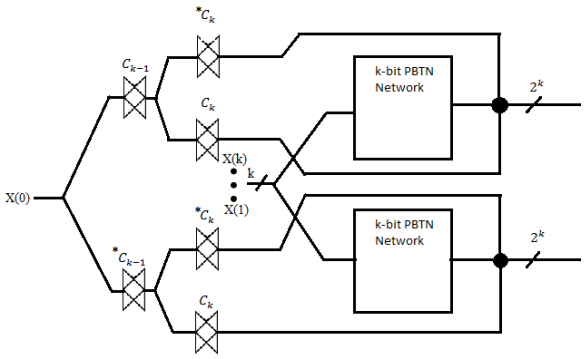


Figure5. k+1 bit 2-MSB PBTN [3]

B. Transmission Gate

The design of the transmission gate is shown in Fig. 6. Transmission gates are the building blocks for the PBTN network. The function of the transmission gate is to control the flow of information from input to output. This is achieved by subjecting the 'Sel' input to different logic levels. Wheninput signal 'Sel' is HIGH, the input state is passed to the output. Conversely, when 'Sel' is LOW, the output of the transmission gate is in high impedance.

The design of the transmission gate was adapted and improved from previous researches [2] [3]. It was found that the configuration from previous researches was unable to completely shut off I_{DS} flowing from input to output even when the transmission gate was supposed to be in high impedance state. Hence, two additional gates were added into the design to ensure the desired output is obtained. Additionally, the W/L ratios of all the transistors were tweaked, simulated, and tested vigorously to optimize its performance in terms of glitch tolerance.

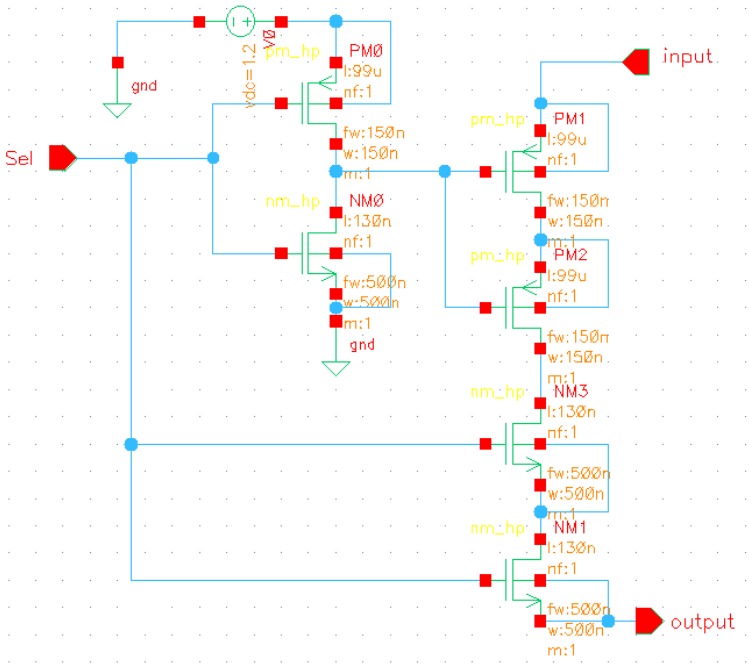


Figure 6. An optimized schematic design of transmission gate

C. Design of 8-bit 1-MSB PBTN

To build a 6-bit 1-MSB PBTN, lower stages are to be constructed in a hierarchical method, starting with 3-bit 1-MSB PBTN, which is proceeded by 4-bit, 5-bit, and then 6-bit and end up at 8-bit. The design of 3-bit 1-MSB PBTN is illustrated in Fig. 7. As shown in the figure, the total number of transmission gates used is derived from the equation of $2^{B+1} - 2$ [3]. Thus, for the 3-bit design of 1-MSB, it requires only 14 transmission gates as opposed to the conventional binary tree network design that needs 32 transmission gates [2].

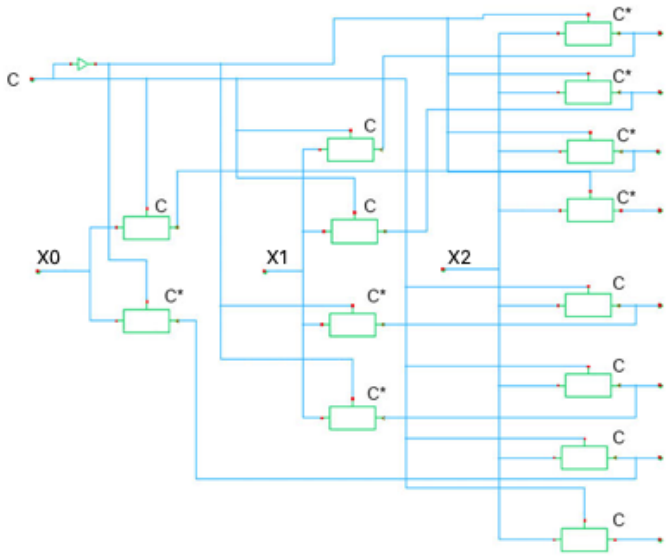


Figure 7.3-bit 1-MSB PBTN design

In Fig. 8, 4-bit 1-MSB PBTN is constructed using two 3-bit 1-MSB PBTN and two additional transmission gates. Inputs X1, X2, and X3 are connected to both 3-bit 1-MSB PBTNs. Input X0 is connected to the two extra transmission gates. The outputs are then connected to the t3 and t7 of the output pins.

For every iteration of 1-MSB PBTN going up the hierarchy, the output from the C* transmission gate is connected to the last output pin of the upper PBTN; whereas, the output from the C transmission gate is connected to the fifth output pin from the bottom.

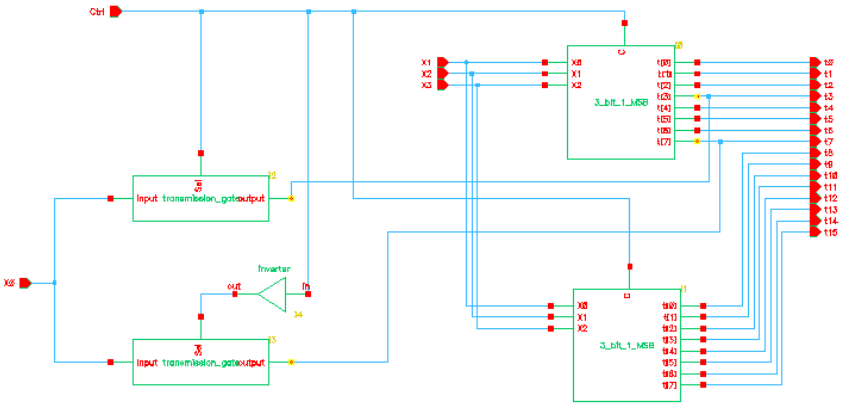


Figure 8.4-bit 1-MSB PBTN

D. Design of 8-bit 2-MSB PBTN

The method of constructing 8-bit 2-MSB PBTN is similar to the previously mentioned 8-bit 1-MSBPBTN.However, 2-bit 2-MSB PBTN is constructed first instead of 3-bits. The design of 2-bit 2-MSB PBTN is shown in Fig. 9 [6].

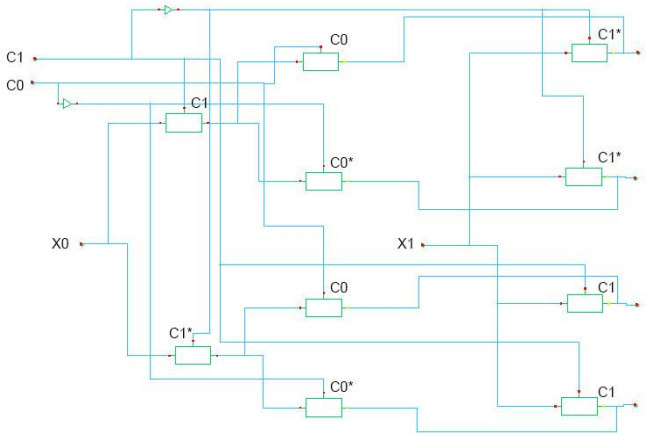


Figure 9. 2-bit 2-MSB PBTN design

In Fig. 10, the 3-bit 2-MSB PBTN is constructed using two 2-bit 2-MSB PBTNs, and six additional transmission gates. The inputs X1 and X2 are connected to both 2-bit 2-MSB PBTNs. Input X0 is connected to the network of transmission gates first. The outputs are connected to the output pins t0 to t3.

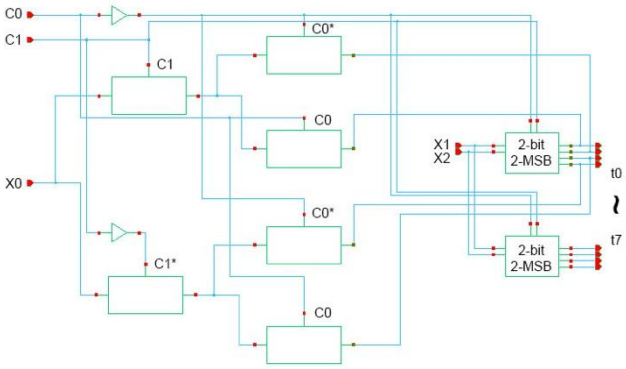


Figure 10.3-bit 2-MSB PBTN

The method of how the transmission gate outputs are connected to the output terminals is illustrated in Fig. 11. The pattern alternates between even and odd bits of 2-MSB PBTNs.

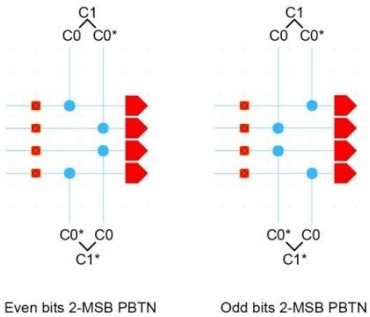


Figure 11.2-MSB k+1 bit transmission gate to output connections

E. Current Steering DAC

Current steering DAC is implemented in this research largely because current steering DACs are capable of providing a very high sampling rate.2^N current sources are required to construct an n-bit current steering DAC. The input digital code is fed into the PBTN where it will be scrambled before passing the values to the DAC [3]. The current steering DAC is made up of individual switchable current sources that consist of four components oftwo NMOS, and two PMOS transistors, which works as a cascade current mirror, a self-bias circuit and a switch. Fig. 12 illustrates the component interconnections of the current cell.

However, the current that is produced immediately from the current mirror is not sufficient; hence, the output must be magnified using a current-controlled current source (CCCS). To produce an 8-bit PBTN DEM DAC, 256 switchable current sources are required. Meanwhile, to produce the maxed-out output, with the digital input of '11111111', 255 units of switchable current sources have to be turned ON, while the remaining 1 block will serve as a dummy and will remain OFF. The 8-bit DAC design is shown in Fig. 13. For this research, the output voltage is designed to be 1 V, while each switchable current source will contribute 20 μA of current. Hence, a resistor with a resistance of 10Ω is connected to the output. In addition, the use of a load with high impedance causes theundesirable effects of increasing the output's DNL and INL, thus an amplifier (CCCS) is used to provide amplification to the output current and is set to provide a gain of 20. Calculations are shown in Eq. (1) below:

$$V_{out} = (2^8 - 1) \times IR = 255 \times 20\,\mu A \times 10\Omega \times 20 = 1.02V \qquad (1)$$

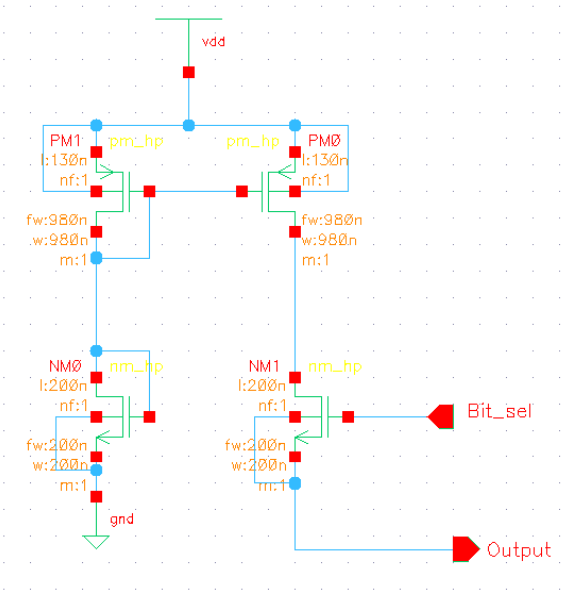


Figure 12. Simple switchable current source

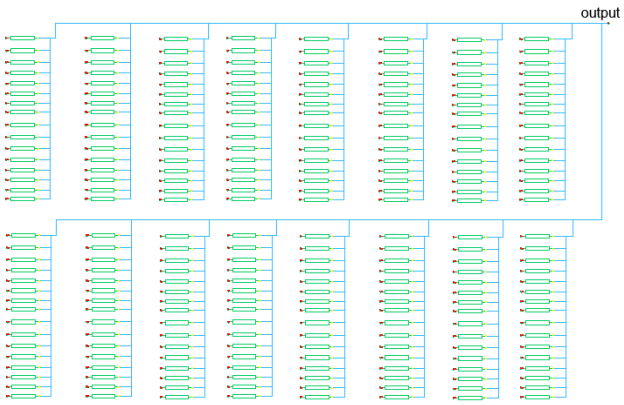


Figure 13.8-bit current steering DAC using 256 current sources

IV. Results and Discussion

Fig. 14 shows the test bench circuit setup or testing of an 8-bit 1-MSB PBTN and 8-bit 2-MSB PBTN respectively. Inputs X0 to X7 are varied from '00000000' to '11111111' at a rate of 2000 Hz. The CCCS gain is set to 20, while load impedance is set to 10Ω. Control signals are varied across time as well.

Simulations for 6-bit 1-MSB PBTN and 6-bit 2-MSB PBTN also use a similar setup. However, the inputs X0 to X5 are varied from '000000' to '111111', and CCCS gain is set to 80 instead.

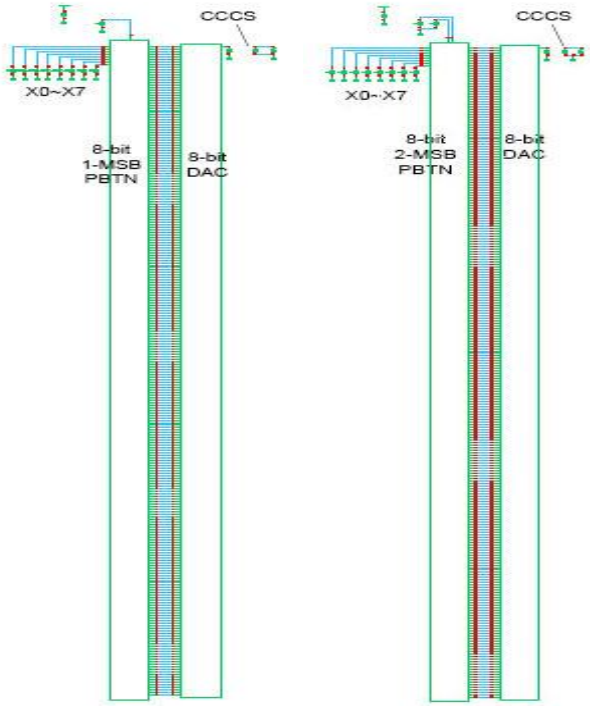


Figure 14. Test bench circuit setup

A. Simulation

The simulation result of 6-bit 1-MSB for the work in [2] is shown in Fig. 15 (as reference) followed by the 6-bit 1-MSB result of this work, shown in Fig. 16. Then, only the result for 8-bit 1-MSB PBTN is shown in Fig. 17. Simulation data from 6-bit 1-MSB PBTN and 6-bit 2-MSB PBTN (from current and previous work), 8-bit 1-MSB PBTN and 8-bit 2-MSB PBTN are compared in Table I.

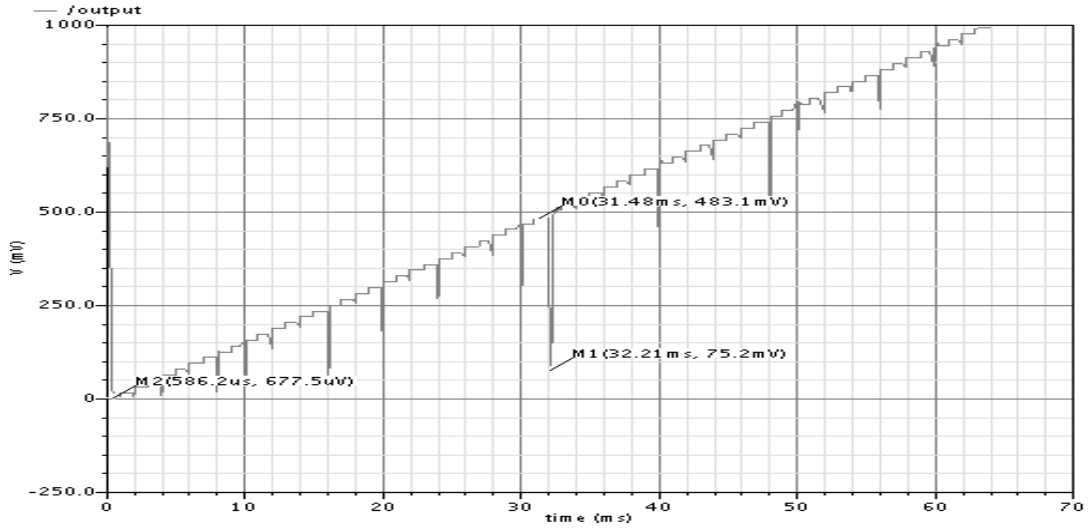


Figure 15. 6-bit 1-MSB PBTN output waveform from work in [2].

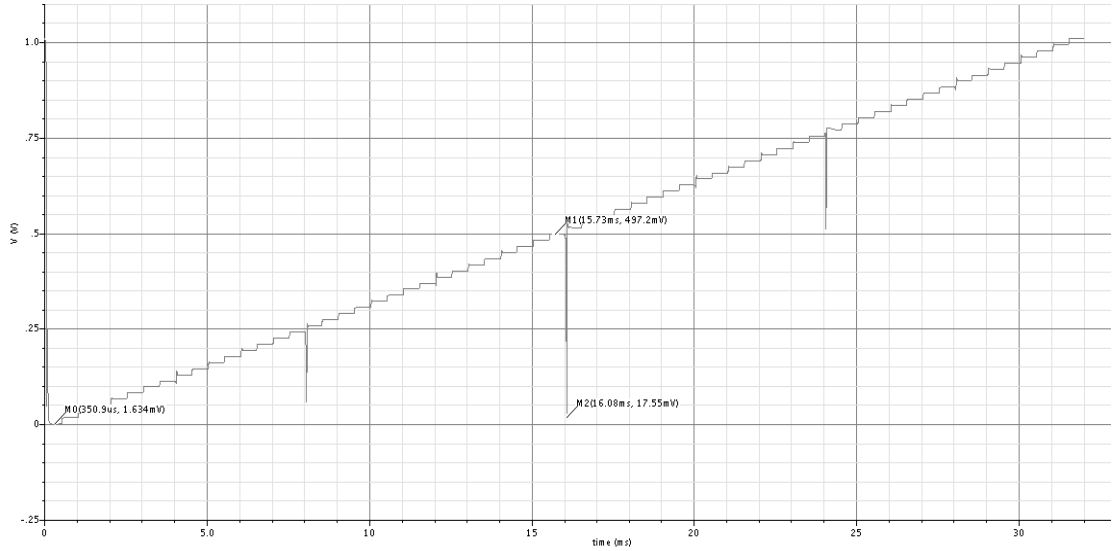


Figure 16. 6-bit 1-MSB PBTN output waveform of this work.

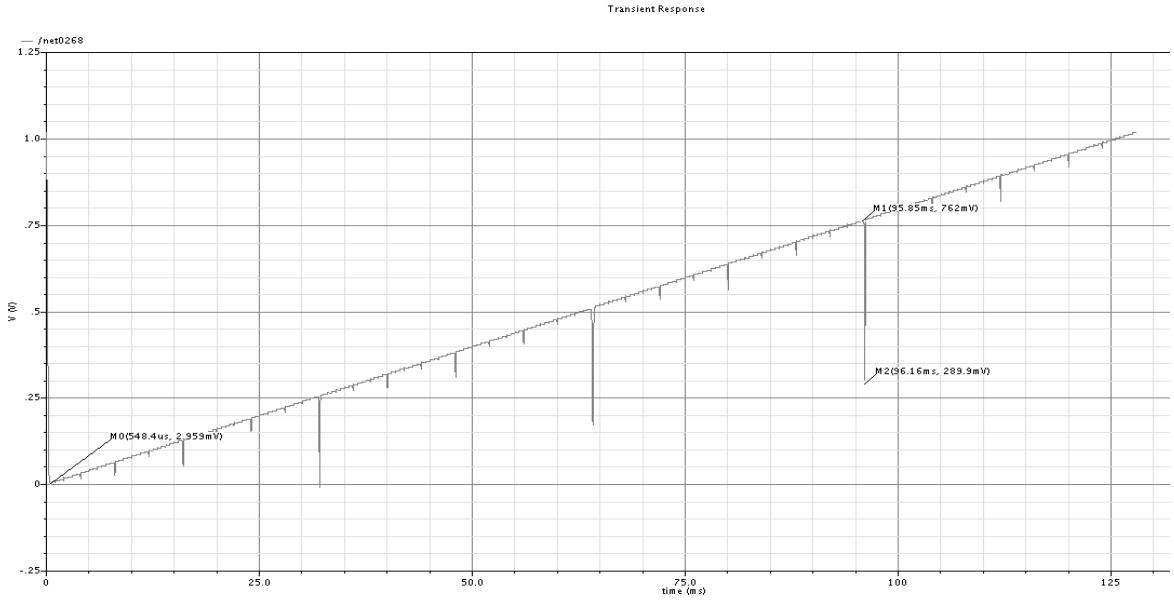


Figure 17.8-bit 1-MSB PBTN output waveform.

Table I. Simulation results comparison

Specifications	[2]	[3]	This research			
	6-bit 1-MSB	6-bit 2-MSB	6-bit 1-MSB	6-bit 2-MSB	8-bit 1-MSB	8-bit 2-MSB
DNL (LSB)	0.3184	0.3632	0.00001895	-0.00928	-0.00028287	0.001324
INL (LSB)	0.0062	0.0074	0.0001457	0.008669	0.000252	0.0007896
Power Consumption	14.13 mW (incl. load)	18.1 mW (incl. load)	2.806 mW (excl. load)	2.8 mW (excl. load)	11.29 mW (excl. load)	11.27 mW (excl. load)
Speed	1 kHz	1 kHz	2 kHz	2 kHz	2 kHz	2 kHz
Transmission gates count	126	250	126	250	510	1018

B. Discussion

From Fig. 15 and Fig. 16, it is noticeable that the glitches are reduced quite significantly as the frequency of glitches occurring has been reduced. Apart from the glitches, from the comparison drawn from Table I, it is apparent that the design used in this research achieved much lower DNL and INL overall, except

for 6-bit 2-MSB's INL being slightly higher than in the previous research at 0.008669 LSB. This research also successfully doubled the speed of the PBTN to 2000 Hz, up from 1000 Hz from previous researches.

The simulation results also showed that the 8-bit 1-MSB performs marginally better when compared to the 8-bit 2-MSB in terms of DNL and INL, but also has slightly higher dynamic power consumption. However, it should be noted that the 8-bit 1-MSB has much lower hardware complexity, which outweighs the slight advantage of the 8-bit 2-MSB. Hence, it can be concluded that the 8-bit 1-MSB is more preferred.

V. Conclusion

The goal of this research was to validate the concept of PBTN, which is a form of DEMapproach, performed by previous researches. The 6-bit PBTNs have been successfully replicated from previous researches [2] [3], and the performances have been successfully improved to provide a much lower DNL and INL. Another significant improvement made was the huge reduction in glitches, as the frequency of glitches occurring has been reduced. This was achievedby the changes made to the design of a single transmission gate.

This research also aimed to push the limits of PBTN into producing higher resolution outputs. The constructions and simulations of the 8-bit 1-MSB PBTN and 8-bit 2-MSB PBTN were successful and produced promising results. Both designs showed good performance specifications in terms of DNL, INL, and power consumption. However, due to the 8-bit 2-MSB consisting of higher hardware complexity, the 8-bit 1-MSB PBTN may be preferred despite the marginal differences in performance metrics. Plus, the speed of the PBTNs have been improved significantly as well. The speed has been successfully doubled to 2000 Hz compared to previous works.

Lastly, limitations were encountered when eliminating glitches from the DAC. Due to the relatively complex architecture of PBTN, the effects of propagation delay are very apparent. This makes it impossible to totally eliminate glitches. The operating speed is also limited by the occurrence of glitches. The effects of glitches were more significant when operating at higher speeds. Nevertheless, the design of transmission gates still possess potential to be further optimized to produce PBTN with better glitch tolerance and higher operating speeds.

Acknowledgements

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