A Survey and an Approach for Content-Addressable Memory Design Based Fast Image-Feature Learning System

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Abstract: *The speed of Content-Addressable Memories (CAMs), here the content is an image data or image feature, is a kind of struggle to logical processors data. The processor architecture must also have increasing capabilities to cope with the fast computational algorithms, data storage and sensing, content detection and diagnosis and improved search based memory designs. The focus of this work is fast computations and search based designs for CAMs. Proposed EB-CAM will be analyzed using IC design tools in 90nm technology, using Verilog hardware description language and usage of Cadence for layout generation and parasitic extraction of the circuit components.*

Keywords- *Image analysis, Feature Learning, Content-Addressable Memory, Processor Hardware, High Speed, Low Power, Pattern Search, Parallel Registers*

I. Introduction

Content-addressable memory (CAM) and associative memory (AM) are types of storage structures that allow searching by content as opposed to searching by address. Such memory structures are used in diverse applications ranging from branch prediction in a processor to complex pattern recognition.

The main contribution of this work is divided in two parts:

(i) reduction in match line (ML) sensing energy, and

(ii) static-power reduction techniques.

The ML sensing energy is reduced by employing

(i) positive-feedback ML sense amplifiers (MLSAs),

(ii) low-capacitance comparison logic, and

(iii) low-power ML-segmentation techniques.

The proposed method can be implemented on hardware based solutions to improve the software-based algorithms. Proposed EB-CAM performs fast content searching than commercially available CAMs by using a unique SearchRegisterLogic() Circuit to achieve high speed content searching, utilizing less CAM clock cycles, these makes the proposed VLSI architecture and implementation technique to improve the content diagnosis process.

II. Objectives Of The Proposed Work

Eight Bit-CAM design with a search register scanning algorithm is presented to improve the performance of CAM for low power VLSI architectures.

EB-CAM design salient features are:

Feature 1   VLSI architecture and implementation technique to improve the content diagnosis process by minimizing *path_delay()* and *lookup_delay()*.

Feature 2   A unique *SearchRegisterLogic()* Circuit to achieve high speed content searching, utilizing less CAMclk() cycles.

Feature 3   Design of EB-CAM performs fast content searching than commercially available CAMs.

Feature 4   The chip level floor plan of proposed EB-CAM utilized less area in a pipelined fashion.

III. Proposed Methodology

A. Content Modeling :

When a content is received by EB-CAM, to perform a gated clock division routing algorithm at every routing, content patterns were determined at every path based on the content size and capacity. The following steps shows the proposed content prediction procedure,

Define : C_{PR} Content predicting

Allocate prefix or postfix 0's in the presence of any over or under bits of the Content Pattern result and move this content into 8 - bit search register,

For Path A and C perform high payload processing, utilizing the maximum high levels of EB-CAM registers performance,

For Path A and B perform high parallel processing, utilizing the maximum high density of EB-CAM throughput, and

For Path A, B and C perform high word content predicting in the manageable clock levels.

Output : Content Pattern predictions

These Content Pattern predictions were proceeded to parallel matching search register logic to perform pattern-of-random architecture , using P_{or} matching frames through S_{RL} diagnose method and Pattern Detection.

B. Parallel Matching Search Register Logic :

The following steps shows the EB-CAM pattern-of-random architecture procedure

Define : P_{or} pattern-of-random and P_d Pattern Detection

Analysis 01 : P_{or}

Perform content matching based on the Filter Actions set by P_{or}.

Action : Negotiation with Presence : In this approach, use of priority encoder is designed to detect the content arbitrary matching with the EB-CAM. This approach results in the reduction of worst case delays, in contrast reducing the power utilizations.

Action : Negotiation with Absence : In this approach, the content entries are non-pipelined to detect the longest matching entries with the EB-CAM. This approach results in lowering the computation delays, in contrast reducing the execution time of the algorithm

Action : Presence : In this approach, the content focus on frequency of matching table entry to list the corresponding number of repeated bit or watch matching is considered with the EB-CAM. This approach results in the efficient content scanning, resulting in sophisticated EB-CAM content matching.

Output : Content Loading and Content Word Retrieval

The performance of R_{sr} is stated by Parallel Matching Search Register Logic. In this logic, the operations performed are *RegisterRead0(), RegisterRead1(), RegisterWrite0(), RegisterWrite1(), RegisterMatch0()* and *RegisterMatch1()*, which are tabulated in table 1,

Table 1 : Parallel Matching Search Register Logic procedure

Operation	RL	WL	ML	$\overline{ML}$	R_{sr}	S_{RL}
RegisterRead0()	0	1	0	1	$0 \rightarrow 1$	$\overline{S_{RL}(1)}$
RegisterRead1()	1	0	1	0	$1 \rightarrow 0$	$S_{RL}(0)$
RegisterWrite0()	0	0	0	1	$w0$	$s0$
RegisterWrite1()	0	1	1	0	$0 \rightarrow 1$	$\overline{S_{RL}(1)}$
RegisterMatch0()	1	0	0	1	$1 \rightarrow 0$	$S_{RL}(0)$
RegisterMatch1()	1	1	1	0	$w1$	$s1$

C. Operation of Single Bit EB-CAM architecture

For single cycle operation, as shown in figure 1, the process is

Process 1 During the *Match_Operation()*, search of EB-CAM for a match to an input *Search_Content()* is performed. The output is *MTrue()* signal associated with associated *Match_Valid()* with an encoded bus of one match EB-CAM cell.
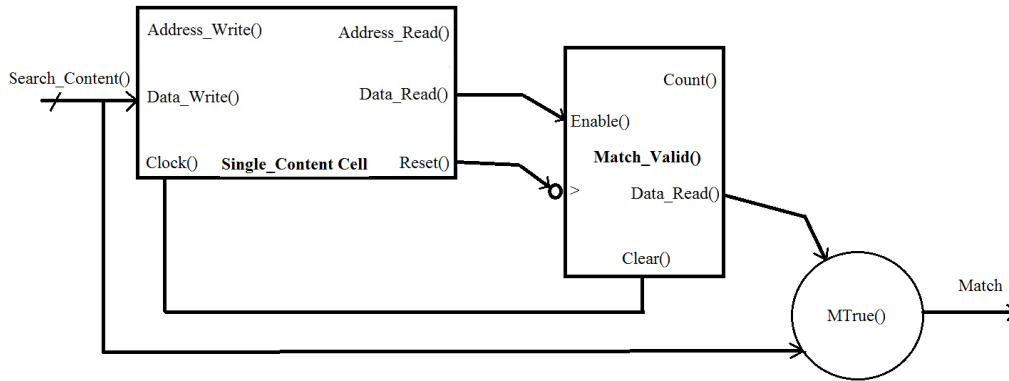
Process 2 During the *NonMatch_Operation()*,search of EB-CAM for a match to an input *Search_Content()* is performed. The output is *MFalse()* signal associated with associated *Match_Valid()* with an encoded bus of one match EB-CAM cell.

Figure 1 : Single Bit EB-CAM Architecture

D. Operating modes of Single Bit EB-CAM cell Design

The proposed EB-CAM Cell for Single Bit Design is shown in figure 2. Single Bit Cell consists of three NMOS transistors, one PMOS transistors and two stacked capacitors. Four of the transistors are denoted by mw0, mw1, ms0, ms1. The stacked capacitors are used to store the charges of ms0 and ms1 transistor charges. The PMOS transistor ms1 drain is connected to V_{dd} : supply voltage and third NMOS transistor ms0 drain is connected to ground. Bit lines represented by *Bit* and $\overline{Bit}$ are supplied with the single-bit *Search_Content()* are supplied with content for write and search operations. Word line (WL) access write access to each EB-CAM operation. The Match Line (ML) is accessed to read *Search_Content()*
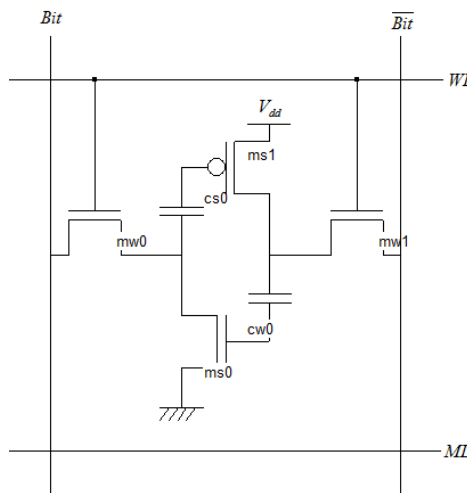

Figure 2 : Cell circuit diagram : Single Bit EB-CAM cell with stacked capacitor structure.

The modes of proposed EB-CAM Cell for *Search_Content()* are shown in figure 3. During *MTrue()* operation, WL is activated for write operation, the date is written into ms0 and ms1 through mw0 and mw1.
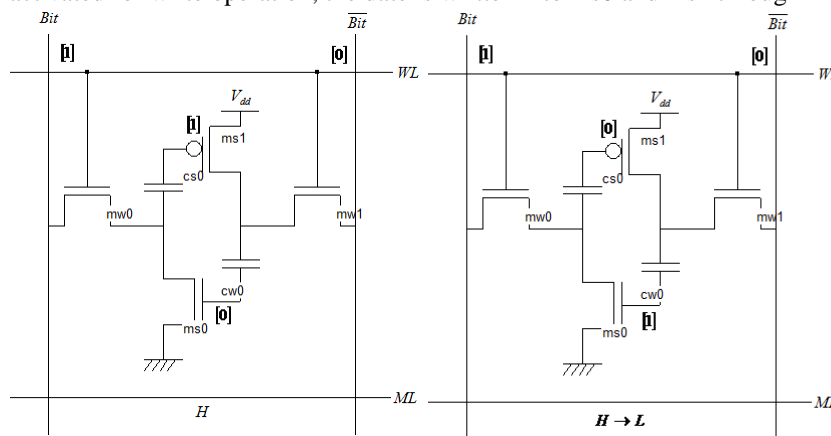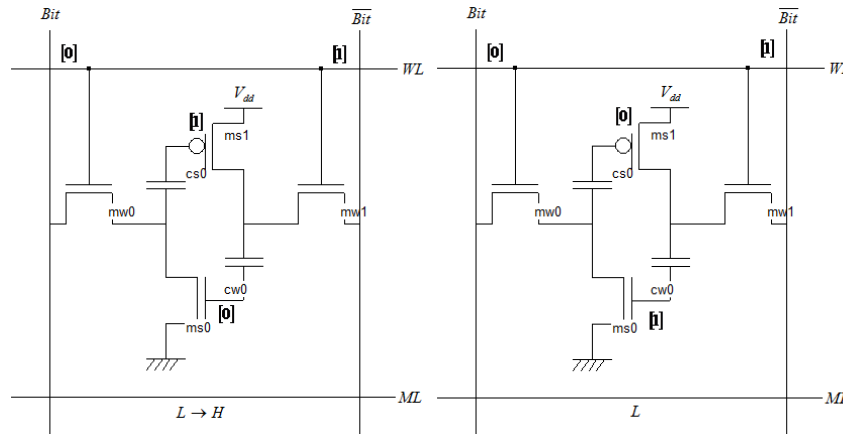

Figure 3 (a)

Figure 3 (b)

Figure 3 (c)   **Figure 3 (d)**

Figure 3 *Search_Content()* Single EB-CAM operations a) *MTrue()* operation, b) *Invalid multipleMatch_Operation()*, c)*Valid multipleMatch_Operation()* and d) *MFalse()* operation

The modes of content search operation is as follows:

Mode 1 As shown in figure 3 a), if Bit, $\overline{Bit}$ and ML are charged to H with their respective proportional power supply and content, a *MTrue()* operation will made validated.

Mode 2 As shown in figure 3 b), if   Bit and $\overline{Bit}$ are charged with H and L, and ML is in varying intermediate level of discharging status, a Invalid *multipleMatch_Operation()* operation will made validated.

Mode 3 As shown in figure 3 c), if Bit and $\overline{Bit}$ are charged with L and H, and ML is in fixed level of discharging status, a Valid *multipleMatch_Operation()* operation will made validated.

Mode 4 As shown in figure 3 d), if Bit and $\overline{Bit}$ are charged to L with their respective proportional power supply and content, and ML is at complete discharging status, a *MFalse()* operation will made validated.

The discharging of Bit and $\overline{Bit}$ will drive the ML to a H position, during this state of operation, if any *Search_Content()* is enabled, the Bit will get H level through ms0 and cw0 from ML line. Similarly if the Bit gets L level through ms0 and cw0, $\overline{Bit}$ will get charged to H and Bit will get charged to L, the content in memory will result in to out of bit lines.

IV.   Results And Discussions

      EB-CAM is designed and simulated using IC design tools in 90nm technology. After designing EB-CAM at the architectural level, behavioural and functional verifications will be done using the Verilog hardware description language, with layout generation and parasitic extraction of the circuit components of all proposed EB-CAM using Cadence.

Table 2 : EB-CAM (2048-bit) Performance Statistics

	Design		Implementation	Performance	
	Combinational Modules	Sequential Modules	Device (%)	Max. Frequency (MHz)	Min. Cycle (ns)
512x8 Distributed RAM	2642	2202	61	181	21.5(Write) 35.2(Read)
1024x8 Distributed RAM	5668	4608	102	228	27.8(Write) 925(Read)
2048x8 Distributed RAM	11436	9016	202	384	38.5(Write) 1,560(Read)

Table 3 : EB-CAM (2048-bit) Design Statistics

	Power Consumption (For 3.5 ns search time)								
	V_{bias}	V_{ML}	I_{ML}	Current Source Enabled Time	Voltage difference between ML_H and ML_L	I_{ML} drop-off	%Q (full match & miss match)	% Speed(full match & miss match)	% Energy/ Search
512x8 Distributed RAM	0-0.6V	0.05V	2μA	1.5ns	300 mV	2.5ns	62	48	60
1024x8	0-	0.45V	18.1	2.6 ns	412 mV	19.5 ns	84	71	81

Distributed RAM	0.6V		µA						
2048x8 Distributed RAM	0-0.6V	0.92 V	78.6 µA	3.2 ns	506 mV	80.2 ns	91	94	90

Table 2 and table 3, shows the suggested EB-CAM (2048-bit) Performance and Design Statistics. As shown in table 3, with the value of V_{bias}=0V - 0.6V, the current produced at ML increases rapidly, causing V_{ML} to rise in turn. Thus increasing the *Search_Content()* speed ie., fast speed and energy saving per search ie., low power. The value of V_{bias} is made adjustable through a sequential module EB-CAM cell to provide low power utilization and fast speed content searching.

V.   Conclusions

In this research work, the proposed EB-CAM design allocates a variable V_{bias} power to content search based on parallel match searching and finding the number of mismatched bits in each EB-CAM word cell. During content searching, Invalid multipleMatch_Operation() and MFalse() operation utilizes very less power of total 0.25 V_{bias}, results in a power reduction for faster clock speed performance. The suggested EB-CAM design can be implemented in a 64K word x 288-b EB- CAM for a 90nm 1.2-V CMOS logic process, for a 3.5 ns search time on s 6Mbit EB-CAM word, the proposed design utilizes minimum 60% less power comparatively with other distributed RAM's.

Finally, the proposed EB-CAM design allows a variable V_{bias} scheme to improve the content search speed and reduce the power per search.

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