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Design of Low Power and High Speed Shift Register

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Abstract: *In recent VLSI technologies to design any circuit main prime factors are speed and power with downscaling of chip size.Shift registers are used for temporary storage of data in processors and sequential circuits. The paper enumerates an efficient design of shift register in terms of speed and power consumption using 180 nm technology.Serial In Serial Out (SISO) and Serial In Parallel Out (SIPO) shift register has been designed using BICMOS logic. These shift registers have implemented by master slave D flip flop as a storage element.Cadence EDA tool has used to implement the proposed shift registers. Proposed design results compared with conventional design results implemented using CMOS technologyand concluded that proposed design has low power consumption and high speed compared to conventional design.*

Keywords: *BICMOS, Master-Slave D flip flop,Latch up, Cadence, Shift Register.*

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I. Introduction

Shift registers are also considered as a sort of sequential circuit which are used to store the data. They are characterized on the basis of set of flip flops connected together so that output produced by a flip flop will be given as a input for the succeeding flip flop. Single clock has given to all the flip flops along with set and reset states. As the main concern for any VLSI circuit is to reduce the delay and power consumption, researchers are continuously trying to introduce new techniques to fulfil these aims. Here SISO and SIPO shift registers have implemented by using BICMOS logic with cadence EDA tool and calculation of delay and power consumption has been performed. The aim of doing this is to compare power consumption & delay of proposed design with conventional design so that we can implement a power and speed efficient circuit.CMOS and Bipolar transistors have combined to introduce a new logic called BICMOS logic so that we can get combined advantages of both the logics. The purpose of combining these two is to design reduced power & high speed circuits. CMOS has reduced power consumption compare to BJT but with some drawbacks of high propagation delay and latch up problem. We can get some advantage with BJT logic compare to CMOS likehigh current driving capabilities and high speed.With the use of BICMOS logic, latch up problem has completely removed and we can achievecombine advantages of both BJT and CMOS logics.[1]

In previously done researchwork, many techniques have used to design shift register circuit aiming design accent like low power consumption & high speed.

In [1], Divya Bora et.al. implemented digital circuits with Tanner EDA tool using BICMOS logic to achieve advantages of large current driving capabilities, low static power and high gain. Latch up problem completely vanished with high switching speed.In [2], Raj Kumar Mistri et. al. implemented 4-bit Universal shift register (USR) using two different techniques is Transmission Gate (TG) and GDI Technique. For simulation LTspiceXVII has used.Compared to TG tech reduction in chip area,reduction in power dissipation & delay is 31.5% ,29.2% and 26.7% respectively using GDI tech. GDI technique has power dissipation of 633.8µw and average delay of 46.4µs.In [3], A.Lakshmi1 et. al. implemented 12bit Parallel in Parallel Out (PIPO) Register using 180nm technology with modified design of D flip flop. The purpose of doing this is to design a positive edge triggered conventional D flip-flop with high speed, low power consumption. This PIPO shift register has power consumption of 0.028mw.

In [4],Achyutpandey et. al. implemented a 4 bit shift registers using self-clocked D flip-flop with Microwind design and simulation tool at 90nm technologyto reduce power consumption, delay and area. SISO shift register has delay of 257 picoseconds and average power consumption of 107µw.SIPO shift register has power consumption of 182 µw. PISO shift register has power consumption of 155 µw. PIPO shift register has power consumption of 123 µw.In [5], VikasFageria et. al. used combination of Activity-Driven Optimized Clock-gating (ADOC) scheme and Run Time Power Gating (RTPG) to design 4-bitSISO shift register.Proposed design has power consumption of 2.518672e-005 and delay of 1.20 ns.

.In [6], Saranya.Met. al. proposed a design of Universal Shift Register at a frequency of 250MHz with conventional static Master-Slave flip flop configuration to improve power delay product. Simulation has performed using H spice.In [7], Noor M. Nayeemet. al.implemented reversible shift registers in all operating modes(SISO, SIPO, PISO, PIPO) and universal shift register. Lower bounds of implemented designs have shown in terms of number of gates needed to show the efficiency.

In this paperSISO & SIPO shift register have been implemented using BICMOS logic. Section 2 explains the working of proposed shift registers circuit. Section 3showingimplemented schematic designs of shift registers along with its components using Cadence Virtuoso schematic editor.Section 4 demonstrate the simulation results.Section5 concluded the paper.

II. Proposed Shift Registers

After store the data in serial or parallel mechanism for transmission of data shift register is used. In sequential manner progression of bits means serial manner and progression of bits in parallel means parallel manner. There are four different modes of shift registers based on structure. Serial-In Serial-Out (SISO) shift register is one in which with every clock one bit shifted either left or right andan input data is serially fed and shifted output also appears serially.Serial-In Parallel-Out (SIPO) shift register is one in which input data comes serially but output stored in parallel manner. Parallel-In Serial-Out (PISO)shift register is one in which input data is stored in parallel manner but serially shifted out of register. Parallel-In Parallel-Out (PIPO) shift register load input data in parallel manner simultaneously and with same clock transferred together to their respective outputs.

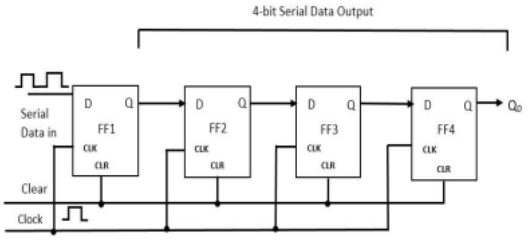

Figure 1: Circuit diagram of SISO shift register

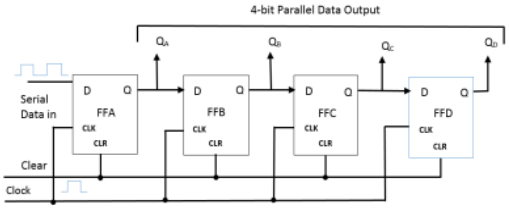

Figure 2: Circuit diagram of SIPO shift register

Master-slave D flip flop shown in figure 3.Clock inverter has used for holding the output and here is a function to disable the inputs by using clock & inverted clock.If needed to eliminate the glitches at the gate node of device, at input terminal PMOS MP3 has used. This vanishes the requirement of clock inverter at the input terminal [8]. Design accents delay & area of circuit can be reduced with the use of this phenomenon. PMOS in feedback switch has used which subsequently controlled by feedback inverter.Pull down network has NMOS. In this BICMOS circuit there is no chance of any effect due to clock skew.

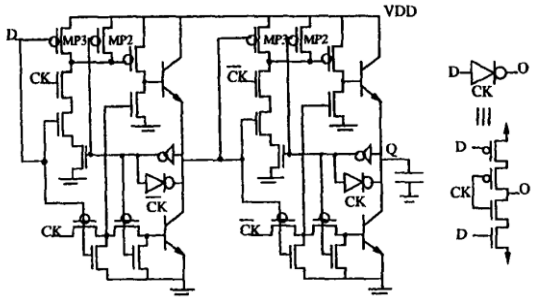

Figure 3: Master- Slave D flip flop circuit implemented using BICMOS

III. Schematic Design

For designing the schematic diagram of shift register we are needed to implement schematics of all its componentsand use all of them together as a complete circuit. Schematic diagrams of all the individual components along with SISO & SIPO shift registers have beendesigned with Cadence Virtuoso schematic editor using BICMOS logic with these specifications: Length L=180nm, Width W= 2 µm.In Figure 4 implementation of schematic for NOT gate has shown with all design specifications. In Figure 5implementation of schematic for AND gate has shown with all design specifications. In Figure 6implementation of schematic for XOR gate has shown with all design specifications. Figure 7& 8 showing schematic design of SISO & SIPO shift registersrespectively.

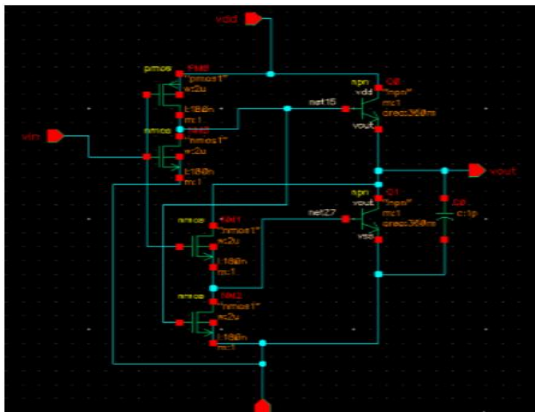

Figure 4: Schematic design implementation of Inverter

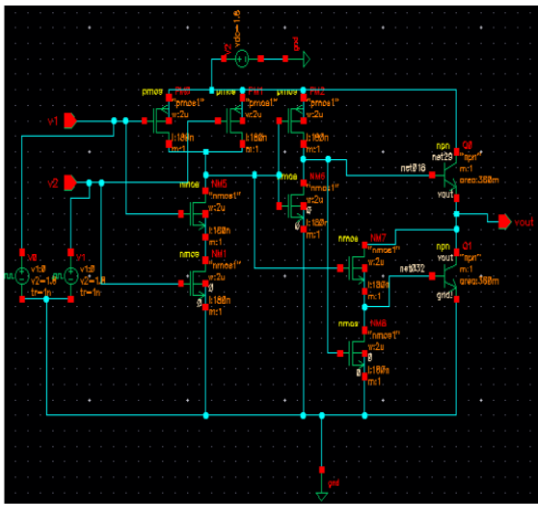

Figure 5: Schematic designimplementation of AND gate

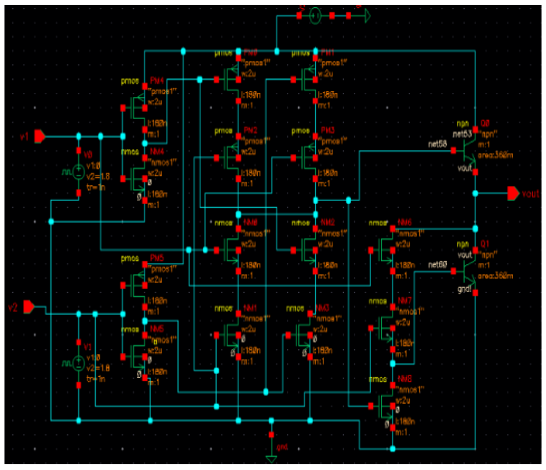

Figure 6: Schematic design implementation of XOR gate

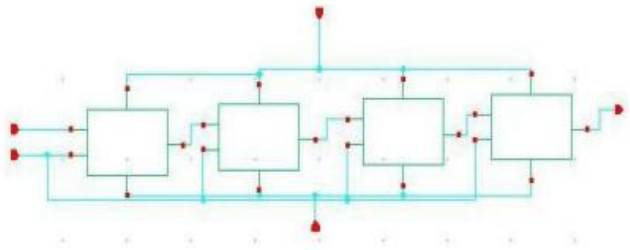

Figure 7: Schematic design implementation of SISO shift register

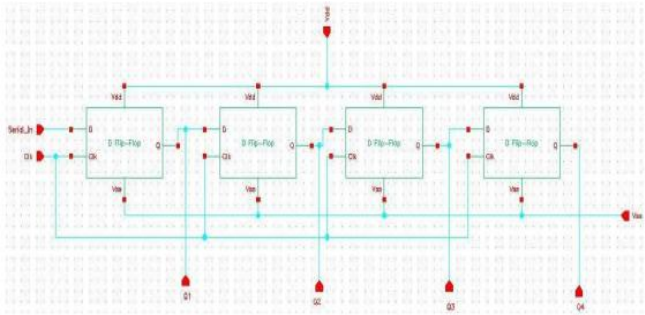

Figure 8: Schematic design implementation of SIPO shift register

IV. Simulation Results

Proposed designs of shift registers and its components have been analysed and verified using analog simulation method of cadence design environment.It is useful to demonstrate transient response for the circuit. Analysis of performance for the proposed shift register circuit has done by comparing its results of delay and power consumption with conventional design results. Table 1 & Table 2 showing this comparison. Following figures showing simulation results for inverter, and gate, xor gate, SISO & SIPO shift register.

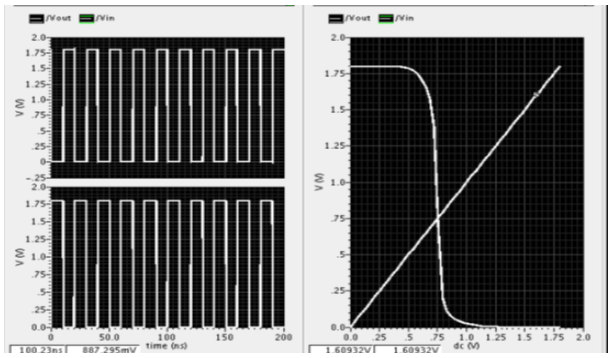

Figure 9: Simulation Design Implementation of Inverter

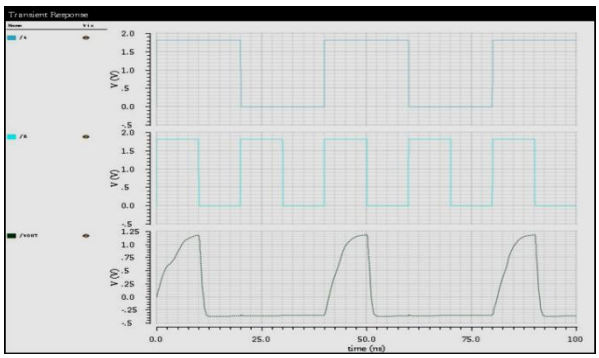

Figure 10: Simulation Design Implementation of AND gate

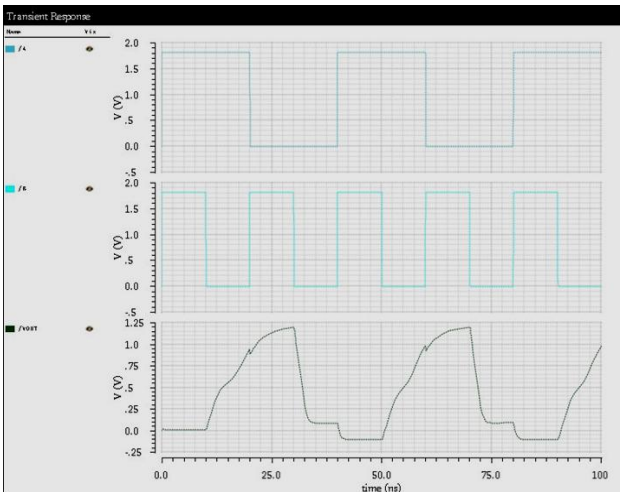

Figure 11: Simulation Design Implementation of XOR gate

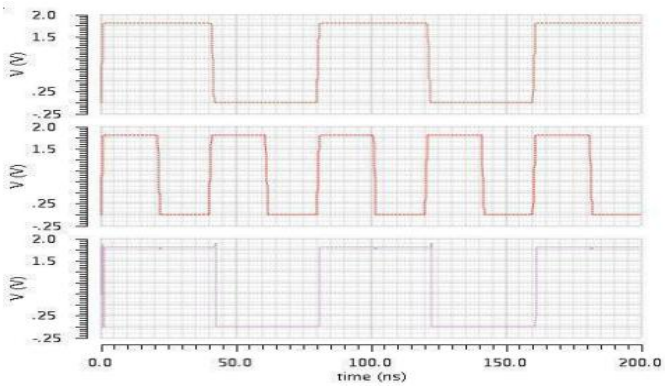

Figure 12: Simulation Design Implementation of SISO shift register

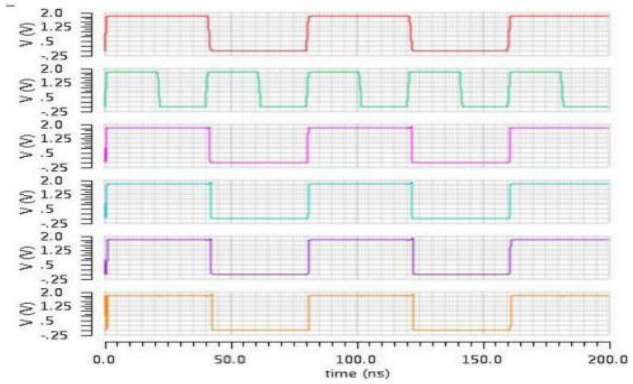

Figure 13: Simulation Design Implementation of SIPO shift register

Table 1: Comparison Table for Delay

Design Technique	Existing design using CMOS logic	Proposed Design using BICMOS logic
SISO	0.97ns	0.83ns
SIPO	0.71ns	0.59ns

Table 2: Comparison Table for Power Consumption

Design Technique	Existing design using CMOS logic	Proposed Design using BICMOS logic
SISO	0.549mw	106 µw
SIPO	0.431mw	179µw

V. Conclusion

In this paper 4-bit SISO & SIPO shift register have been implemented using master slave D flip flop. The purpose of implementing these shift registers is to reduce power consumption & delay. BICMOS logic is used todesign these proposed circuits and their results compared with results of conventional design implemented with CMOS logic. Table 1 and Table 2 showing comparison results and on the basis of this comparison it is clear that proposed shift register circuits are efficient in terms of power consumption and delay.In future work improved placement and routing algorithm can be used to optimized the design further.

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