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Design of 45nm graded Strained Si-pMOSFET and comparative analysis for high performance VLSI circuit

Pramod Martha[1],Ashish Tiwary[2],Kabiraj Sethi[3]
[1]*Assistant Professor,Gandhi Institute of Engineering and Technology,Gunupur,Odisha,India*
[2]*Assistant Professor,Gandhi Institute of Engineering and Technology,Gunupur,Odisha,India*
[3]*Associate Professor,VSSUT,Odisha,India*
Corresponding Author: Pramod Martha

Abstract: *Strain engineering has been emerged as a perfect solution for the short channel effects (SCE) such as hot electron effect and self-heating effect occurs in the device with Nano dimensions. In this work a 45nm Strained Si-PMOSFET designed and simulated in 2D ATLAS simulator. Due to strain effect the drain current observed is twice that of the Si control PMOS, also there is a decrement in threshold voltage(-0.9V).The transconductance is of 90 mS/mm. The proposed device also investigated also on the basis of the total current density and the electric field, and by comparison with conventional PMOS strained Si PMOS is suitable for modern ULSI circuits.*

Keywords: *Strain, graded junction, DIBL ,total current density*

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I. Introduction

Strained-Si technology provides a solution for aggressively scaled devices by enhancing the transport properties of both electrons and holes [1]. Tensile Strain applied to thin Silicon channel by putting a thin silicon layer above the SiGe as shown in fig.1, modifies the conduction and valence band energy levels, which results in reduction of the intervalley scattering and carrier effective mass ultimately increasing the carrier mobility. The lattice mismatch between the Si & SiGe is 4.17% results in tensile strained silicon [2].

The strain influences the carrier properties of the device especially when the device dimensions are in nano range. In this work a 45nm Strained Si-PMOSFET has been designed by following the basic fabrication steps described in section II in ATHENA and simulated in 2D ATLAS simulator of Silvaco TCAD family. The device simulation explained in section III and the results discussed in section IV.

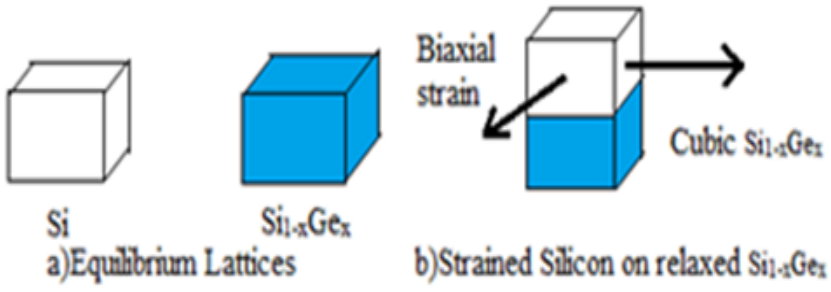

Fig.1. Schematic illustrations of (a) equilibrium lattices, (b) pseudomorphic strained Si on relaxed Si_{1-x} Ge_x.

2Device Design

The structure of the Strained Silicon nMOSFET after fabrication using ATHENA of Silvaco TCAD[3] illustrated in Fig.2.A 20nm thick graded $Si_{1-x}Ge_x$ layer with Ge content increasing from 0% to 20% deposited over the n-type Si<100> substrate. To apply strain on the Silicon layer again a thin (15nm) relaxed $Si_{1-x}Ge_x$ with constant(20%) Ge content deposited. On the relaxed $Si_{1-x}Ge_x$ layer a thin(9nm) strained-Si channel layer was grown.The gate oxide grown above the strained Si by dry oxidation at 900^0C. The extracted oxide thickness is of 57.345Å.

The entire region discussed above except gate oxide is n- type doped with Boron impurity of the order ($\sim 10^{16} cm^{-3}$). Strained-Si layer forms the channel doped with the pentavalent Arsenic of twice that of the graded $Si_{1-x}Ge_x$ layer and relaxed $Si_{1-x}Ge_x$ layer. The polysilicon doped with n type impurity phosphorus deposited and patterned. The p- type Source and drain regions were created by implanting phosphorus impurity of the order $\sim 10^{16} cm^{-3}$.

The annealing process performed to activate the carriers along with repairing the damages done to lattice due to high temperature and pressure. Thermal annealing has done at 800^0C for 30 seconds. Spacer oxide deposited and patterned by wet oxidation of polysilicon works as an insulator between three terminals. Excess oxide then selectively etched away. For metallizing the source and drain a 5nm Al has deposited and selectively etched away for metal contact. The cross section & doping profiles of the fabricated device are shown in fig. 2-4. The above processes are performed by following the fabrication processes described in [4].

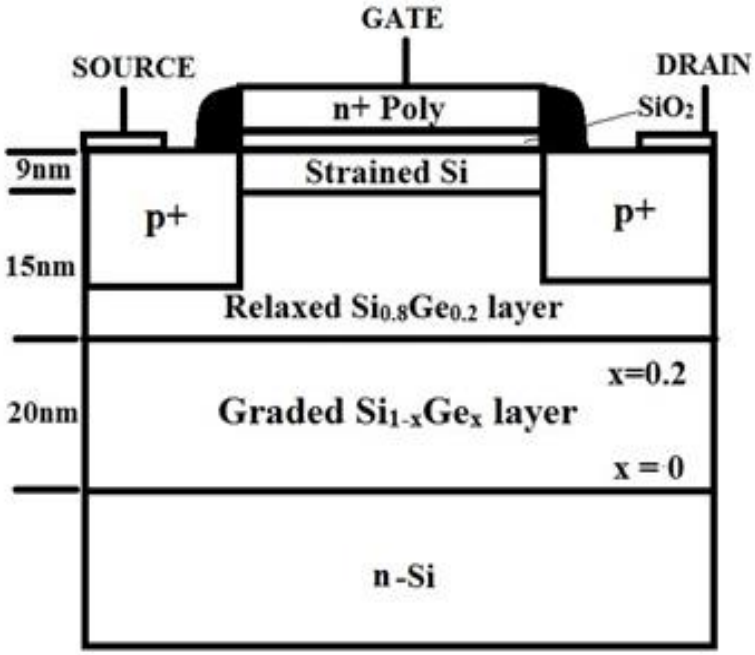

Fig.2 Cross Sectional View of Strained Si-pMOSFET

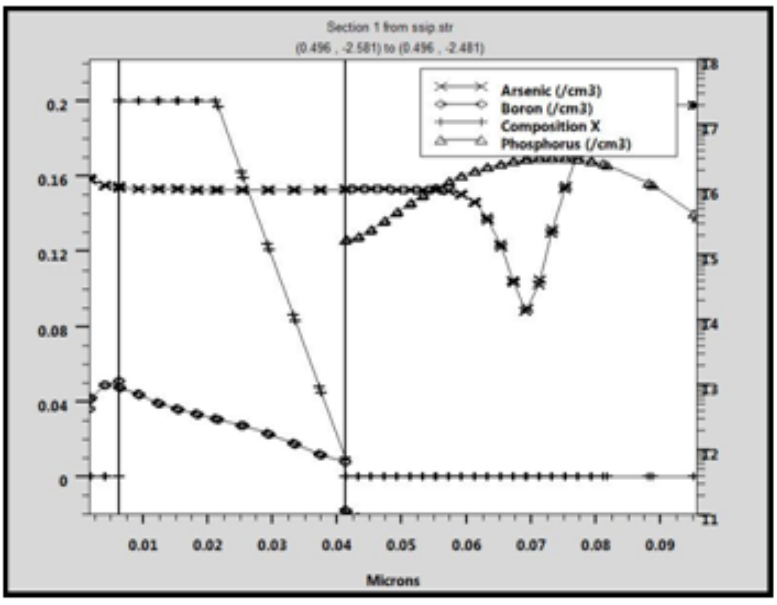

Fig.3 Concentration profile view of the 45nm St-Si pMOS

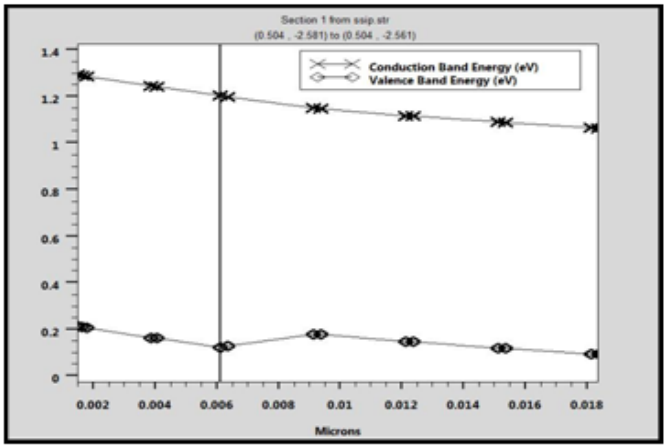

Fig.4 Energy band Structure at the interface of Strained Si and $Si_{0.8}Ge_{0.2}$

3Device Simulation

The 2D numerical solution was performed using the Atlas from Silvaco[5].To obtain the realistic result several models including Shock-ley–Read–Hall recombination(SRHmodel),Auger recombination (Augermodel),concentration-andtemperature- dependent mobility(analyticmodel),parallel electric field dependent mobility(FLDMOB model), Lombardimobility(CVT Model), were activated in simulation. Along with the above model for strained Si-PMOSFET, the temperature and doping concentration dependent Arora mobility model [6] has been employed to enhance the mobility of hole. The most important thing about the Arora model is that the mobility of carrier decided by the Ge concentration present in SiGe layer.

Along with above model, under biaxial strain, the energy band models for unstrained SiGe and strained Si were generated based on [7,8,9].The material properties used in the simulations are summarized as follows:

$\chi_{sSi} = 4.05 + 0.6x$ (1)

$E_{g(sSi)} = 1.12 - 0.4x$ (2)

$\chi_{SiGe} = 4.05$ (3)

$E_{g(sSi)} = 1.12 - 0.43x + 0.206x^2$ (4)

$\varepsilon_{r(sSi)} = 11.9$ (5)

$\varepsilon_{SiGe} = 11.9 + 4.1x$ (6)

III. Result and Discussion

Both the Strained Si and the conventional PMOSFET device simulated at different bias voltage. The simulation starts with varying the gate voltage at different drain voltage shown in fig.5 .From this it can be observed that the threshold voltage is -0.93V which is very much less in comparison to the conventional Si control PMOSFET.

Table.1. Comparision of Threshold Voltage

Device	Threshold Voltage
Conv. Si Control	-1.30V
Strained Si Control	-0.93V

The output characteristic curve(I_D~V_D) shown in fig. ,and at a particular gate voltage the performance of strained Si-pMOS is better than Si control device. Also no negative slope in the current curve for strained device obtained, which confirms that no self-heating effect.

Table.2. Comparision of Drain Current

Device	Drain Current(V_g=-3.3V)
Conv. Si Control	-0.3mA
Strained Si Control	-0.6mA

The DIBL[10] is a short-channel effect in MOSFETs originally referred to the reduction of the device Vt of the transistor at large Vd is shown in Eq. (7). DIBL in the sSi device has been studied as in Fig.6, the devicesimulated at two different drain voltage V_{d1} and V_{d2} of 3.5V and 1.5V respectively.

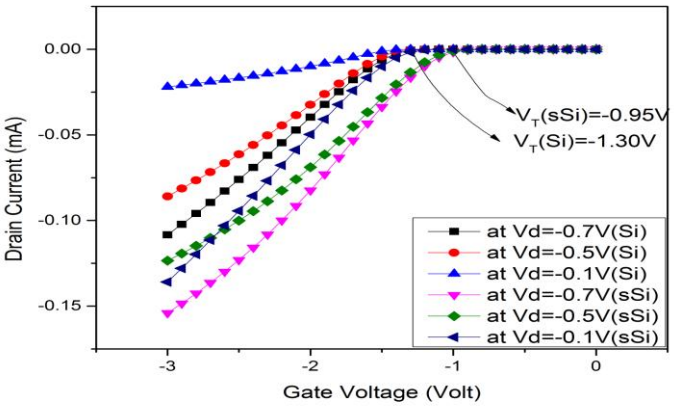

Fig.5 Current Drive Characteristic(I_D~V_{GS}) Curve

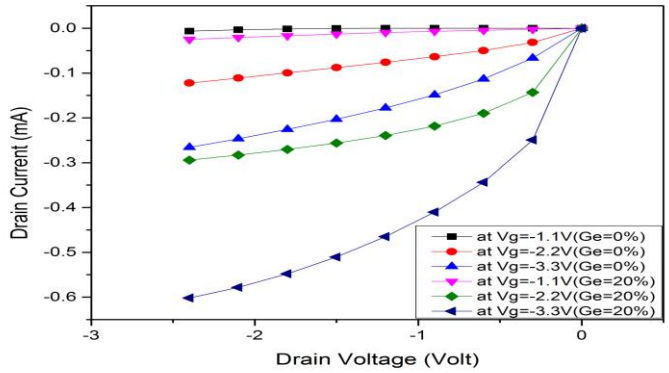

Fig.6 Output Characteristic (I_D~V_D) Curve

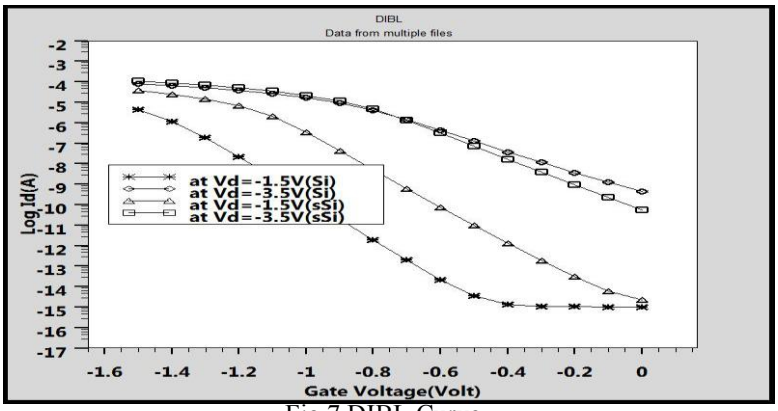

Fig.7 DIBL Curve

DIBL evaluated using:

$$DIBL = \Delta V_t / \Delta V_{ds} (mV/V) \qquad (7)$$

As the effective mass of the Si reduced due to strain effect, the mobility of hole increased and the resistance along the channel decreased. Due to this current density increased in the channel with respect to the Si control pMOSFET shown in fig. .Similarly both the devices simulated at V_{GS}=-1.1V and V_{DS}=-2.5V, the resultant electric field shown and compared in fig. .For the Strained Si the electric field in channel obtained is 2.12MV/cm and for Si control, it is 1.57MV/cm.

Table.3. Comparision of Total Current Density

Device	Electric Field	Total Current Density
Conv. Si Control	1.57MV/cm	1.08MA/cm^2
Strained Si Control	2.12MV/cm	1.81MA/cm^2

The transconductance shows the change in the drain current for a small change in the gate control voltage. So transconductance decides the device response to a very small change in gate voltage. Fig. 8 shows the transconductance of different devices varying the Ge concentration in the SiGe layer. It is observed from the fig that the transconductance value of the proposed device with Ge concentration 20% is of 0.09 S/mm which is better than other. The transconductance value can be found out by using following equation:-

$$g_m = \left(\frac{\partial I_d}{\partial V_g}\right), at\ V_{ds} = Constant \qquad (8)$$

Table.3. Comparision of Transconductance

Device	Transconductance(at Ge=20%)
Conv. Si Control	0.01 S/mm
Strained Si Control	0.09 S/mm

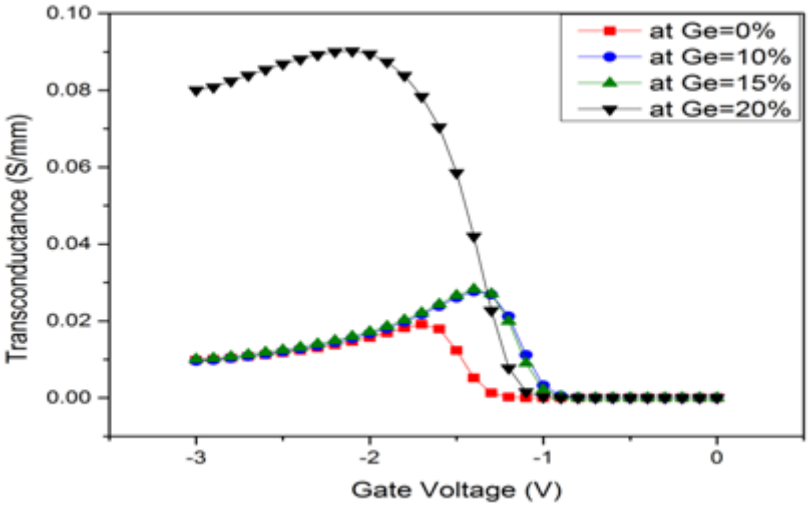

Fig.8 Transconductance at different Ge Concentration

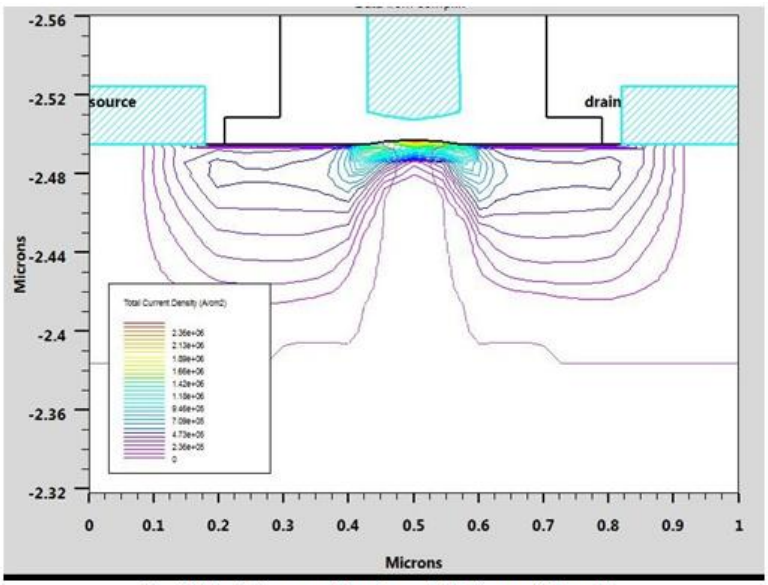

Fig.9 Total Current Density of Si Control Pmosfet

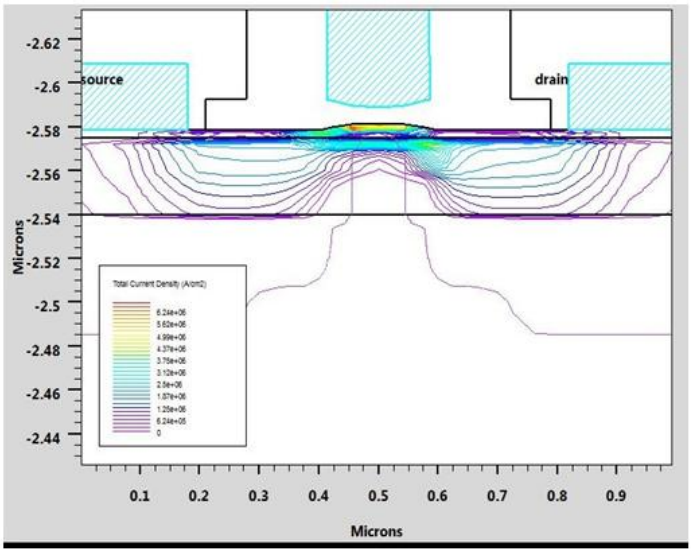

Fig.10 Total Current Density of Strained-Si pMOSFET

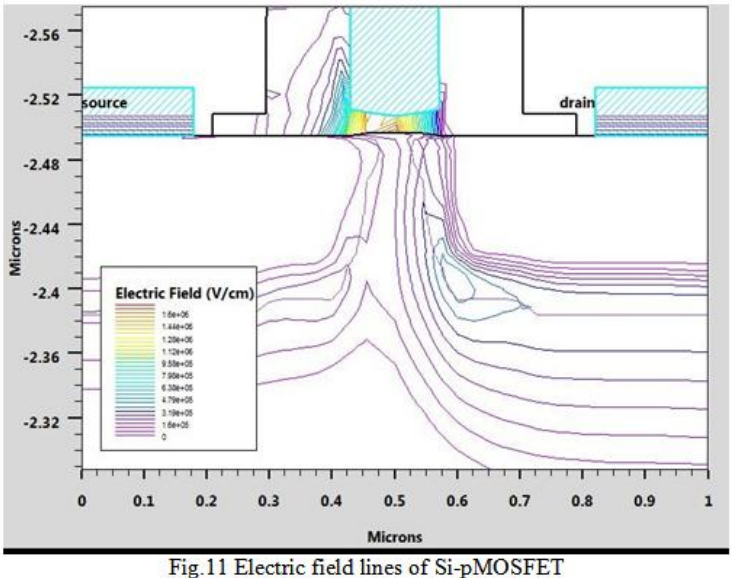

Fig.11 Electric field lines of Si-pMOSFET

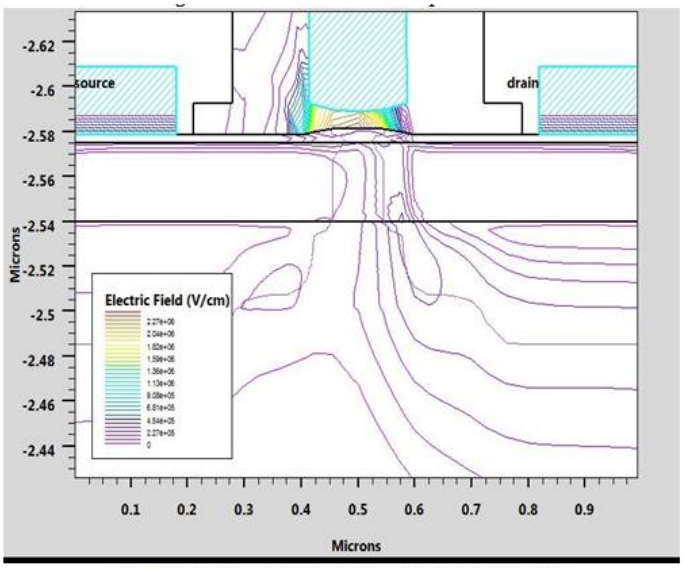

Fig.12 Electric field lines of Strained Si-pMOSFET

IV. Conclusion

Above discussion clearly suggest that in the nano regime strained silicon MOSFET emerges as a perfect candidate for high speed VLSI circuit. In 130nm range strained silicon MOSFET has high transconductance and low capacitance compared to the conventional Si control discussed in [11]. In this work same model has been implemented for 45nm St-Si pMOSFET and it has less threshold voltage and high drain current, and other parameters compared in Table 1-3. Also better transconductance of 0.09 S/mm (Ge=20%) obtained that defines the device response for a small change in gate voltage. Two new parameters total current density and electric field of both device calculated and compared.

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