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High Speed and Cost Effective Root Raised Cosine Filter using Distributed Arithmetic Algorithm

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Abstract: *Intersymbol interference in wireless communication system is considered to be a major problematic area. Root-Raised Cosine (RRC) filters are used to overcome this issue. In this paper RRC filter using DA algorithm is designed and implemented. DA or Distributed Arithmetic replaces the conventional multiplier design with Look-up tables (LUTs) for typical implementation of FPGAs. The proposed design of Root-Raised Cosine (RRC) filter is implemented and stimulated using MATLAB and Xilinx ISE environment. Virtex-2-XC2V3000 target FPGA is used to synthesize the proposed design. The design implemented and synthesized is operating at a frequency improvement of 47.9% in comparison to existing frequency to provide effective solution to the existing problems.*

Keywords: *Distributed Arithmetic Algorithm, FPGA,ISI, Raised Cosine*

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I. Introduction

The pulse shaping filter can be used in many ways like for area estimation, speed enhancement, low power consumption and other performance parameters, can be controlled in multicarrier systems. The work is designed and studied within the technology area of Wireless and Digital Signal Processing (DSP) and explains the importance of optimization of power consumption parameters and delay associated with filters with use of efficient combination of outlying circuitry [1].

Software defined ratio (SDR) flexibility can be improved using variable sampling rates which can be applied to various applications of Digital Signal Processing. Filters applying anti-aliasing can be reduced and processing using variable sampling rates is possible. Such Digital signal processing based complex applications find much space among SOC implementations' having lower cost, providing high performance and find much demand among design as well as research engineers [2, 4]. FPGAs find maximum application in Digital Signal Processing (DSP) system. DSP processors are outdated in comparison to FPGAs which provide more organized solutions for implementing DSP applications providing higher throughput. FPGAs have found an unstoppable demand for systems requiring lesser hardware providing better cost efficiency. FPGAs find various benefits in implementation to DSP applications. Some can be listed as lesser power consumption, potentially smaller area for additional applications and cheaper implementation. The architecture of DSP processors having sequential architecture prohibits it from performing in accordance to the technical market demand. This time-to-market factor, high performance, development cost and facilities related to ASIC designs have been overcome by FPGAs [5, 6]. Conventional DSPs and FPGAs work in coexistence, integrating both pre- and post- processing systems providing high performance processing system. FPGA implementation generally deploys functions of Finite impulse response Filters (FIR). Fully parallel architecture can be used if sampling rates required are high and where new input samples are fed at every clock edge and a new output sample is produced. FPGAs can provide platform for such filter designs applying combinations general logic fabric embedded arithmetic hardware and onboard RAM. Computing systems have found a new face which is highly efficient and advancing quickly. Developments in the past have show that FPGAs can extensively reduce the cost of development in a system and if compared to various attributes of commercially available processors then the results are highly competitive. MAC filter functions based on FIR system can be traditionally performed in serial manner by DSP chips. Whereas in case of FPGAs the designer has the freedom to implements its design in parallel fashion using resolute registers and multipliers which are available in latest FPGAs. High parallel architectural implementation of FPGAs in DSP applications that enhances the system performance founds its virtue in global market. Though, a trade-off is always present among area and performance parameters. Which could be overcome by selecting appropriate parallelism level for function implementation? Integration of system logic forms an additional merit to FPGAs implementation. This paper presents the implementation and designing of Raised Cosine Filter using distributed arithmetic (DA) procedure.

II. RRC Filter

Raised Cosine Filter is used to avoid interference, rectangular pulse infinite bandwidth is not considered in such cases. Rectangular pulse is passed through a low pass filter and we can observe the shape change from rectangular pulse to a pulse with no sharp edges and smoothly outlined. Therefore it is also known as pulse shaping process. The rectangular pulse exhibits non zero amplitude and smooth pulse exhibits few ripples prior and post pulse interval. The ripples can cause decoding of data in an incorrect manner at the receiver end as this ripple interferes with the pulses. The interference can be made minimum by maintaining a time domain shape and such a filter selection that provides the desired reduction in bandwidth. It finds its application in wireless devices and cellular phones for increasing speed, reducing power consumption and area [7]-[10].

$F(w) = \tau \quad 0 \le w \le c \quad (1)$

$= \tau \{\cos^2[\tau(w-c)/4\alpha]\} \quad c \le w \le r \quad (2)$

$= 0 \quad w > r \quad (3)$

Where

τ is the pulse period

α is roll off factor

c is equal to $\pi(1-\alpha)/\tau$

r is equal to $\pi(1+\alpha)/\tau$

Raised Cosine Filter is very helpful in pulse shaping; it makes the signal compatible for the channel. It makes channel interference or noise free, in hardware implementation of filter by changing the suitable factors the designed filter can be used in different application and area and speed can be optimized.

III. DA Algorithm Based Interpolator

FPGA devices have a huge amount of implementations using Distributed Arithmetic (DA) algorithms. Modulo Arithmetic, Distributed Arithmetic, etc. are some of the efficient computation techniques that performs multiplication and addition using these schemes. Crosiers firstly introduced this multiplier less architecture deploying partially the partition of the function, implying the usage of 2's complement in data binary representation. Look Up tables and accumulators have replaced the usage of multipliers, thus providing multiplier-less MAC operations. Improved speed and efficient calculations form few of the important features of the DA technique. Non-zero coefficients representing the FIR frequency response can be minimized using this approach. This approach for modification can be implemented for various raised cosine FIR filters [11]. Sum-of-product calculations find major application in multimedia domain. In distributed arithmetic rearrangement and blending of multiplication is done such that the arithmetic gets distributed. FPGAs memory is helpful in MAC operation implementation. DA suits well to FPGA realization as LUTs along with shift-add-operations can be well mapped into LUTs target FPGA structures [12]. These can be expressed as

$$y = \sum_{k=1}^{k} A_k X_k \quad (4)$$

X_k given an N-bit 2's complement number

$$X_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \quad (5)$$

$$y = \sum_{k=-1}^{k} A_k [-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n}] \quad (6)$$

$$y = -\sum_{k=1}^{k} (b_{k0} A_k) + \sum_{k=1}^{k} \sum_{n=1}^{N-1} (A_k b_{kn}) 2^{-n}$$

$$y = -\sum_{k=1}^{k} A_k b_{k0} + \sum_{n=1}^{N-1} [\sum_{k=1}^{N-1} A_k b_{kn}] 2^{-n} \quad (7)$$

Interpolation is simply the process of up sampling together with by filtering. The filtering removes the undesirable spectral images. Not to be confused, it is a linear process, interpolation which is somewhat different from the "math" sense of interpolation, but on the other hand the interpolation factor which is simply the ration of the output rate to the input rate. It is usually symbolized by "L".

IV. Matlab Based Interpolator

The proposed FIR interpolation filter uses a roll off factor value of 0.25 and is simulated using Gaussian window with interpolation factor of 8. Further the designed raised cosine filter is quantized in MATLAB environment. The filter length considered is 48, the hardware architecture of the filter design is reduced by using DA algorithm. DA algorithm is used as it is a multiplierless technique which plays key role in making the filter cost effective. The Fig. 1 shows the magnitude response of RRC filter, which depicts magnitude frequency relation of direct form FIR polyphase interpolator which is quantized at fixed point representation and Fig. 2 shows the impulse response of RRC filter.

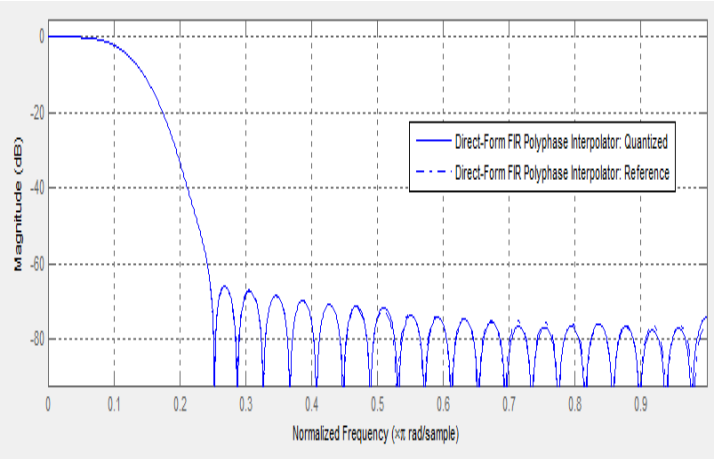

Fig. 1 Magnitude response of RRC filter

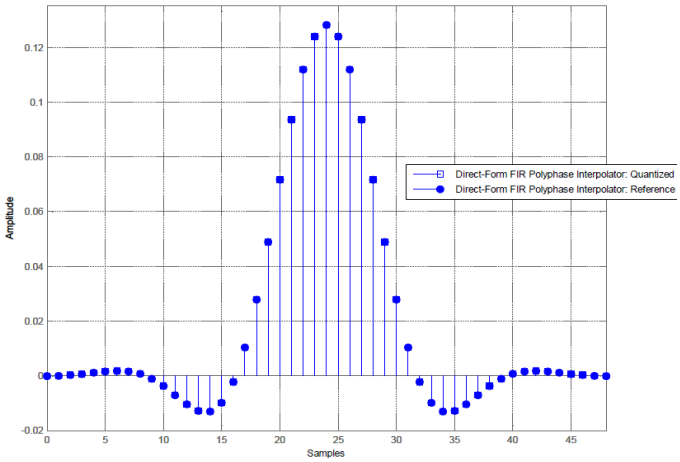

Fig. 2 Impulse response of RRC filter

V. Hardware Synthesis

The newly designed filter is further simulated on Xilinx platform, which provides a placing and routing report of the proposed filter. In this research work Virtex 2 development system is being utilized which provides a hardware platform that is much advanced and contains high performance Virtex 2 platform FPGA. This platform is surrounded by peripheral components collectively and helps in creating a complex system that can demonstrate Virtex 2 platform FPGA's capability.Figure 3 shows the simulation of RRC filter using Virtex 2. In this the main focus is on designing a filter which consumes less space and provides output which takes less speed than the previous work.

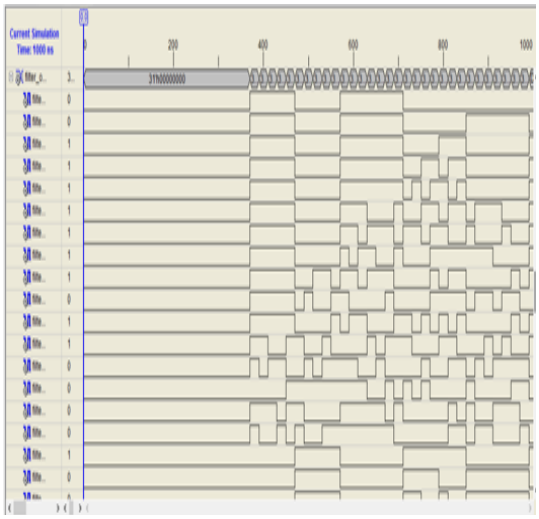

Fig.3 ISE Simulated based Response

VI. Synthesis Results

The proposed 49 tap filter is based on direct II form architecture. The implementation of the proposed work is carried on target device XC2V3000-4FF1152 using Xilinx ISE 10.1 EDA tool. The reconfigurable architecture designed is optimized. Table I shows resource utilization report which gives the clear picture about area and delay.

Table. I Resource Utilization Virtex 2

Parameters	**Proposed Work Tap 49 16x17 bit**
Target Device	XC2V3000-4FF1152
Number of Slices	733
Number of slices flip-flop	622
Number of 4 Input LUTs	1101
Number of bonded IOBs	51
Total equivalent gate count	15175
Maximum Frequency (MHz)	86.88

Table II shows the comparison between proposed and previous work on FPGA platform, which shows 36.7% improvement in the LUT consumption, 48.42% improvement in the total equivalent gate count and 47.49% improvement in the maximum frequency.

Table. II Resource Comparison

Parameters	**Previous Work** [1]	**Proposed Work**
Number of 4 Input LUTs	1742	1101
Total equivalent gate count	29425	15175
Maximum Frequency (MHz)	58.9	86.88

Fig. 4 shows the comparison between the previous and proposed work of resource utilization and clearly shows the benefit of this research work over the later.

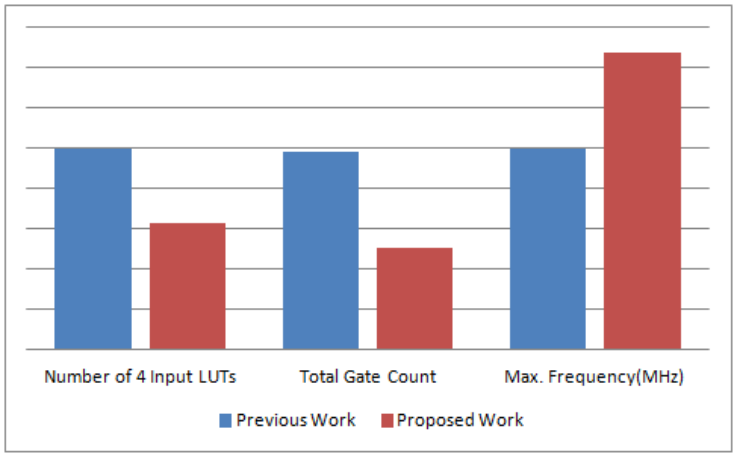

Fig. 4 Comparative Analysis

VII. Conclusion

This research work gives a view of multiple challenges and problems faced during the designing of a reconfigurable filter utilized in multi carrier system. This research work proposes an optimization technique of two steps to overcome the problems and challenges and helps in getting the desired filter that is efficient in terms of reducing the area consumption. The proposed solution provides improvement in the maximum operating frequency of 47.49% in the designed filter. The proposed work shows improvement in the LUT consumption of 36.7% and 42.42% in case of total equivalent gate count. The comparison of previous and proposed work clearly showcase the benefits of the proposed work in terms of area and speed consumption. The proposed work therefore seems best fit for the next generation 3G/4G/5G applications where power and area needs to be optimized.

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