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Lowering Power Delivery Issues in 3D-IC

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Abstract: *Scaling of transistor size has provided new possibilities in VLSI industry. 3D IC opens door to tremendous applications. The major concern in 3D IC is power dissipation which occurs both in static and dynamic mode of operation. The major parameters on which the power consumption depends on are the supply voltage, clock frequency, die Area, Feature size and number of gates. We have taken the parameters in such a way so that our power consumption got reduced to a lesser amount. we aim to showcase a flow to tackle this problem with following parameters:*

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Table 1 : Value of variants.

S.NO	VARIANTS	VALUES
1.	Feature Size of IC	10 Nanometres
2.	Die Size	60 square millimeters
3.	Clock Frequency	0.4 GHz
4.	Number of Gates	60 Million

I. Introduction

Scaling of transistor size has provided new possibilities in VLSI industry. 3D IC opens door to tremendous applications. The major concern in 3D IC is power dissipation which occurs both in static and dynamic mode of operation. Static mode of operation means device is inactive and in dynamic mode of operation device is in working mode. Previously power dissipation in static mode was negligible but now a days with increase density and high frequency of operation power dissipation in static mode is non negligible. In 3D-ICs which contain million of devices in very small area the leakage current increases to a considerable value and causes power dissipation. To reduce this there are various techniques have been proposed. The major parameters on which the power consumption depends on are the supply voltage, clock frequency, die Area, Feature size and number of gates. As we know that, the lower supply voltage uses less power, so, this factor should be low.

Mathematically, we can say that power consumption is given by

$P = C * V^2 * f$

Where P is the Power Consumed
C= Capacitance
V= Supply Voltage
f= frequency of operation

At the technological and architectural level we can try to minimize the variables in these equations to minimize the overall energy consumption. One of the effective way of reducing power at the technological level is reducing the supply voltage, because the power consumption drops quadratically with the supply voltage. However, lowering supply voltage results in reduction of performance Another option is to reduce the frequency but that may cause longer delay, as system may take longer time to perform same task with lower frequency. So, to reduce the Power Consumption from the above formula, we have taken the lesser clock frequency for achieving the better results. Along with that, we have taken the lesser supply voltage. If the product of V^2 and f are lesser, then Power Consumption will also reduce. In the end, we got the Pie chart for Simulation which is showing the Power Consumption for an IC with a feature size of 10nm, Clock frequency 0.4 GHz, Die size of 60 sq.mm and having a60M number of gates.

Logic Gate Area = 2.09 sq.mm
Repeater Area = 11.02 sq.mm
Average wire length = 6.8 gate pitches
Average logic gate size = 10.0

Total Power Consumption = 0.7 W
Logic gate power: Dynamic = 0.0W and Leakage = 0.02W
Clock power: 0.05W
Repeater power: Dynamic = 0.04W and Leakage = 0.39W
Interconnect power: 0.17W

Figure1: Pie Chart for Simulations

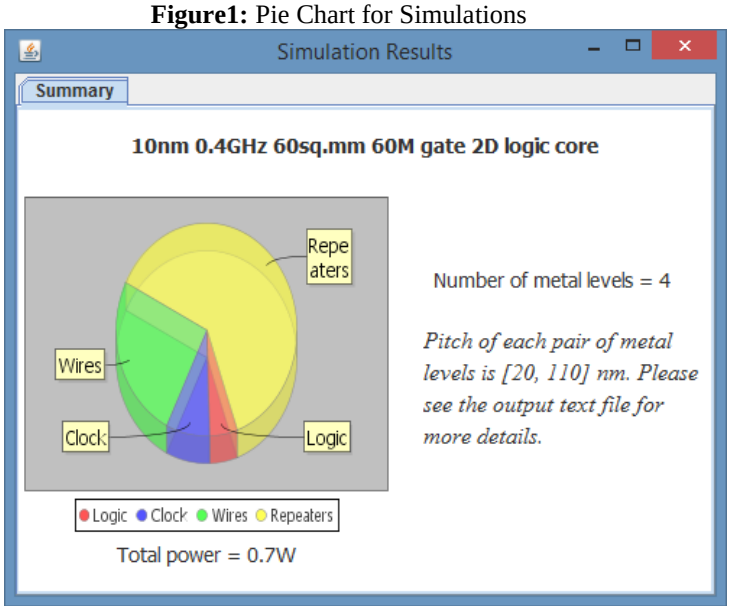
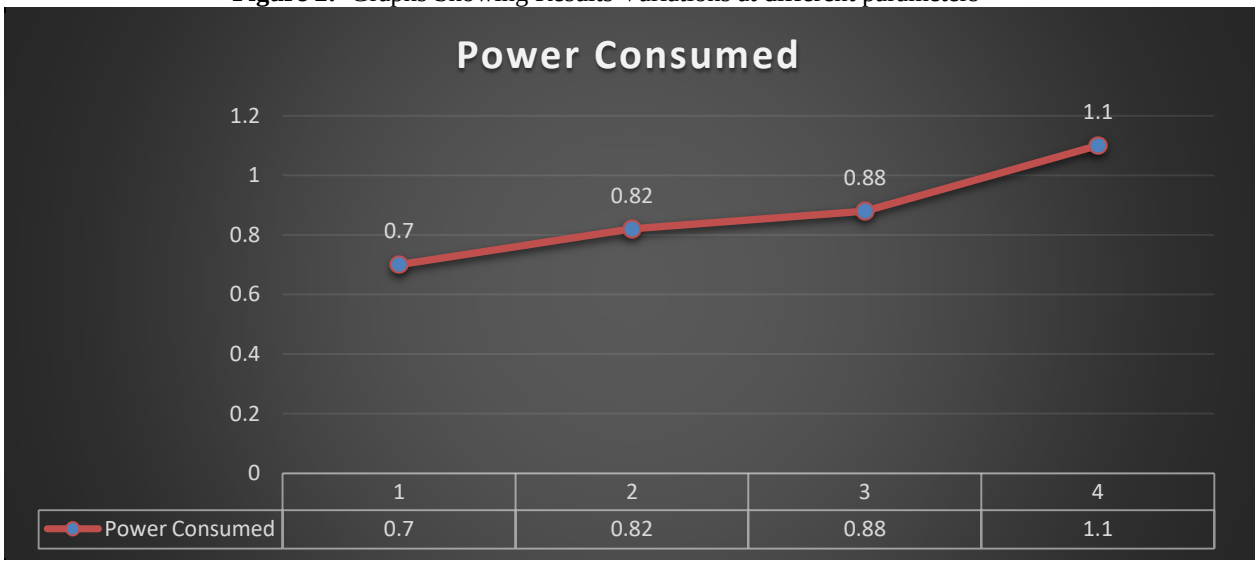


Table 2 : Value of variants parameters.

S. No	Size of IC	Die size	Clock frequency	Number of Gates	Output Power
1.	10	60	0.4	60	0.7
2.	18	70	0.5	100	0.82
3.	15	80	0.55	120	0.88
4.	22	50	0.6	196	1.1

Figure 2: Graphs Showing Results Variations at different parameters



II. Conclusions

Power consumption is major issue in designing 3D ICs but with balanced reduction of input power supply and lowering clock frequency within range that does not affect the system performance we can achieve reduction in power dissipation which majorly solve the issue of thermal issues associated with 3D-ICs, and reduce the chances of thermal breakdown.

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