PCIe BUS: A State-of-the-Art-Review

Anuj Verma[1], Pawan Kumar Dahiya[2]

[1]. Student of M.Tech. in ECE (VLSI Design) in DCRUST, Murthal, anujsusniwas@gmail.com.
[2]. Assistant Professor in ECE Dept. in DCRUST, Murthal, pawan.dahiya@gmail.com.

Abstract: *PCI Express (Peripheral Component Interconnect Express) abbreviated as PCIe or PCI-E, is designed to replace the older PCI, PCI-X, AGP standards. A data communication system is developed for use the transfer data between the host and the peripheral devices via PCIe. The performance and the available area on the board are effective by using the PCIe. PCIe is a serial expansion bus interconnection method which is use for high speed communication. PCIe represents the currently fastest and most expensive solution to connect the peripheral devices with general purpose CPU. It provides a highest bandwidth connection in the PC platform. In this paper, the different types of bus architecture are reviewed. Further, it is described how data transfer take place between the CPU to the destination in PCIe architecture.*
Keywords*: PCIe, AGP, PCI-X, PCI*

I. Introduction

Peripheral Component Interconnect Express (PCIe) is a serial expansion bus standard used for attaching one or more peripheral devices (Mouse, Image scanners, Microphones, Loudspeakers, Digital Cameras, Tape drives and other devices) with the Computer . It is a serial expansion bus which transfers the data between the internal hardware of the computer (including CPU and RAM) and peripheral devices [4]. It is a standard bus that allows for the exchanging the data from one point of a computer to another point.

PCIe is designed by Intel, Dell, HP and IBM in 2004. It is the improved version of PCI-X (Extended). PCIe is usually deployed with different 1, 4, 8, 12, 16 or 32 lanes for the implementation to the motherboard [3]. It supersedes the different computer buses as Accelerated Graphics Port (AGP), Peripheral Component Interconnect Extended (PCI-X), Peripheral Component Interconnect (PCI), In this paper, all these bus standards are compared with the PCIe.

Each peripheral device which is connected with the motherboard through the PCIe link has a dedicated point-to-point connection with the PC. This means that devices are ready to communicate with the PCs but due to different bandwidth with PC units they will not share the same bus. To communicate with the multiple devices, PCI Express use switches for established the connection [5]. PCI Express switches works as an endpoint and this endpoint can connects with multiple PCI switches. Thus multiple devices can connect with the PCs.

The contribution of the paper is as under:
* Different types of bus architecture are reviewed.
* The data transfer process between CPU to destination in PCIe architecture is also explained.

The rest of this paper is organised as under:

Section 2 has the literature survey. In Section 3, PCIe is discussed in detail how the PCIe works with the Physical layer, data link layer and the Network layer. Section 4 shows discussion and comparison of these buses. Section 5 concludes the paper.

II. Literature Survey:

Now a day, computers have become the essential part of the human life. Computer which have very high transfer rate of data is used for the communication. High transfer rate is achieved by the data bus which is used in computer [2]. Here are the different bus architecture which is discussed as: Accelerated graphics Port (AGP), Peripheral Component Interconnect (PCI), Peripheral Component Interconnect extended (PCI-X), and Peripheral Component Interconnect Express (PCIe) bus standards.

2.2 ACCELERATED GRAPHICS PORT (AGP):
* Accelerated graphics port (AGP) has a peer-to-peer connection between the CPU units and the external devices
* Mostly, AGP uses for attach video card with the computers.
* AGP do not share the buses with the processor. It provides a dedicated path with the slot established into the motherboards. It has high clock speed which allows high transfer rate of data.
* AGP has separated address path and data path for the transactions.

- The AGP bus sends many addresses to the processor and a host processor will process on this address. This technique reduces the delay and idle state of bus.

2.3 PERIPHERAL COMPONENT INTERCONNECTS (PCI):
PCI is a computer bus for connect hardware devices with the computer. It is a parallel synchronous bus, which sends data parallel to the devices. The transactions of PCI is Burst oriented. PCI bandwidth is best utilizing the burst mode.

- **Synchronous:** PCI is a synchronous bus that means it uses single clock and the clock runs at 33MHz by default but can run lower just to save power and can runs to higher if the hardware needed.
- **Transaction/Burst Oriented:** The transactions of PCI is Burst oriented. For the transaction in the PCI, firstly start the specific address and start to transfer the data in burst form. PCI also has 32 lanes of transferring data. Once the address is specified, many data cycle can go through the PCI.
- **Bus Mastering:** Bus Mastering means that it works in master slave configuration. Master is using for initiate the transactions (read or write) between the CPU and the host and slave response to the initiated transactions.
- **Plug & Play:** In plug and play, the host computer will determine the identity of PCI port in the PCI bus such as manufacturers, functionality, video and the network devices. It also determines the ability about the memory and interrupts as well.

2.4 PERIPHERAL COMPONENT INTERCONNECTS-EXTENDED (PCI-X):
      PCI-X is revised version of conventional PCI bus. The clock speed of PCI-X is double the clock speed of PCI from 66 MHz to 133 MHz [8] and hence the data exchanged between the computer processor and peripherals devices is doubled. The amount of data transaction between the CPU and peripheral devices is 1064 MB/s with the PCI-X bus and 133MB/s with the PCI bus. The efficiency and data storage capability of PCI-X also improves and the fault tolerance capability of PCI-X also improves then the PCI. The PCI-X features are described as;

- There is a master ready signal (IRDY) and a slave Ready signal (TRDY) which will defines the initialize the transaction of data through the PCI bus. These TRDY and IRDY signal has been deleted from PCI-X and PCI-X allow the data to be transmitted into the burst mode.
- Frame signal should not be asserted before the end of transaction.
- The master device cannot be in wait state but a slave device may be in wait state so target/slave device has to be in wait state until the data is not transferred from the master device to the slave device.
- The burst size of the PCI-X bus transmission is decided before start the transmission.

III. Peripheral Component Interconnects Express (PCIe):
PCIe is a serial expansion bus standard for connecting a computer to one or more peripheral device. PCIe works on the different lanes. The transaction speed of PCIe is varying with the different PCIe architecture. It is a packet based protocol in which the packet contains the address and the data. The bridge forwards a packet to the targeted devices. Table 2 shows the characteristics and features of different PCIe architecture.

3.1 PCIe FEATURES:
    The key features of PCIe are listed as under:

- It is a point to point master-slave configuration.
- It is a serial bus architecture which requires fewer pins than parallel bus.
- **Scalable:** Scalable means that if a single lane is able to transfer the data 2 GB/s than another lane can transfer 4GB/s. This is the scaling of the bandwidth.
- It is a packet based transaction protocol.
- PCIe has the same memory, I/O, configuration address space as PCI.
- The data integrity and error handling capability of PCIe is better than the PCI.

3.2 PCIe ARCHITECTURE:
      The PCIe bus is a serial bus expansion which works on the three different layer out of the seven layer of OSI model. These three layers are physical layer, data link layer and the transaction layer. The data is passed through these layers. The mechanism of PCIe standard is plug and play based PCI.
      The Physical layer provides the point-to-point serial connection between the peripheral devices and processor unit of PCI. The read and write requests transportation occurred in transaction layer. The mechanism of the PCIe is depends upon these layer. The packet-based transaction and the split transaction protocol occurred

in the transaction layer. The link layer is used to linking the sequence numbers and CRC of the packets for the transaction layer. This linking provides a highly reliable data transfer mechanism [1]. The physical layer have a transmit pair and a receive pair. The combination of transmit pair and the receive pair is called a lane. The bandwidth of the PCI Express lane is about the 250MB/s in each direction. Now a day, the PCI board data rate can be increase by fold it's twice or fourth times. This bandwidth is providing for the same devices.
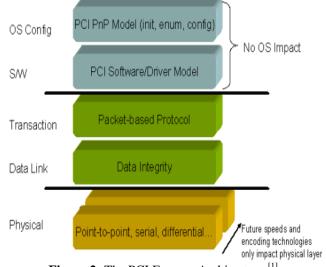

Figure 2: The PCI Express Architecture [1].

3.2 PCIe TOPOLOGY:
PCIe Topology will help to understand that how the different peripheral devices will communicate with the CPU through the PCIe link. The CPU will access the root complex in order to configure the IP and CPU will also configure the different endpoint with the help of root complex. The root complex can directly access the memory. Thus, the PCIe endpoints will communicate the CPU and the memory with the help of root complex as shown in figure 3.

We can attach many PCIe endpoints with the root complex with the help of PCIe Switches. These different components will communicate between the CPU or Memory and peripheral devices through the PCI express expansion bus. These PCIe endpoints can read and write data from the memory.
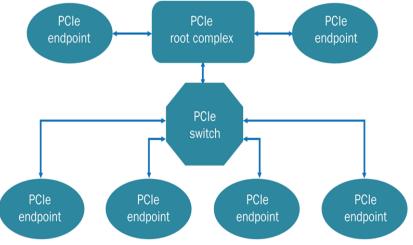

Figure 3: The PCIe Topology [8].

3.4 PCIe STACK:
Packets should be serially assembled and transaction of packets is occurred in different three layers: Transaction layer, Data Link layer, Physical layer [3]. After passing these three layers, data is interchange among the devices. The Transaction Layer control to the data packaging and flow of the package in the peripheral device with the CPU units. The Data Link Layer provides the link between other two layers and also do error management between the layers. The Physical Layer is a collection of physical link, 8b/10b encoding, interface

initialization and scrambling. The physical and Data Link Layer works internally but the transaction layer works with the devices. Mainly, PCIe works on the Transaction Layer Packets (TLPs)[1].

The link layer is responsible for the packet delivery by the PCI express link. The link layer also link the sequence number with the CRC and send it to the transaction layer as shown in figure 4.
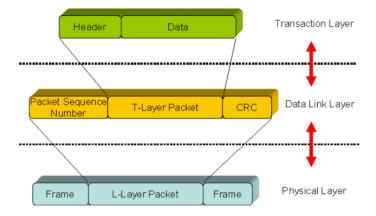

Figure 4: The data link layer adds data integrity features [1].

The packet of data is send to the other end of system only when a buffer is ready to collect the data which eliminates the wastage of bus bandwidth due to resource constraints. If the signal is corrupted at the time of transaction, the link layer will automatically retain the packet.

IV. Comparison And Discussion:

Table 1: Comparison of different buses.

BUS	YEAR	INTRODUCED BY	SPEED(Mbps)	STYLE	WIDTH(bits)
PCI	1992	INTEL	133-533	Parallel	32/64
AGP	1996	INTEL	2133	Parallel	32
PCI-X	1998	IBM, HP, COMPAQ	1064	Parallel	64

Table 2: Comparison of different PCIe Architecture

PCI Architecture	Raw Bit Rate(GT/s)	Interconnect Bandwidth(GB/s)	Bandwidth Lane Direction	Total Bandwidth for x16 link(GB/s)
PCIe 1.1	2.5	2	~ 250 MB/s	~ 8
PCIe 2.0	5	4	~ 500 MB/s	~ 16
PCIe 3.0	8	8	~ 1 GB/s	~ 32
PCIe 4.0	16	16	~ 2 GB/s	~ 16

As shown in the table 1. The PCI-extend has the bus width of the 64-bits and the highest speed of data transfer is 2133MBPS by the AGP bus. After the PCI-X, a PCIe bus is introduced which has the different speed rate with the link. As discussed in table.2 interconnect bandwidth of PCIe 4.0 is highest than the other version of PCIe.

V. Conclusion

While the PCIe protocol promises high bandwidth, the switching capacity of the PCIe high latency over the older bus architecture as (AGP. PCI, PCI- X). Here, we presents different bus architecture and compare these with the PCIe . Now PCIe is explored with its new architectures which have high speed, high bandwidth and high bit rates. PCIe designs pose significant challenges to designers. The requirements for the interface, depending on whether the PCI Express device has to connect to another end points, root complex and switches

References

[1]. The NI website [online]. Available: http://www.ni.com/white-paper/3767/en/#toc5/.
[2]. The hardwareverification.weebly.com website [online] Available: http://hardwareverification.weebly.com/pci---express-architecture.html.
[3]. Hossein Kavianipour, Steffen Muschter, Christian Bohm, "High Performance FPGA-Based DMA Interface for PCIe", IEEE Transactions on Nuclear Science, vol.2, pp no. 745-750, April 2014.
[4]. Hossein Kavianipour, Christian Bohm, "High Performance FPGA- Based Scatter/Gather DMA Interface for PCIe", IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC), pp no. 1517-1520, 2012.
[5]. K. Harish, H.S. Aravina, "Development of 8-lane PCI-Express Protocol using VHDL", International Journal Advanced Networking and Applications, vol. 3, pp no. 1169-1175, 2011.

[6].   Ankita R. Tembhare, Pramod B. Patil, "Design & implementation of PCI Express Bus Physical layer using VHDL", International Journal on recent and innovation Trends in Computing and Communication, vol.2, pp no. 1883-1886, july 2014.

[7].   Iqbalur. Rahman Rokon, Towsif. Sazzad, Samilat. Kaiser, "Hardware Implementation of PCI Interface using Verilog & FPGA", International Conference on Electrical, Electronics and Civil Engineering(ICEECE), pp no. 199-203, Dec. 2011.

[8].   The embedded website, Available: http://www.embedded.com/print/4374518.