IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 7, Issue 3, Ver. I (May. - June. 2017), PP 42-45
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and FPGA Implementation of AMBA APB Bridge with Clock Skew Minimization Technique

M. Kiran Kumar[1], Amrita Sajja[2] Dr. Fazal Noorbasha[3]
[1,2]*Assistant Professor, Dept of ECE, Anurag Group of Institutions, INDIA*
[3]Associate Professor, Department of ECE, KL University, *INDIA*

Abstract: *The Advanced Microcontroller Bus Architecture (AMBA) is used as the on-chip bus in system-on-chip (SoC) designs. APB is low bandwidth and low performance bus used to affix the peripherals like UART, Keypad, Timer and other segment equipment's to the bus architecture. The aim of this paper is to design and implement AMBA APB (Advanced Microcontroller Bus Architecture - Advanced Peripheral Bus) Bridge with efficient deployment of system resources. Clock is a major concern in designing of any digital sequential system. Clock skew is introduced when the difference is generated between the arrival times of clock signal. One of the approaches to minimize clock skew is ripple counter. The three bit down ripple counter approach used. APB Bridge with clock skew minimization technique is implemented in the paper using Verilog HDL. For the simulation purpose, Vivado Design Suite ISim has been used. For the synthesization purpose and design utilization summary Vivado Integrated Design Environment (IDE)*

Keywords*: System on Chip (SoC), Verilog, AMBA, APB Bridge..*

I. Introduction

Integrated circuits have embark the era of System-on-a-Chip (SoC), which refers to integrating all peripherals of a computer or other electronic system into a single chip. The advanced microcontroller bus architecture (AMBA) is used as the on-chip bus in system-on-chip (SOC) designs. Since the inception of AMBA has astray for furthermore microcontroller peripherals, and is now extensively used on a range of ASIC and SOC components including applications mainframes used in latest portable mobile devices like smart phones. The AMBA protocol is an open standard, on-chip interconnect specification for the concurrence and management of functional blocks in a system-on-chip (SoC).It facilitates right-first-time development of multi processor designs with large number of controllers and peripherals. An AMBA-based microcontroller roughly endure of a high-effort system backbone bus (AMBA AHB or AMBA ASB), able to maintain the extrinsic memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) peripherals reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.

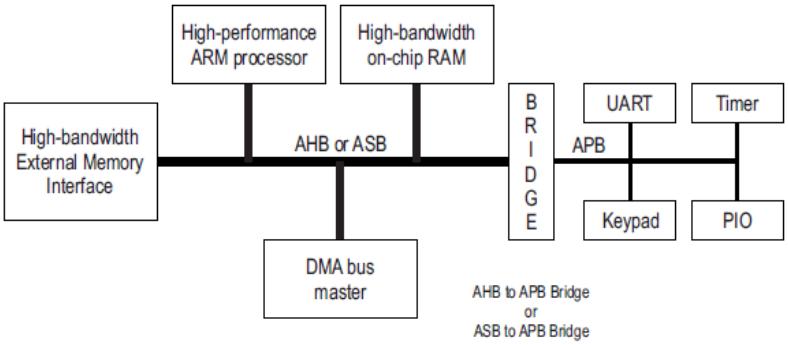

Figure 1 A Typical AMBA System.

II. Amba Apb Bridge

The APB is part of the AMBA protocol family. It provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface. The APB has un-pipelined protocol. All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow.

2.1 CLOCK SKEW: Clock is a signal used for synchronization when the data passes through the storage elements like flip-flops and latches. But, unnecessary switching activities of clocks may cause a huge amount of power dissipation around 15% to 50%. Clock skew is introduced when the difference is generated between the arrival times of clock Signal. Differences in clock signal arrival times across the chip are called clock skew. It is a basic design standard that timing must satisfy register setup and hold-time requirements. Clocking sequentially-adjacent registers on the same edge of a high-skew clock can potentially cause timing violations or even functional failures. There are various techniques which can be used to minimize the clock skew. In this paper three bit ripple counter approach is used to minimize the clock skew. An asynchronous ripple counter the output from the past stage is given as the clock for the preceding stage so that output ripples beyond each stage to reach the actual count.

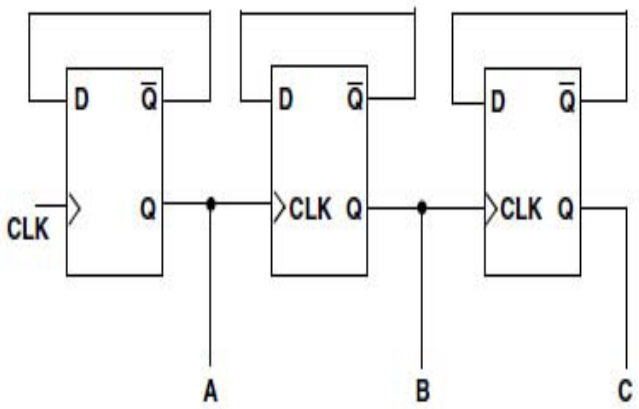

Figure 2 Three Bit Ripple Counter

III. Simulation Results

The APB Bridge is designed using FIFO and ripple counter with clock skew minimisation technique.The APB bridge has been designed, simulated synthesized by Xilinx Vivado tools and 8-bit APB bridge is implemented on Zynq Board. The timing simulations and implementation are shown in figure 3, 4,5,6,7.

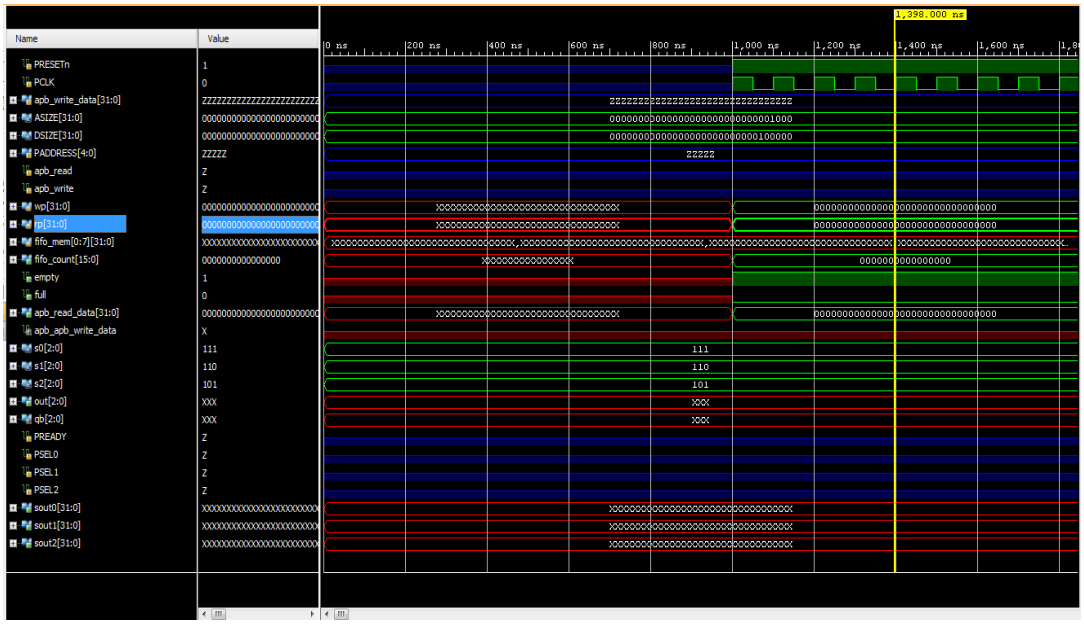

Figure 3 Simulation Result of Reset Controller

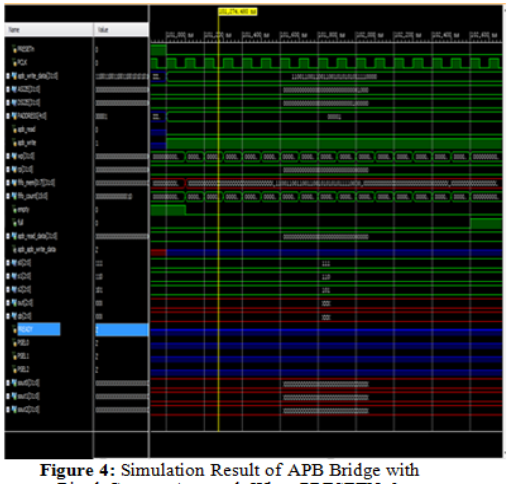

Figure 4: Simulation Result of APB Bridge with RippleCounter Approach When PRESETN=0, apb_write=1, apb_read=0, apb_write_data=11001100110011001010101011110000,PADDRESS=00001

Figure 5: Simulation Result Of APB Bridge With Ripple Counter Approach when PRESETN=0,apb_write=0,apb-read=1,apb_write_data=11001100110011001010101011110000,PADDRESS=00001,PREADY=1

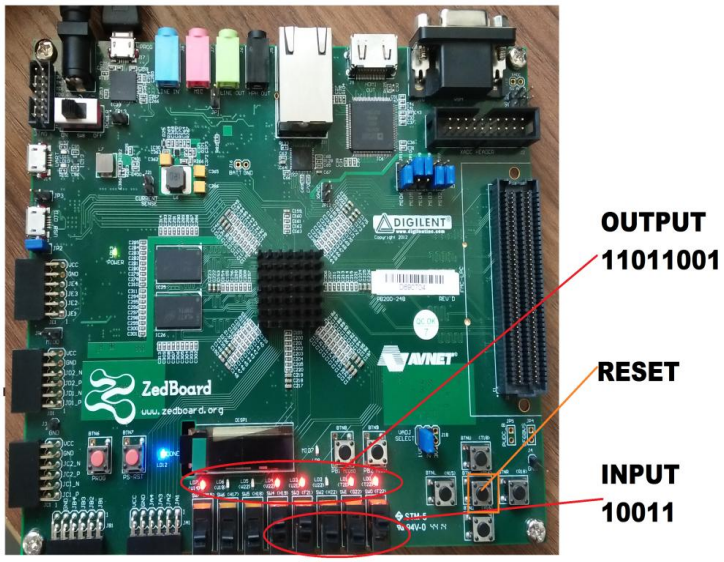

Figure 8: Implementation Of 8bit APB Bridge when PSEL0 is high.

IV. Conclusion

The implementation of AMBA APB Bridge with efficient deployment of system resources which can provide low bandwidth between AMBA high speed ASB and low speed APB buses and APB multi slave interface is designed. It defines both bus specification and a technology independent methodology for designing, implementing and testing customized high-integration embedded interfaces. The objective of the paper is achieved when bridge is designed with three bit ripple counter for minimizing the clock skew. In this Design the Xilinx VIVADO IDE Tool is used for synthesis and simulation and verified the APB Bridge with one master and two slaves. This design supports APB protocol 32 or 64 bit data width.

References

[1] AMBA Specifications 2.0, Copyright ARM Limited 1999.
[2] KiranRawat, KanikaSahni, SujataPandey, "Design of AMBA APB Bridge with Reset Controller for Efficient Power Consumption", 9th IEEE International Conference on Industrial and Information System (ICIIS2014), Indian Institute of Information Technology and Management, Gwalior, 15-17 December 2014.
[3] KiranRawat, KanikaSahni, SujataPandey,Ziauddin Ahmad "A Novel Low Power Design Approach To Exploit The Power Usage Of AMBA APB Bridge "in 1st International Conference on Recent cognizance in wireless communication & image processing – ICRCWIP-2014, Springer Publication, Jaipur , 16-17 Jan 2015.
[4] KiranRawat, KanikaSahni, SujataPandey, "RTL Implementation for AMBA ASB APB Protocol at System on Chip Level "in 2nd International Conference on Signal Processing & Integrated Networks", SPIN 2015, Amity University, Noida, 19-20 Feb 2015.

[5] Amit Kumar, Shankar, Neeraj Sharma," Verification of Asynchronous FIFO using System Verilog" International Journal of Computer Applications (0975 – 8887), Volume 86 – No 11, January 2014.
[6] Vani.R.M, M.Roopa," Design of AMBA Based AHB2APB Bridge" IJCSNS International Journal of Computer Science and Network Security, VOL.10 No.11, November 2010.
[7] Santhi PriyaSarekokku, K.Rajasekhar," Design And Implementation Of APB Bridge Based On AMBA AXI 4.0" International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 9, November- 2012.
[8] AMBA® APB Protocol Version: 2.0 Specifications.
[9] Heli Shah, R Chinmay Modi, BhargavTarpara," Design & Implementation of Advance Peripheral Bus Protocol" International Journal of Scientific Engineering and Applied Science (IJSEAS) - Volume-1, Issue-3, June 2015 ISSN: 2395-3470.