IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 7, Issue 3, Ver. I (May. - June. 2017), PP 27-34
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design And Implementation Of Arithmetic Logic Unit Using Modified Quasi Static Energy Recovery Adiabatic Logic

M.L.Keote[1], P.T.Karule [2]
[1]*Department of Electronics and Telecommunication Engg. Yeshwantrao Chavan College of Engg., Nagpur, Maharashtra, India*
[2]*Department of Electronics Engg, Yeshwantrao Chavan College of Engg, Nagpur, Maharashtra, India*

Abstract**:** *This paper presents implementation of Arithmetic Logic Unit as it is fundamental building block of various computing circuits. 4 bit ALU is designed using Modified Quasi State Energy Recovery Logic (MQSERL) and CMOS logic. For implementing ALU, circuits which are needed are Multiplexer , Full adder and various basic gates such as Inverter ,XOR, AND and OR are designed using both logic style. Comparative power analysis has been done to validate the Proposed MQSERL logic style which gives less power dissipation compared to conventional logic. The Arithmetic and Logic Unit designed using proposed MQSERL logic is 24.14 % and 33.28% power efficient than CMOS logic . The operating voltages for all the circuits are 1.8V and simulated using 180nm tanner technology. For MQSERL circuits, two sinusoidal power clock which are 180^0 phase shifted with each other are used by maintaining frequency at 100MHz and frequency of the input signal maintained at 50 MHz.*

Keywords**:** *Low power VLSI, Quasi static energy recovery logic, Energy efficienty circuits, adiabatic computing, and Arithmetic logic unit.*

I. Introduction

In today's digital systems, the low energy operation is must. To achieve low power operations the approaches are to reduce supply voltage of circuit, loading capacitances of gates and to reduce switching activity. The alternative approach for energy reduction is Adiabatic circuits which has been examined in recent years [1-13]. Adiabatic logic works with the concept of reducing the power by giving stored energy back to the supply and this can be achieved by using an AC power supply called the power clock. Various Adiabatic logic families have been investigated which are reversible[7-8] and irreversible in nature. Reversible circuits [9-10] have control signal coming from next stage, the design complexity is considerable but irreversible circuits have higher switching activity and use of multiphase power clock make them unfavourable for design. In order to overcome the disadvantages of irreversible logic circuits ,Quasi Static Energy Recovery Logic (QSERL) has been proposed in literature [9] which resembled the static behavior and reduces the switching activity and design complexity. It utilizes two complementary sinusoidal power clocks. QSERL reduces energy dissipation. Operation of QSERL is performed in two phases Hold and Evaluate. But QSERL suffers from alternate hold phases due to which output is in floating condition which causes inrobustness. Modified quasi static energy recovery logic (MQSERL) is presented in order to eliminate the disadvantages of QSERL. The proposed logic style is a good alternative to conventional CMOS logic style. The paper presents implementation of multiplexer, full adder and basic gates using MQSERL logic style and CMOS logic style. Finally 4 bit Arithmetic unit and Logic Unit [15,18] is designed and Performance of ALU is determined using both logic style by computing power dissipation and the number of NMOS and PMOS required for its implementation . All the circuits are operated at clock frequency of 100MHz and voltage of 1.8V.

II. Modified Quasi Static Energy Recovery Logic Circuit

The Modified Quasi Static Energy Recovery Logic circuit is shown in fig 1.[9][11-12] consists of PMOS transistor which controls the charging path and NMOS transistor at bottom controls the discharging path . PMOS transistor is connected to clock signal and NMOS transistor at the bottom is connected to clock signal which is 180^0 phase shifted with upper clock signal. The proposed circuit offers less complexity in terms of wiring and design compared to Quasi Static Energy Recovery Logic (QSERL).

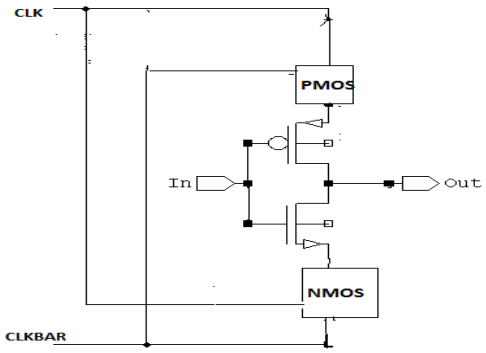


Fig 1. Structure for MQSERL

The clock signals are sinusoidal in nature as it offers less power dissipations compared to triangular and trapezoidal power clock. the sinusoidal clock charges and discharges the load capacitance slowly .The two clock signals are complementary to each other and height of clock signal is 1.8V peak to peak. The circuit operates is performed in two phases evaluation and hold. During evaluation phase clock signal goes high and complementary clock goes low while in hold phase operation clock signal goes low and complementary clock signal goes high. Capacitor is charged through pmos transistor when output is low and pmos transistor is on during evaluation period, and output logic reaches at high level. When output is high and nmos transistor is on , capacitor discharges through nmos transistor and recycling of charges takes place reaching output logic at low level. The impact of leakage is less significant due to swinging and complementary clock signal.

III. Design of Mux and Full Adder

A. Design of 4:1 Mux using MQSERL

The structure for MQSERL 4:1 Mux is shown in fig.2. A multiplexer is combinational circuit that selects several input signal and forward the selected input to output line depending on status of select line. it consists of 14 pmos transistor in charging path and 14 nmos transistor in discharging path.

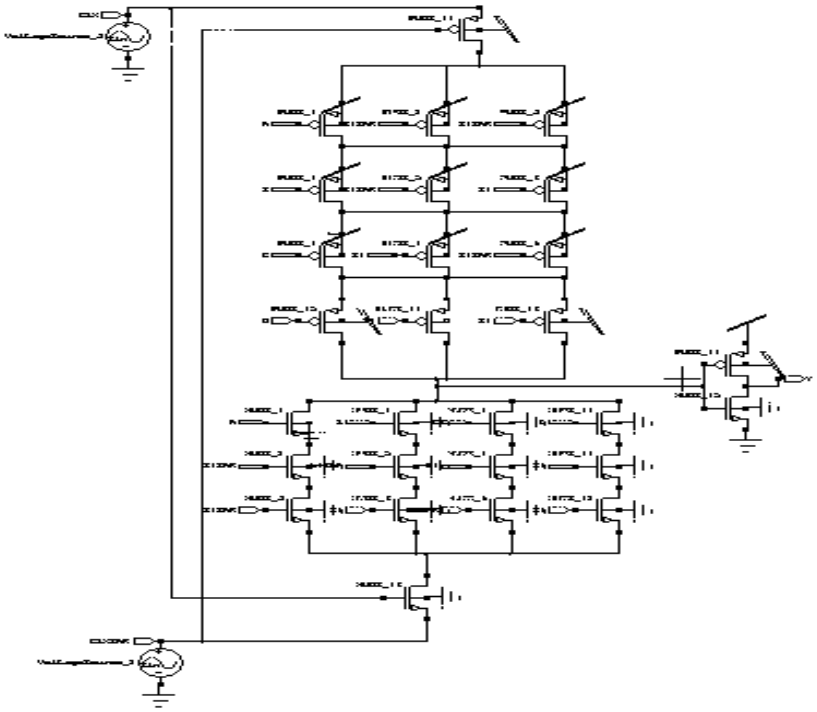


Fig 2. Design of 4:1 MQSERL MUX

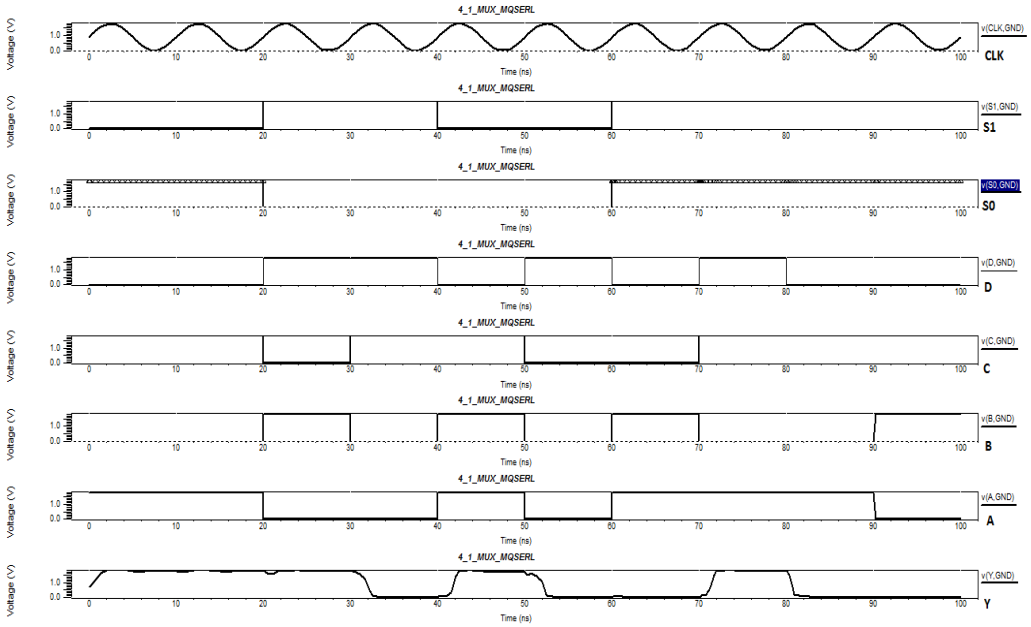


Fig.3. Simulation Waveform of 4:1 MQSERL MUX

The clock signal frequency is maintained at 100 MHz. Two clock signals are 180^0 phase shifted and offset is set at 0.9v. The circuit is simulated by setting the W/L ratio at 1. The input signal frequency is 50Mhz and logic 1 level is set at 1.8v and logic 0 at 0v. Though number of transistor required for the MQSERL Mux is more compared to CMOS Mux but 51.45% power is saved in MQSERL Mux. Comparative analysis is shown in Table I.

Table I. Comparative Analysis between CMOS and MQSERL 4:1 MUX

DEVICE	Number of Transistor required	NMOS	PMOS	Power Dissipated in uwatt
CMOS 4:1 MUX	26	13	13	5.718
MQSERL 4:1 MUX	28	14	14	2.776

B.Design of Full Adder using MQSERL

The Full Adder ciruit is designed using MQSERL logic is shown in Fig.4. An adder is a digital circuit and used in Arithmetic logic unit.There are three inputs A,B, and Cin and two outputs sum and carry.

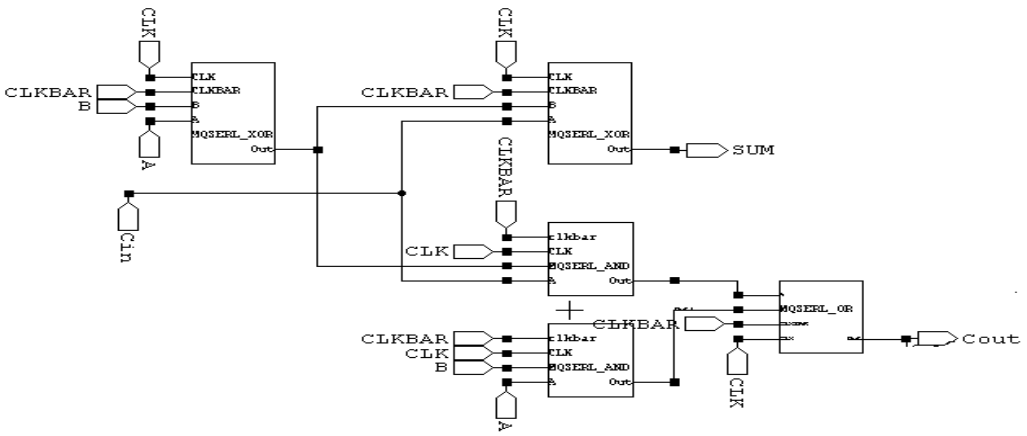


Fig.4. Design of MQSERL Full Adder

Fig. 5 Simulation Waveform of MQSERL FULL ADDER

Full adder is designed using two XOR , two AND and one OR circuit using both logic style.The Fig. 5 shows simulation waveform for Full Adder circuit. Table II gives comparative analysis. MQSERL Full Adder is 19.02% power efficient than CMOS full adder though number of transistors required for implementation is more compared to CMOS logic.

TABLE II. Comparative Analysis between CMOS and MQSERL Full Adder

DEVICE	Number of Transistor required	NMOS	PMOS	Power Dissipated in uwatt
CMOS Full Adder	38	19	19	61.88
MQSERL Full Adder	44	22	22	50.11

IV. Design of 4 Bit ALU

The Arithmetic Logic Unit is a digital circuit used to perform arithmetic and logic operations. It represents fundamental building block of central processing unit. Truth table for 4 BIT ALU is shown in table III. A 2:1 multiplexer is used to select the arithmetic and logic operation. When M=0, Logic operations are performed and for M=1, arithmetic operations are performed.

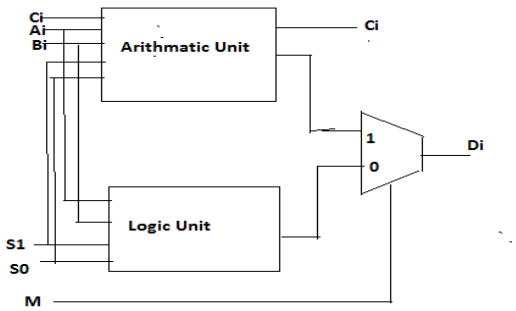


Fig.6.Design of 4 Bit ALU

TABLE III. ALU Truth Table

M=0 Logic Operations				
S0	S1	Cin	OPERATION	FUNCTION
0	0	X	$\overline{A}$	Invert A
0	1	X	$A \oplus B$	Exor
1	0	X	A+B	OR
1	1	X	A.B	AND
M=1 Arithmatic Operations				
S0	S1	Cin	OPERATION	FUNCTION
0	0	0	$A+\overline{B}$	A plus one's complement of B
0	0	1	$A+\overline{B}+1$	Subtraction
0	1	0	A+B	Addition of A and B
0	1	1	A+B+1	Increment Addition of A and B by 1
1	0	0	A-1	Decrement A
1	0	1	A+B+1	Increment Addition of A and B by 1
1	1	0	A	Transfer A
1	1	1	A+1	Increment A by 1

A. Mqserl Logic Circuit

The logic circuit performs the basic logic micro operations such as NOT, OR, AND and XOR. From these four micro operations all known logic micro operations can be derived. Figure 7 shows the logic diagram for one stage of logic circuit. The four gates generate the four logic operations and the multiplexer select the desired operation as shown in Fig.9.

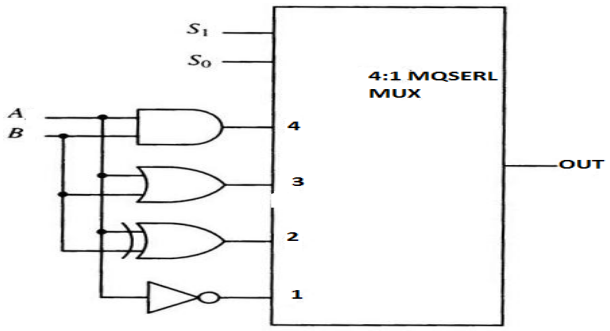
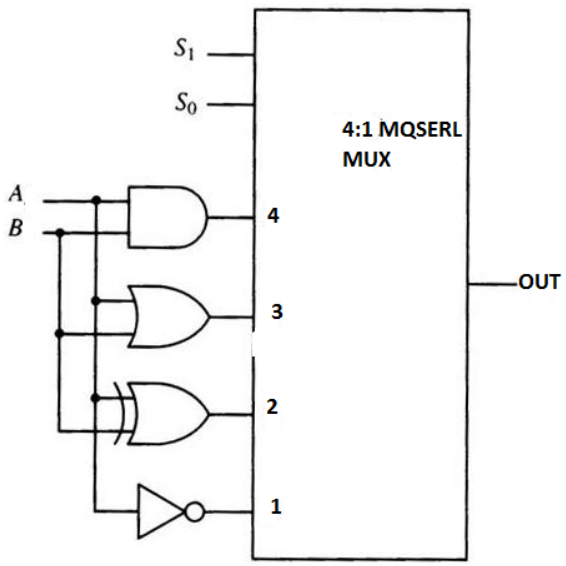


Fig.7. Design of Logic Unit



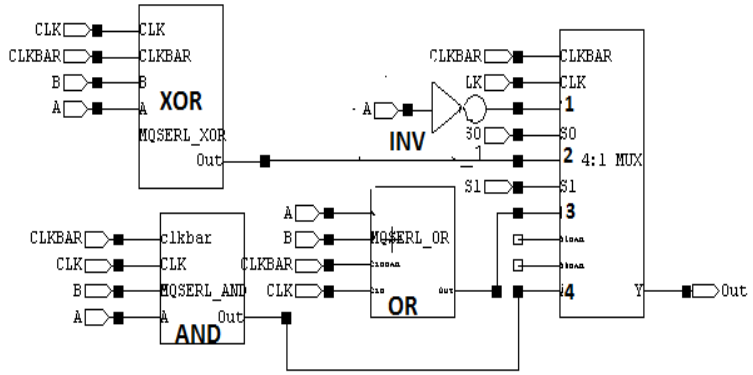


Fig.8. Design of MQSERL LOGIC UNIT

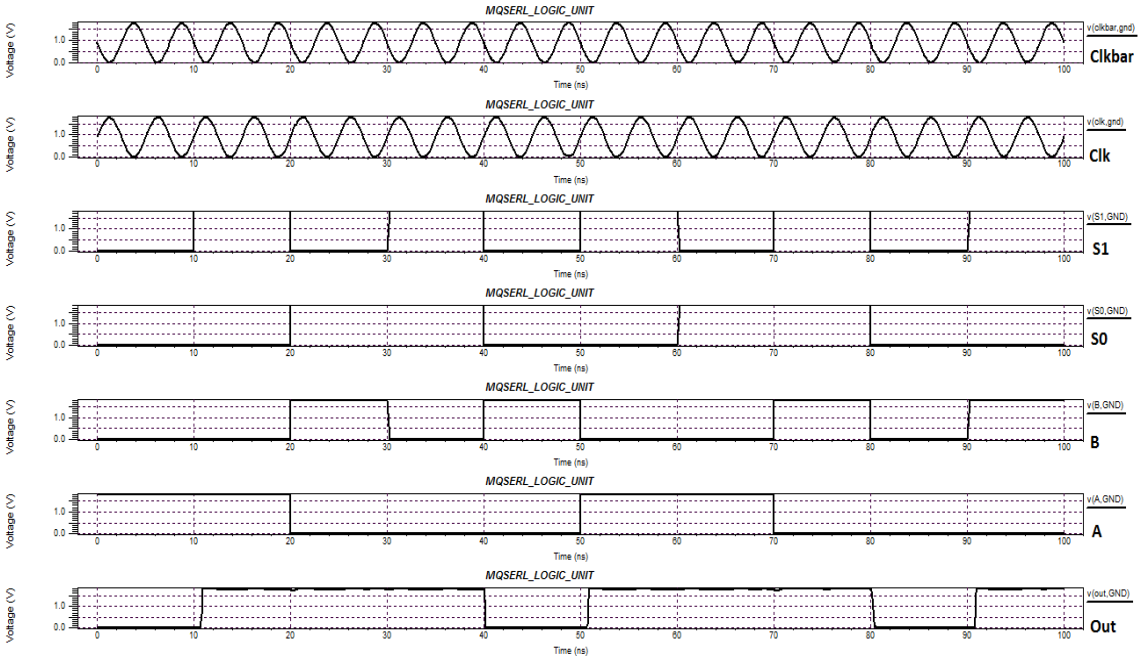


Fig.9. Simulation Waveform for MQSERL LOGIC UNIT

TABLE IV. Comparative Analysis between CMOS and MQSERL Logic Unit

DEVICE	Number of Transistor required	NMOS	PMOS	Power Dissipated in uwatt
CMOS LOGIC UNIT	50	25	25	38.45
MQSERL LOGIC UNIT	58	29	29	25.65

B. MQSERL Arithmatic Unit

The arithmetic circuit performs typical arithmetic operations such as addition, subtraction and increment or decrement by one and transfer .The basic component of an arithmetic circuit is the Full adder. By using a multiplexer to control the data inputs to the adder, it is possible to obtain different types of arithmetic operations. The circuit diagram for 4-bit arithmetic is shown in Figure 10.

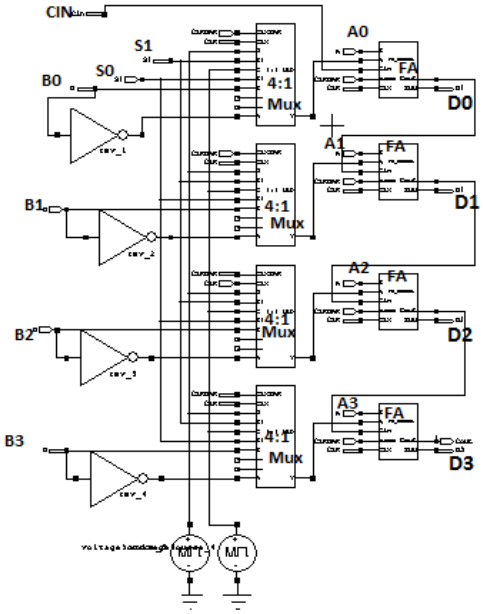


Fig.10. Design of MQSERL Arithmatic Unit

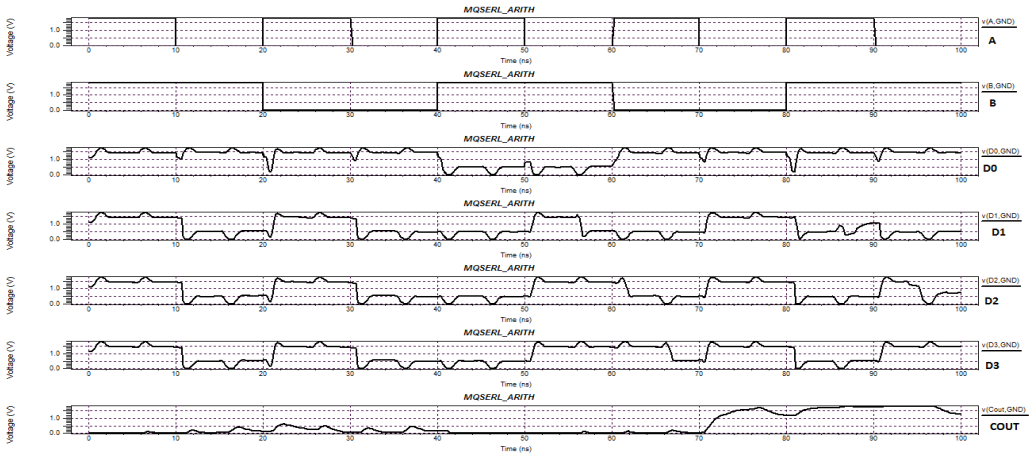


Fig.11. Simulation Waveform of MQSERL Arithmetic Unit

TABLE V. Comparative Analysis between CMOS and MQSERL Arithmetic unit

DEVICE	Number of Transistor required	NMOS	PMOS	Power Dissipated in uwatt
CMOS ARITHMETIC UNIT	266	133	133	283.69
MQSERL ARITHMETIC UNIT	308	154	154	215.18

V. Experimental Results

Power dissipation analysis of two logic styles i.e. CMOS logic and MQSERL logic for various digital circuits are summarized in the table below. The W/L ratio was set at 1 and circuits are simulated using 180nm technology file.The operating voltage was 1.8V and complementary sinusoidal power clock of 100Mhz and input signal frequency of 50Mhz are used for all circuits.

TABLE VI.. Power Dissipation Analysis

DESIGN	**Power Dissipated in uwatt**	
	CMOS	***MQSERL***
4:1 Mux	5.718	2.776
Full Adder	61.88	50.11
Logic unit	38.45	25.65
Arithmetic Unit	283.69	215.18

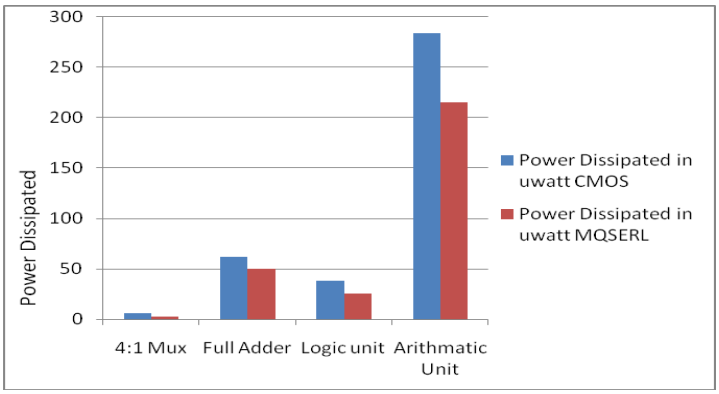


Fig.12. Comparative Power Analysis.

VI. Conclusion

The comparative analysis and results indicates that the proposed Modified Quasi Static Energy Recovery Logic (MQSERL) is better approach for design of digital circuits than CMOS circuits. The design of Arithmetic Unit using the proposed logic is 24.14% and Logic unit is 33.28 % efficient compared with CMOS logic. While comparing the designs of two logic styles, the same environment is maintained such as clock frequency, input signal frequency to compute power dissipation.

References

[1] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou, "Low-Power Digital Systems Based on Adiabatic-Switching Principles," IEEE Trans. VLSI Systems, 2(4), 398-407, Dec. 1994

[2] W. C. Athas, L. "J.". Svensson, J. G. Koller, N. Tzartzanis, and E.Chou,"A framework for practical low-power digital CMOS systems using adiabatic-switching principles," in Proc. Int.Workshop Low Power Design,Napa Valley, CA, 1994, pp. 189–194.

[3] J. S. Denker, "A review of adiabatic computing," in Proc. 1994 Symp.Low Power Electronics, San Diego, CA, Oct. 1994.

[4] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," IEEE J.Solid-State Circuits, vol. 30, pp. 311–315, Mar. 1995.

[5] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit,"IEEE J. SolidState Circuits, vol. 31, pp. 514–522, Apr. 1996

[6] Y. Takahashi, T. Sekine, and M. Yokoyama, .Two-phase clocked CMOS adiabatic logic,. in Proc. IEEE Asiapacifiic Conf. Circuits and Systems, Macao, China, Nov.359

[7] Y. Ye, K. Roy, Energy recovery circuits using reversible and partially reversible logic. IEEE. Trans.Circuit Syst. **43**(9), 769–778 (1996)

[8] J. Lim, D. G. Kim, and S. I. Chae, "A 16-bit carry-look ahead adder using reversible energy recovery logic for ultra-low-energy systems, IEEE J. Solid-State Circuits, vol. 34, no. 6, pp. 898–903, Jun. 1999

[9] Y. Ye and K. Roy, "QSERL: quasi-static energy recovery logic," IEEE J. Solid-State Circuits, vol. 36, no. 2, pp. 239–248, Feb. 2001

[10] Cihun-siyong Alex Gong, Muh- Tihan Shiue, Ci-Tong Hong, And Kai- Wen Yao, (2008),"Analysis and Design of an Efficient Irreversible Energy Recovery Logic in 0.18-μm CMOS", IEEE Transaction on Circuits and Systems, Vol. 55, No. 9, pp. 2595-2607.

[11] Shipra Upadhyay, R. K. Nagaria, and R. A.Mishra "Low-Power Adiabatic Computing with Improved Quasi static Energy Recovery Logic " Hindawi Publishing Corporation VLSI Design Volume 2013, Article ID 726324, 9 pages .

[12] M.L.Keote,P.T.Karule, "Modified Quasi Static Energy Recovery Adiabatic Logic Implementation for Low Power Application" Int. Conference on Advances in computing, communication and Automation (fall) ICACCA ,Bareilly India 978-1-5090-3480-2/16/$31.00 ©2016 IEEE

[13] Wang Pengjun and Yu Junjun, (2007),"Design of Two-Phase sinusoidal Power Clock and ClockedTransmission Gate Adiabatic logic Circuit", Journal of Electronics (China), Vol. 24, No. 2,pp. 225-231.

[14] S. Kim and M. C. Papaefthymiou, "True single-phase energy-recovering logic for low-power, high-speed VLSI," in Proc. Int. Symp. Low-Power Electronics and Design, Monterey, CA, Aug. 1998, pp. 167–172.

[15] M. C. Knapp, P. J. Kindlmann, and M. C. Papaefthymiou, "Implementingand evaluating adiabatic arithmetic units," in IEEE Custom Integrated Circuits Conf., San Diego, CA, 1996, pp. 115–118

[16] Mehrdad Khatir, Alireza Ejlali, Amir Moradi, (2011),"Improving The energy Efficiency of Reversible Logic Circuits by The Combined Use of Adiabatic Styles", Integration the VLSI Journal, Elsevier, Vol. 44, pp. 12-21.

[17] Wang Pengjun and Yu Junjun, (2007),"Design of Two-Phase sinusoidal Power Clock and ClockedTransmission Gate Adiabatic logic Circuit", Journal of Electronics (China), Vol. 24, No. 2,pp. 225-231.

[18] Sriraj Dheeraj Turaga, Kundan Vanama, Rithwik Reddy Gunnuthula , K.Jaya Datta Sai " Design of Low Power 4-bit ALU Using Adiabatic Logic" IOSR

[19] Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 2, Ver. I (Mar-Apr. 2014), PP 43-48 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197