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Design and Implementation of a Low Noise Amplifier for Ultra Wideband Applications

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Abstract: *This paper represents the design and implementation of Low Noise Amplifier for Ultra wideband application using 0.18μm CMOS Technology. The proposed two stage LNA is for a 3-5 GHz. At supply voltage of 1.8V, for the exceed limit of 50μm of width of each transistor, the power consumption is 7.22mW. Noise figure is 4.33dB, Maximum power gain i.e. S21 is 20.4dB, S12 < -20dB, S11 < -8dB, S22 < -10dB. For the required bandwidth range, LNA is unconditionally stable and have good linearity.*

Keywords: *LNA, Biasing circuit, Input and Output matching, Power Consumption, Noise Figure, Gain, Stability.*

I. Introduction

The LNA functions in the world of unknowns. As the front end of the receiver channel, it must capture and amplify a very low-power, low voltage signal plus associated random noise which the antenna presents to it, within the bandwidth of interest. The range of band of frequencies is 3.1GHz to 10.6GHz [1]. For LNA, Noise figure, Gain, Power Consumption and Linearity are the primary parameters. Noise limits the minimum signal level that a circuit can process with acceptable quality[2]. Today's analog designers constantly deal with the problem of noise because it trades with power dissipation, speed and linearity[2]. The published literature says minimum noise figure and maximum gain can't be achieved at the same time. So we need optimum value of Noise Figure and Gain. For higher gain, the signal strength gets stronger and stronger & signal to noise ratio also gets better. Maximum gain will eventually affect Noise figure. Normally the gain of 1st stage is high enough to suppress the effect of 2nd stage in the total noise figure[3]. However, Noise and Power matching becomes possible in CMOS Technology[3]. It is always better to have a low power consumption circuit because it greatly affects the cost of the circuit or system. Inductive degeneration improves the linearity of the circuit. The biasing circuit has been introduced in the design connected to the first stage. Biasing circuit is important to obtain consistent circuit performance[4]. With the help of this, noise figure reduces and we get the satisfied output gain. One excellent way of biasing the MOSFET is to have a constant gate voltage and average source resistance[4]. This work represents the design of two stage circuit of LNA introducing the biasing circuit trying to achieve all the required parameters simultaneously.

II. Design of The Circuit

Designing of RF circuits is a challenging job, since even after performing lengthy calculations and finding parameter values it is less guarantee that the design performs as expected[5]. The proposed LNA design has been implemented on Cadence tool with 180nm CMOS technology. The LNA has a limitation of exceed limit of width of each transistor as 50μm for a minimum value of 0.18μm length in order to achieve maximum gain with the minimum noise figure and Power Consumption. For RF_in 50Ω and RF_out 50Ω, mathematically we will find the following parameters,
Calculation of Gate Oxide Capacitance is as follows,

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \qquad [6]$$

Where $\epsilon_{ox} = \epsilon_0 \times \epsilon_r$
$\epsilon_0 = 8.854 \times 10^{-12}\ F/m$
$\epsilon_r = 3.9$
t_{ox} = thickness of gate oxide

Then ,

$$C_{ox} = 8.42 \times 10^{-3}\ F/m^2$$

Now Optimum Width of a Transistor is

$$W = \frac{1}{3 \times C_{ox} \times \omega \times L} \qquad [6]$$

$$\omega = 2\pi f_2 - 2\pi f_1$$

Where $f_1 = 3 \times 10^9$ & $f_2 = 5 \times 10^9$

Therefore , $\omega = 2\pi \times 2 \times 10^9$ and $L = 180nm$, $R_s = 50\Omega$

Hence , $W \approx 350\mu m$

Gate Source Capacitance can be calculated as

$$C_{gs} = \frac{2 \times W \times C_{ox} \times L}{3} \qquad [6]$$

$$= 353fF$$

Source Inductor L_s is

$$\frac{g_m \times L_s}{C_{gs}} = 50\Omega \qquad [6]$$

Assuming the drain current Id of 5mA for the required application, the transconductance of the system can be calculated as

$gm = Id \times Vdsat$

Where $Vdsat$=200mV as per the rule of thumb in the analog design. But we will consider $Vdsat$ = 100mV and hence we get gm = 50mS.

Therefore , Ls = 882pH

and Lg is

$$f = \frac{1}{2\pi \times \sqrt{(L_s + L_g) \times C_{gs}}} \qquad [6]$$

And we get $L_g = 7nH$

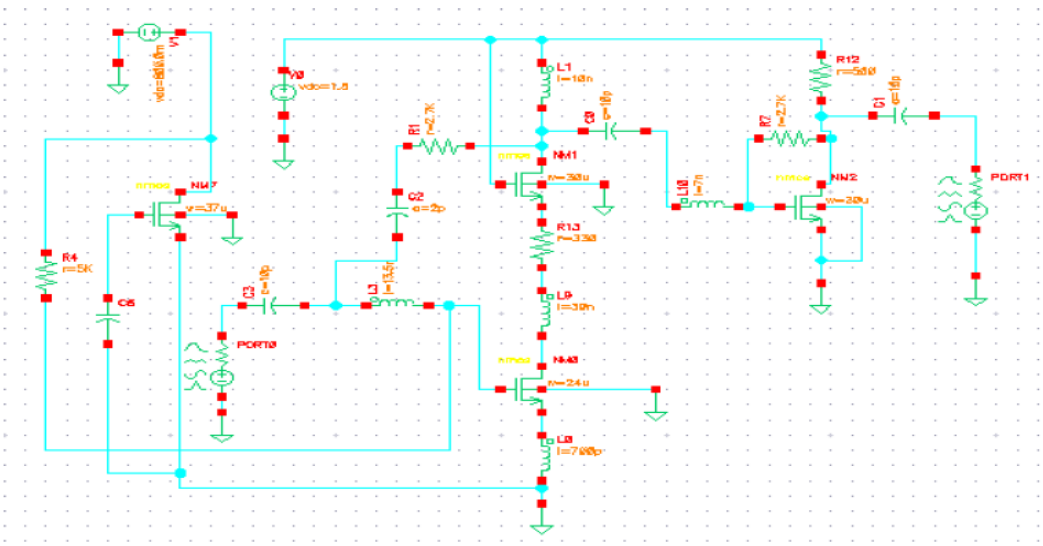
Noise figure (NF) can be calculated as

$$NF = 10log_{10}\left(1 + \frac{RF\_out}{RF\_in}\right)$$

And $NF = 3dB$

Analysis of the Circuit in Cadence:

The proposed design has been simulated with 0.18µm CMOS technology in Cadence. All the transistors are in saturation region.

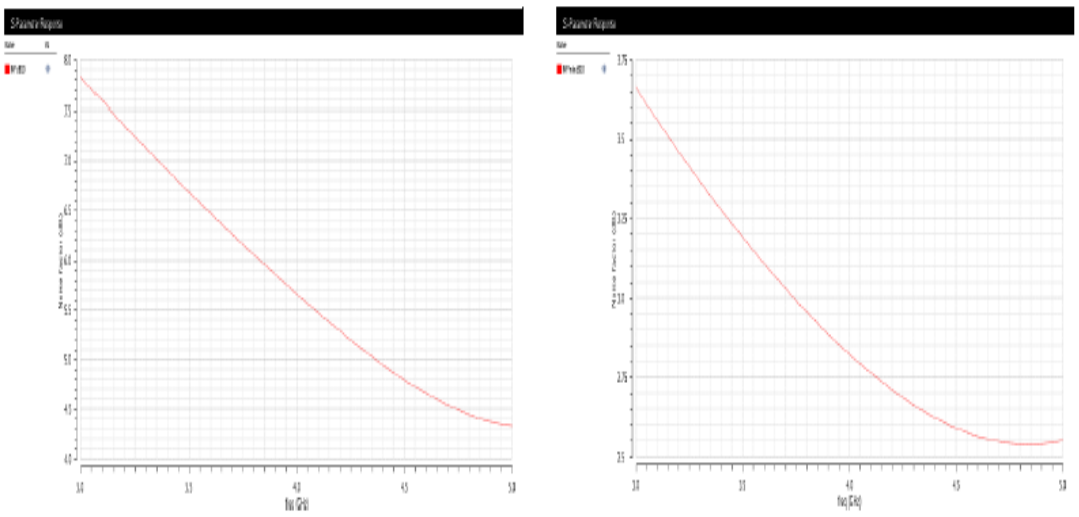


The LNA consist of two stages. The first stage is a cascade topology. Cascade topology promises higher power gain, good noise performance, low power consumption. The topology has superior noise performance using feedback technique and it is possible to use this in wideband applications [2]. The R-C feedback has been used in the first stage, it helps to improve the gain and it has very good wideband input matching characteristics. The feedback circuit of this topology has a value of resistor as $2.7K\Omega$ and Capacitor value as $2pF$. The value of Lg and Ls is $13.5nH$ & $700pH$ respectively. The width of transistor $NM0$ is $24\mu m$ while the width of $NM1$ is $30\mu m$. The value of inductor Lin placed between two transistors $NM0$ and $NM1$ of first stage is $30nH$. This is also called as source degenerative cascade topology. The introduction of this interstage inductor enhances the gain of cascade LNA [6]. Thus Lin serves as inter-stage matching between drain of $NM0$ and source of $NM1$. The inter-stage LNA can provide more gain and less miller effect. It also helps to improve the output matching. The presence of Lin improves the Noise figure. This improvement is more pronounced if the inter-stage matching inductor is off chip thus avoiding large parasitic capacitance [6]. This improves the stability also in the proposed circuit. Capacitors at input and output are DC blocking capacitors [1] having the value of 10pF. The resistor placed in series with the Lin helps to improve the scattering matrix parameters.

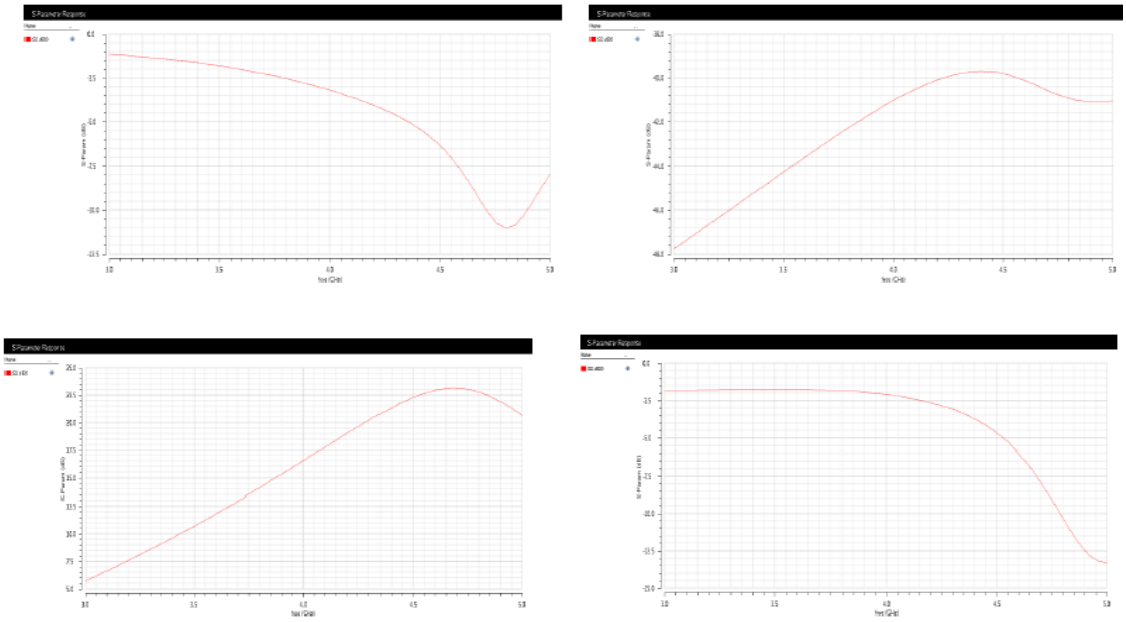
The resistive feedback in the second stage helps to maintain the positive gain. The first stage has shunt peaking inductor consisting of value $12nH$ and the second stage has a shunt resistor of value 500Ω. It helps to reduce the chip area, to obtain proper gain and also reduces the Noise figure. Because of shunt peaking technique, the low power consumption and low noise figure can be achieved simultaneously [7]. The internal resistance of all the passive components is 0, although it hardly affects gain but it reduces noise figure to some extent. The biasing circuit is introduced in the proposed circuit. Out of three biasing schemes, we have used constant voltage bias which is most useful for Radio Frequency (RF) and video amplifiers employing small DC drain resistors [2]. Biasing circuit is important to maintain the consistency in the circuit. It also helps to reduce the Noise Figure. Here the bias voltage is of $0.8V$. The value of $Rbias$ in the biasing circuit is chosen to be large to minimize the noise entering into the design [5]. The value of $Rbias$ is $5K\Omega$ in the circuit.

III. Simulation

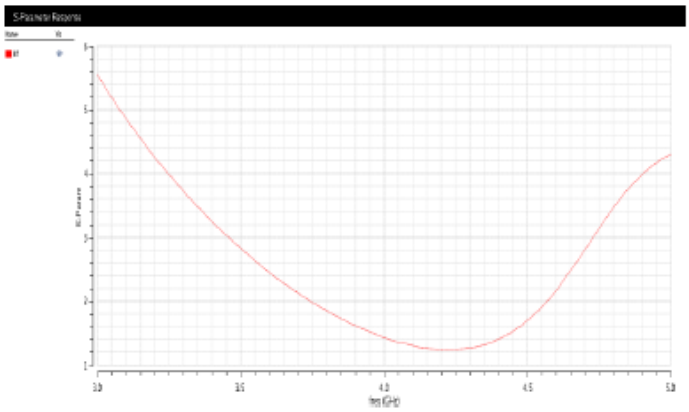
1. **Noise analysis –** The resultant noise figure and minimum noise figure of a designed LNA is 4.3dB and 2.6dB respectively. Here the improvement is, even after second stage, the Noise figure is continues to reduce.



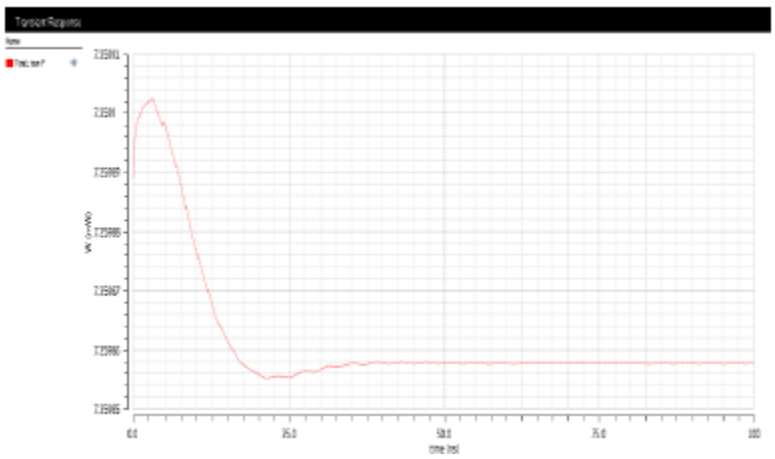
2. S–Parameter analysis – The simulated results shows that the LNA has maximum gain of 20.4dB. Also the gain is continuously increasing even after the second stage. Reverse gain coefficient is less than -30dB and Input reflection coefficient is less than -8dB. Also the output reflection coefficient is improved to -13.5dB and this provides a very good output matching.



3. **Stability analysis –** As the reverse isolation increases , stability improves. And in the previous analysis it is proved that reverse isolation is up to -40dB. One can use the techniques such as resistive loading and neutralization to improve stability for an LNA. Stability analysis shows that $Kf > 1$ across 3-5GHz band of frequencies stating that the designed LNA is un-conditionally stable.



4. **Power Consumption –** The power consumed in the circuit is 7.22mW. By improving the scattering matrix parameters, power consumption can be reduced.



Comparison :

PARAMETER	THEOROTICAL	PROPOSED WORK
Frequency	3-5GHz	3-5GHz
Supply Voltage	1.8V	1.8V
Ls	882pH	700pH
Lg	7nH	13.5nH
Power Consumption	<50mW	7.22mW
Noise Figure	<=3dB	4.3dB
Power Gain	>10dB	20.40dB
W/L ratio	350µm/0.18µm	24µm/0.18µm
Stability	$K_f > 1$	$K_f > 1$

IV. Conclusion

The LNA has been designed in 0.18µm CMOS Technology with the supply voltage of 1.8V. In the proposed design, the biasing circuit has been introduced which helps to perform the circuit consistently and to reduce the Noise. Also the inter-stage inductor has been added. In spite of limitation of maximum width of each transistor, the objective is achieved. A comparison between the present results and the results of previously reported LNA shows that Continuous reduction of Noise figure and increasing gain even after the second stage is the improvement in the circuit.

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