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Design and Power Measurement of 2 And 8 Point FFT Using Radix-2 Algorithm for FPGA Implementation

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Abstract: *In Cooley–Tukey algorithm the Radix-2 decimation-in-time Fast Fourier Transform is the easiest form. The Fast Fourier Transform is the mostly used in digital signal processing algorithms. Discrete Fourier Transform (DFT) is computing by the FFT. DFT is used to convert a time domain signal into its frequency spectrum domain. FFT algorithms uses many applications for example, OFDM, Noise reduction, Digital audio broadcasting, Digital video broadcasting. It's used to design butterflies for different point FFT. In this paper given to design and power measurement 2 and 8 point FFT by using VHDL. Simulation and synthesis of design is done using Xilinx ISE 14.2.*

Keywords: *Fast Fourier transform (FFT), Discrete Fourier transform (DFT), DIT, Radix-2, VHDL, FPGA.*

I. Introduction

Now a day field of digital signal processing is very important of transmission, there is a many growths in FFT algorithms which is way in designing a system. In this paper explains the implementation and simulation of 2and 8-point FFT using radix- 2 algorithm. Due to radix-2, FFT can achieve less time delay, beat down the area complication and, also reach cost dominant execution with minimum grow up time .

Fast Fourier Transform is an algorithm to compute Discrete Fourier Transform (DFT). DFT is used to convert a time domain signal into its frequency spectrum domain. DFT is computational tool that play a very determining role in many digital signal processing applications. The main importance of DFT in practical applications is due to a large extent on existences of computationally efficient algorithms, known as Fast Fourier Transform (FFT) algorithms, for counting the DFT. There are numerous isolated FFT algorithms implicating a large spectrum of calculated from effortless complicated calculation arithmetic to set theory and calculation theory. FFTs are algorithms for speedy calculated of discrete. Fourier transform of a information vector. The FFT is a DFT algorithm which decrease the count of calculations necessity for N point from $O(N^2)$ to O(N log N) everywhere log is the base-2 logarithm .

$$f_j = \sum_{k=0}^{n-1} x_k e^{-(2\pi i/n)jk} \qquad j = 0, \ldots, n-1.$$

In FPGA calculation there are two types of power

- Static Power- In static power spending the utilize of strength is minimum to keep the accelerator in power-up state.
- Dynamic Power- Dynamic power consumption is based on its switching activity.

II. Field Programmable Gate Arrays

From long period of time FPGAs architecture is used by the users. It have potential to mapped various applications on system. Figure 2.1 is basic FPGAs structure. It shows that FPGAs use fine grained technique to develop applications. FPGAs contain SRAM based memory which makes the system flexible. FPGA is very popular because of its flexibility.

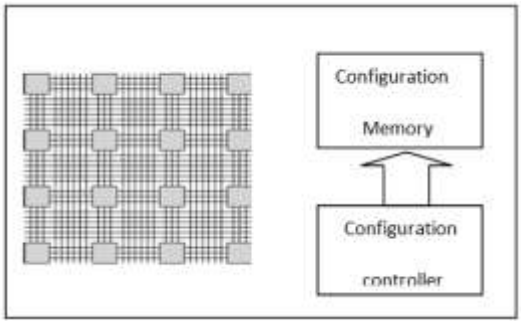


Fig.2.1: Basic architecture of FPGAs

III. Radix-2 Fast Fourier Transform Algorithm

Radix-2 algorithms are the most widely used in FFT algorithms. While counting DFT, we every time compute N-point DFT. The calculation N can be component as,

$N=r_1, r_2, r_3, \ldots\ldots\ldots r_v$ ---(a)

Here r is a prime,

Now if $r_1=r_2=r_3= \ldots\ldots r_v=r$

We can write,

$N=r^v$ ----(b)

Here r is denominated as radix (base) FFT algorithm and v is shows number of phases in FFT algorithm.

Radix denotes base and if it's value is '2' then it is said as radix-2 FFT algorithm. put the value of r=2,

$N=2^v$ ------(c)

If we are computing 2 point DFT then N=2

$2=2^v$

$V=1$

Therefore, designed for 2 point DFT, convenient are single stage of FFT Algorithm.

If we are computing two point DFT then N=8

$8=2^v$

$V=3$

Therefore, for 8 point DFT, convenient are 3 stages of FFT algorithm.

In Fast Fourier transform algorithms, a butterfly structure is a part of a calculation that jointly the outcome of compact discrete Fourier transforms (DFTs) during a massive DFT, or conversely (demolition a massive DFT above during sub transforms). The title "butterfly" move nearer from a structure of the data-flow representation in radix-2 case, as detailed beneath. The before time event in imprint of the period is idea to be in a 1969 MIT technical report. The similar formation may as well be establish in the Viterbi algorithm, utilized for locating the very similarly series of mystic states. Twiddle factor fundamentally mentioned to the root of unity difficult multiplier continual in butterfly manipulations of cooley-Tukey FFT Algorithm. Twiddle factor can as well be applied for every information free multiplier continual in FFT.

IV. Implementation of Dit-2 Point FFT Algorithm Using VHDL Code In Xilinx

In several years hardware design language has become an integral part of the industry for designing of the low level as well as high level hardware design as it is the most compatible language hence is widely used by the venders due to its functionality of being interchangeable that it can be functioned as per the users choice it widely used for the efficient synthesis of the FPGA as its supports annexation of technology precise modules .

In the below figure 4.1, find the 2 point FFT algorithm for radix-2.

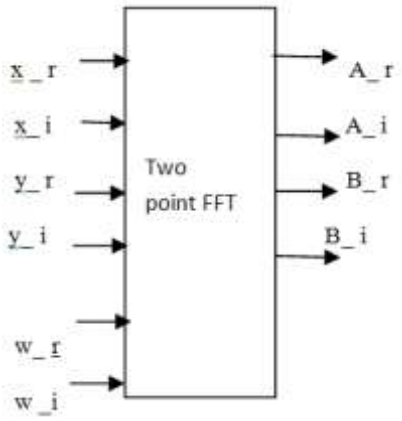


Fig.4.1: Basic block of 2 point FFT

In the above figure 4.1 shown the two point FFT algorithm. This figure has two input and one twiddle factor. x and y are the inputs, w is twiddle factor, these are imaginary and real forms. A and B are output those are also imaginary and real forms. Which Collect all the input and twiddle forms write the code in VHDL and perform the operation in Xilinx 14.2

V. Implementation of DIT 8 Point FFT Algorithm Using VHDL Code In Xilinx

In this below figure shown the block diagram of 8point FFT algorithm for radix-2

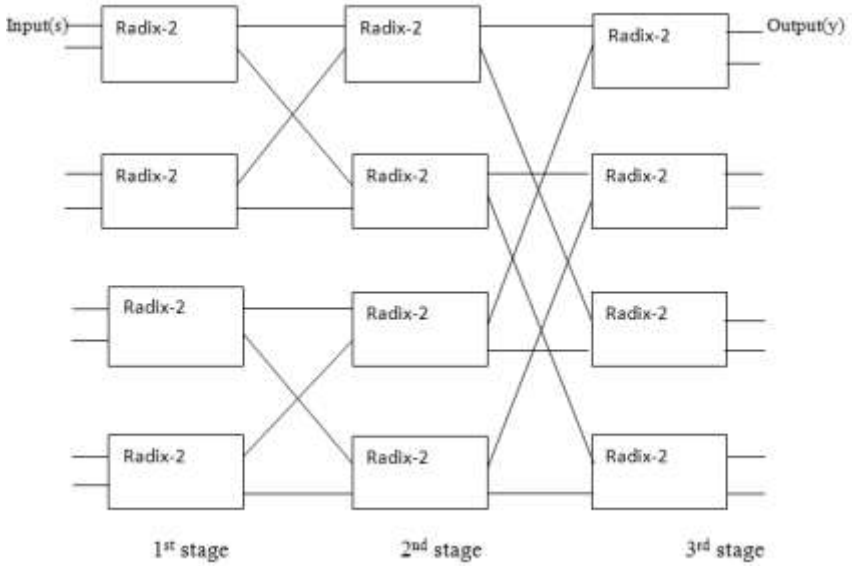
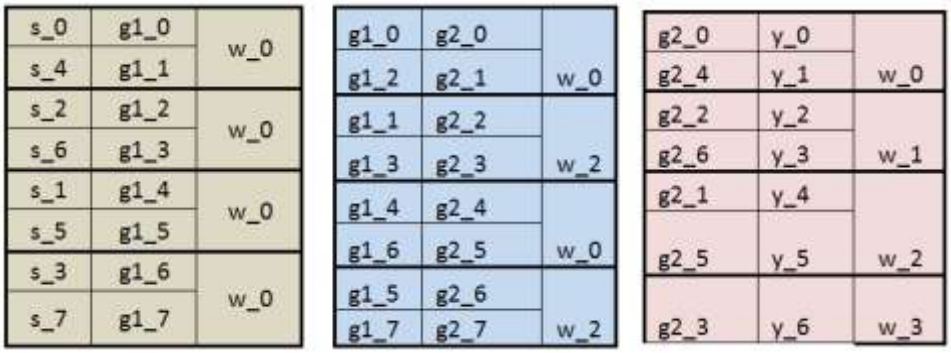


Fig.5.1: Block Diagram of 8 point FFT using 3 stage Butterfly Units



1st stage 2nd stage 3rd stage

Fig.5.2: Internal structure of 8 point FFT Butterfly units

In the above figure 5.1 shows 8 point FFT algorithm in butterfly structure. This structure have three stages. In Fig.5.2shown the internal operation of three stages 8 point FFT algorithm. Depend on internal structure write the code in VHDL and perform the operation in XILINX 14.2 tools.

VI. Simulation And Results

The RTL block thus acquired for the DIT domain by using radix-2 ,2 point FFT algorithm RTL view is shown fig.6.1 and simulation result shown in figure 6.2.

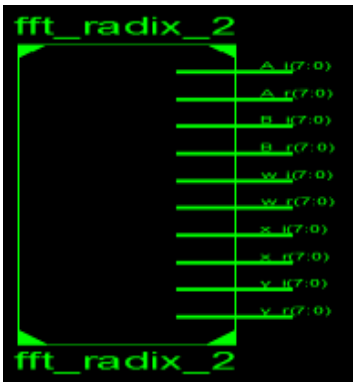


Fig.6.1: RTL View of 2 point FFT

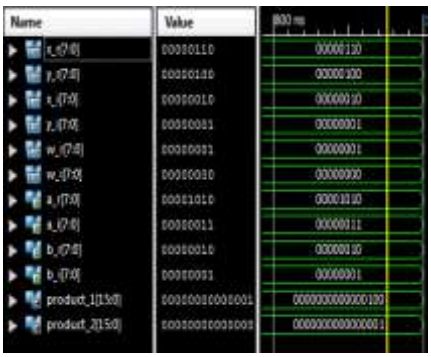


Fig.6.2: simulation result of 2 point FFT

The RTL block thus acquired for the DIT domain by using radix-2 ,8 point FFT algorithm is demonstrate fig.6.3 and Internal Architecture of 8 point FFT butterfly component shown in figure 6.4.

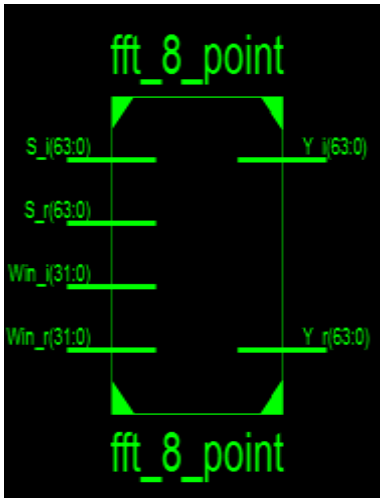


Fig.6.3: RTL View of 8 point FFT

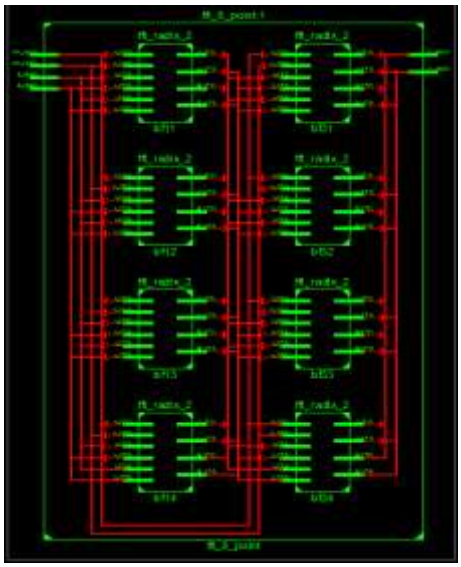


Fig.6.4: Internal Architecture of 8 point FFT

VII. Power Result

The power result shows the overall power performance of 2 and 8 point FFT algorithm. Table shows the static and dynamic power results of 2 and 8 point FFT algorithm.

FFT Length	Static Power	Dynamic Power	Total Power
2 point	0.020w	0.013w	0.033w
8 point	0.449w	0.160w	0.609w

Table: Power results of FFTS

VIII. Conclusion

In this paper we have designed 2 and 8 point FFT design using Radix-2algorithm and their simulation and synthesis are finished in VHDL using Xilinx 14.2 tool. This work demonstrate the design of 2 and 8 bit radix-2 DIT FFT is implemented in the FPGA .

The simulation of 2 bit radix-2 FFT is finished and outcome is received in Isim window. The power result of 2 bit and 8 bit radix-2 FFT are done and outcomes acquired in Xilinx XPower Analyzer, we have got two types power first static power and dynamic power.

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