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FPGA Implementation of High Speed and Low Area Four Port Network-On-Chip (NoC) Router

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Abstract: *In today's modern life high speed devices are the essential components of daily human life to reduce efforts of day to day works. For this reason those device must be able to operate at very high speed. To increase the operating speed, normally multi-core processing architecture is used. In those cases, the total task is sub-divided into multiple tasks and each processing cores are executing a particular task in parallel manner. But to calculate accurate value of the total task the individual processors must share some of the variables depending upon the task. So, bi-directional communication is necessary between all processing elements present in the multi-core system. But many issues occur in normal bus architecture to support this kind of communications. This case Network-On-Chip (NoC) router is suitable. In this paper we propose four port NoC router which can operate at high speed by consuming less area.*

Keywords: *FPGA Architecture, Matrix Switch, Network Architectures, NoC and VLSI Techniques etc.*

I. Introduction

The sophistication of the electronic devices increases rapidly due to the revolutionary development in the microchip (IC) technology. As a result, the number of IP blocks increases on the System on Chip (SoC). This increases the amount of data transferred from one IP block to another IP block present on the chip. The existing bus architectures are not able to transfer the required amount of data without reducing the device operating frequency. To overcome this problem, Network on Chip (NoC) is used for the communication between the IP blocks present on the chip. In other word, NoC is mainly used to build network interface (NI) between various IP blocks present on the chip. Normally NoC uses basic network topologies like mesh, ring, and torus etc., [1] for communication purpose.

II. Literature Surveys

Mathew and Mugilan [2] proposed reconfigurable router architecture by using heterogeneous router architecture. The proposed router can change the buffer length dynamically. It uses the multiplexers to reduce the power consumption. But this requires large area and hardware resources. Nasim Nasirian and Magdy Bayoumi [3] proposed power efficient adaptive routing algorithm. The algorithm directs the traffics in the network with respect to the routers status. This reduces static power consumption and average delay of the circuit. But this also increases the area and cell leakage power. Shaoteng Liu et al., [4] combine circuit switching and packet switching techniques. The proposed technique gives high throughput and low latency. But this requires large setup time. Somashekhar and Rekha [5] proposed ten port router using crossbar switch. This reduces power consumption and delay. But the architecture uses arbiter which increase area requirement. Paria and Reza [6] proposed Reconfigurable NoC router by replacing few routers by five port switches constructed by standard SRAM cells. This architecture reduces delay, power consumption and increase throughput of the circuit at the cost of area overhead. Suraj et al., [7] proposed dual crossbar NoC router architecture. This decrease device utilization at the cost of device latency.Giuseppe Ascia et al., [8] proposed Neighbors-an-Path adaptive routing algorithm. The algorithm uses immediate neighbor's congestion level for adaptive routing. The algorithm uses less area. Maurizio Palesi et al., [9] proposed application specific routing algorithm (APSRA). The algorithm is designed specifically for a set of applications to maximize adaptivity and performance. M. Plalesi et al., [10] proposed distribute traffic algorithm for NoC. Rodrigo et al.,[10] proposed Logic Based Distributed Routing (LBDR). The proposed technique can perform operation without routing table. Mavevich et al., [12] proposed centralized adaptive routing technique for NoC along with a specific mesh topology. This algorithm continuously monitors the traffic load and modifies the packet depending on load. Jose Flich et al., [13] classified the existing routing algorithms depending on their important properties. Martha et al., [14] propose multi-object adaptive immune algorithm (M^2AIA) to overcome the problem of mapping NoC in a large set of applications. The latency and power consumption of this algorithm depends upon the range of application considered. The efficiency of proposed algorithm is good. This algorithm is coded using C++ language. Sergio

Saponara et al., [15] propose multi-processor NoC based architecture for image/video enhancement. The architecture uses packet switched data for good communication. This structure is implemented on 65 nm CMOS technology. The structure produce high throughput and operate at 400 MHz frequency. Varginie Fresse et al., [16] propose predictive NoC architecture for image analysis using PIV algorithm. Total hardware resources in the architecture break down to many single blocks in such way that improves predictability. Also each block can be optimized separately to maximize operating frequency.

III. Proposed Architecture

The block diagram of proposed NOC router is shown in Fig. 1 which consists of four FIFO and one controller unit. The proposed block is having input and output ports in all four directions namely East, West, North and South. Depending on the control logic one of the four input data is routed to one of the four output port with some delay inserted by the FIFO. Also the FIFO's of the respective port is empty or full will be detected by empty and full port respectively. This is mainly used to avoid data collision, a problem which occurs in the communication networks.

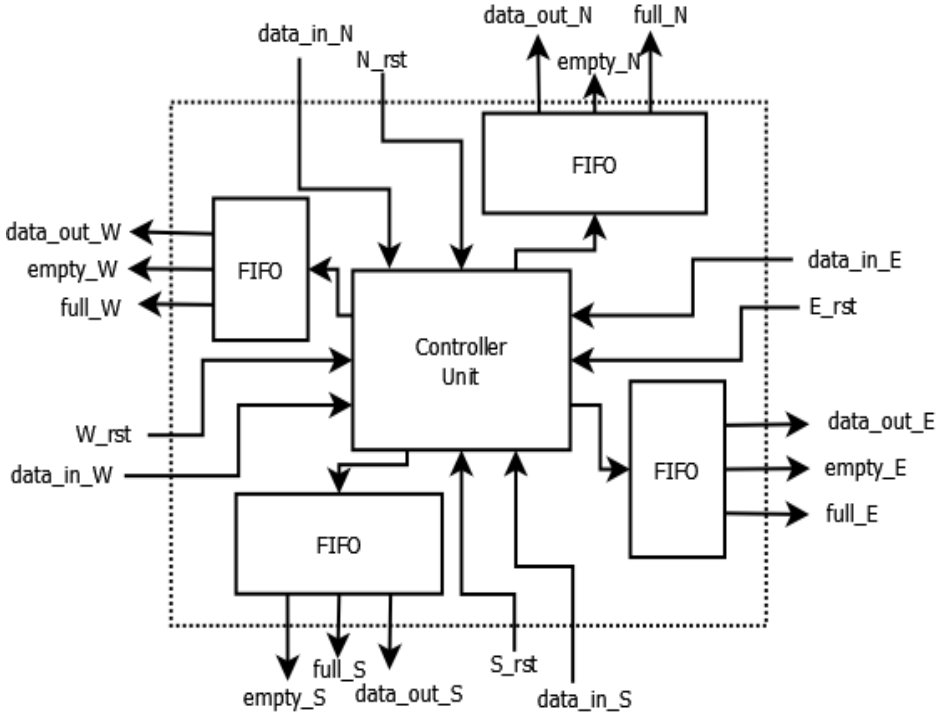

Fig.1: Proposed Block Diagram of NoC

2.1. FIFO

The block diagram of FIFO is shown in Fig. 2. The main use of the FIFO is to synchronize the input data at output side with the clock signal and hold the data packet temporarily for a predefined period.

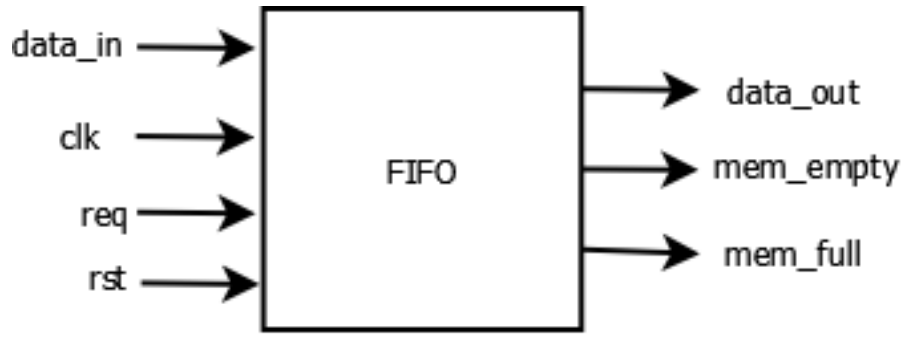

Fig.2: Block Diagram of FIFO

The internal structure of the FIFO is shown in Fig. 3. The FIFO mainly consists of three D flip-flops which are also known as FIFO depth [17]. The Counter and Decision block is used to indicate the memory conditions (i.e. full or empty).

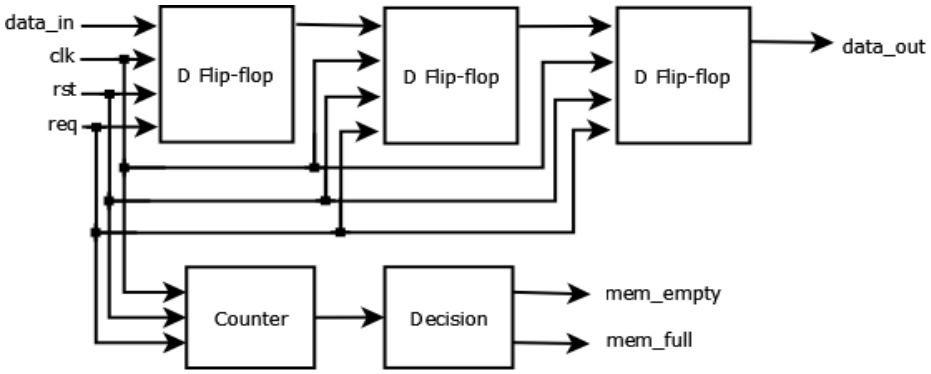

Fig.3: Internal Structure of FIFO

2.2. Controller Unit

The controller unit is used to control the direction of data flow through the router by controlling all the ports representing data flow in respective directions. The internal structure of the controller unit is shown in Fig. 4. This block mainly consists of multiplexers, de-multiplexer, D flip-flops and DEMUX Controller. Depending on the port select line each multiplexer will pass one of the four input signal to the respective output port. At each output port one D flip-flop is used to synchronize all data with clock signal. The enable port of the D flip-flop is controlled by DEMUX and DEMUX Controller. The DEMUX controller is used to route the request signal (req) to the rst port of the D flip-flop depending upon destination address which activates that particular direction D flip-flop to rout the data correctly in proper direction.

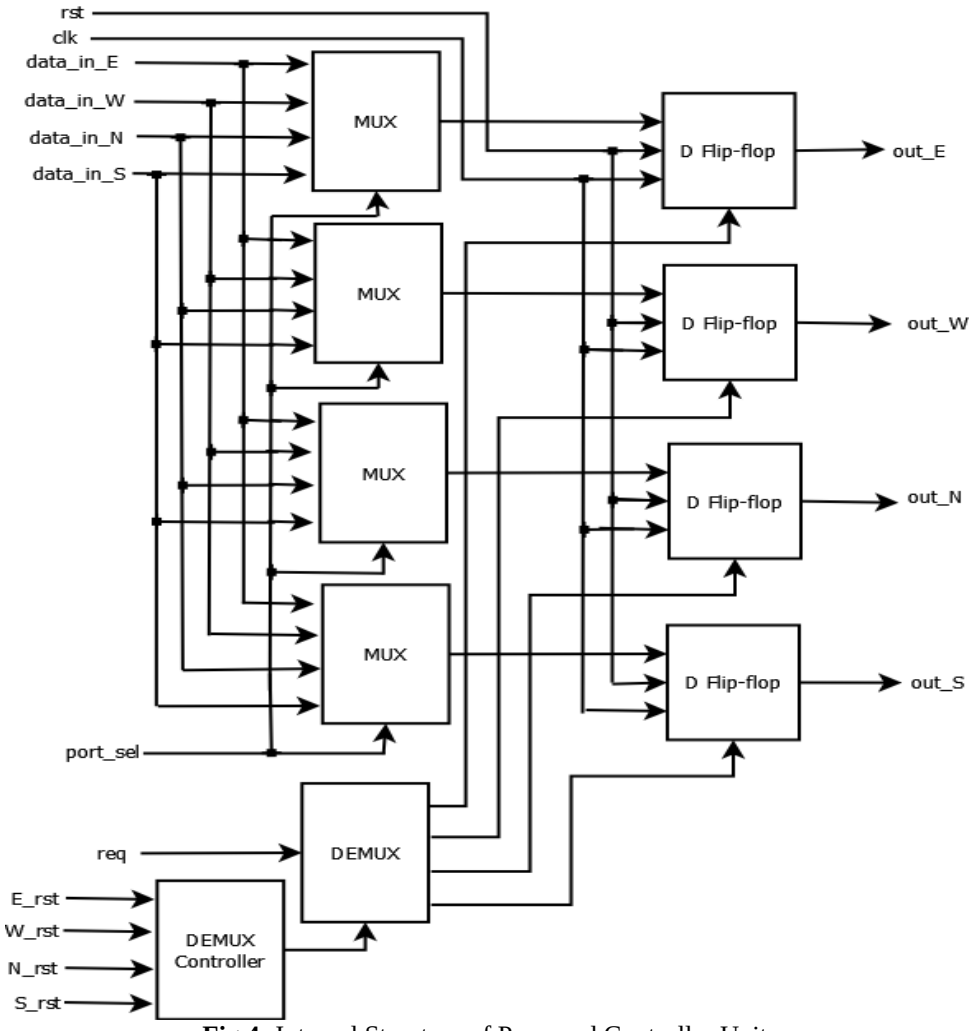

Fig.4: Internal Structure of Proposed Controller Unit

IV. FPGA Implementation

The proposed architecture is implemented on Spartan-6 (XC6SLX45-3csg324) FPGA board using Xilinx 14.5 software and simulation is checked by ISim simulator P.58f version. The coding of the architecture is done using VHDL language.

4.1. RTL Schematic

The snapshot of the RTL schematic generated by the software is shown in Fig. 5 which will show the internal blocks and their interconnections.

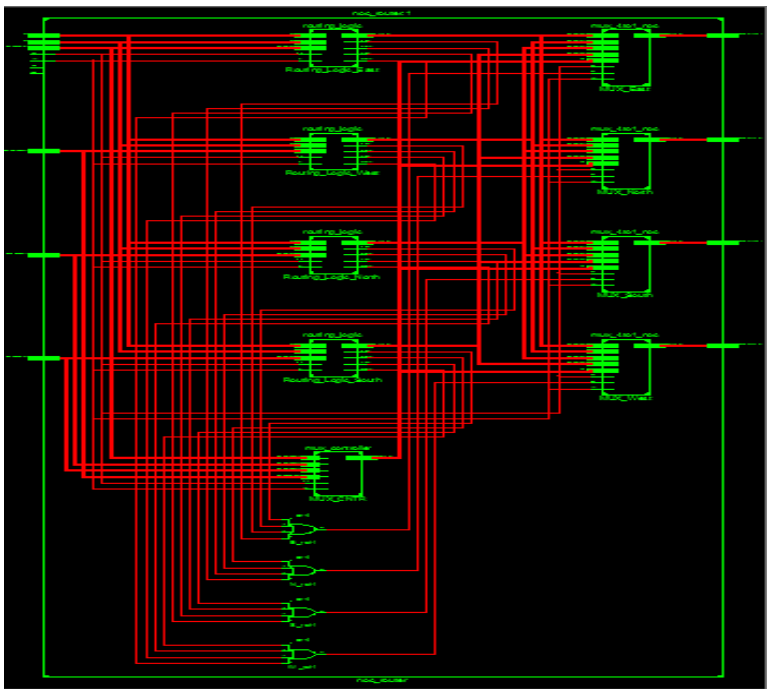

Fig.5: RTL Schematic of Proposed Router

4.2. Technology Schematic

Any FPGA will map digital logic in-terms of lookup table, LUT etc. The Internal Schematic of FPGA mapping is shown in Fig. 6

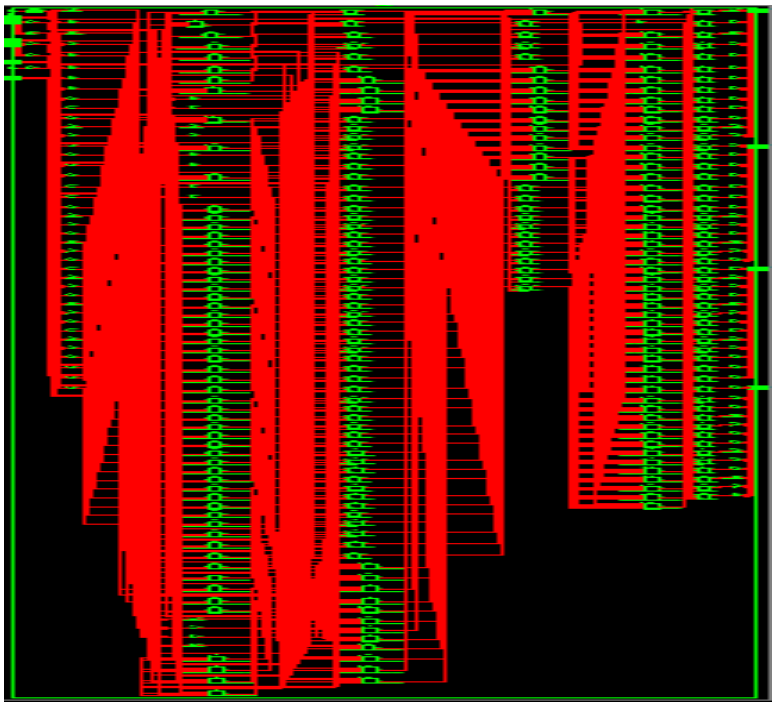

Fig.6: Technology Schematic of Proposed Router

4.3. Synthesis Report

The hardware utilization of the proposed structure is given in Table 1 for Spartan-6 (xc6slx45-3csg224) board. The proposed NoC router uses 224 slice registers, 162 slice LUT's and 128 LUT-FF pairs. The maximum operating frequency is 292.987 MHz.

Table I: Device Utilization Summery of Proposed Architecture

Parameters	Device Utilizations
Numbers of Slice Registers	224
Numbers of Slice LUT's	162
Numbers of fully used LUT-FF Pairs	128
Maximum Operating Frequency (MHz)	292.987

V. Comparisons With Existing Techniques

Hardware comparisons of proposed technique with existing techniques are given in Table 2. The architecture proposed by Suraj et al., [7] was implemented on Virtex-5 board and uses 1322 slice registers and 1022 slice LUTs. The architecture proposed by Afroz and Shaik [18] was implemented on Spartan-3 board and uses 31056 slice registers, 56690 slice LUTs, 22163 LUT-FF pairs with maximum operating frequency of 49.718 MHz. Also the architecture proposed by Ashis and Bhoyar [19] was implemented on Virtex-2 board and uses 529 slice registers, 954 slice LUTs, 523 LUT-FF pairs with maximum operating frequency of 226.19 MHz. The proposed architecture uses 529 slice registers, 954 slice LUTs, 523 LUT-FF pairs with maximum operating frequency of 292.987 MHz implemented on Spartan-6 board.

Table II: Hardware Comparisons of Existing Architectures with Proposed Architecture

Parameters	Suraj et al., [7]	Afroz and Shaik [18]	Ashis and Bhoyar [19]	Proposed
Board	Virtex-5 (XC5VLX50T)	Spartan-3 (XC3S500E)	Virtex-2 (XC2VP30)	Spartan-6 (XC6SLX45)
Number of Slice Registers	1322	31056	529	224
Number of Slice LUTs	1022	56690	954	162
Number of fully used LUT-FF Pairs	----	22163	523	128
Maximum Operating Frequency (MHz)	----	49.718	226.19	292.987

VI. Conclusion

In this paper we propose four port Network-On-Chip (NoC) router which is able to transfer the data in bi-directional manner. The architecture is able to operate at high speed without consuming large area. This is because the architecture is designed using basic elements are used in digital logic such as multiplexer, de-multiplexer, D flip-flop etc. Also the proposed architecture is suitable for VLSI implementation.

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