IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 6, Ver. II (Nov. - Dec. 2016), PP 82-86
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Algorithm to Design VGA Controller on FPGA Board

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Abstract: *The proposed work is to design and implement VGA (Vedio Graphics Array)Controller on FPGA, as a standard display interface, it is widely used. The controller is developed using Verilog HDL (Hardware description language) . It is implemented on FPGAs chip of Altera DE2-115 Development and Educational Board. The system will display the image on the monitor screen and test the design on the FPGA board.*
Keywords: *VGA Controller; Altera Quartus II; DE2-115 Development Board,Verilog HDL*

I. Introduction

A well-known standard interface VGA is used in many embedded systems video surveillance systems, ATM machines, video players, or video conferencing. This system provides a simple method to connect a system with a monitor for showing images or information. Depending on the needs of these applications, some systems may not require a high display quality. Therefore, VGA controller, which is a logic circuit to control the VGA interface, can be easily realized by FPGA technology with a low cost and high flexibility.[1]

Industrial production machines of today must be highly flexible in order to fulfil all unplanned demands. FPGA are especially suited to fulfil these requirements. FPGA provides an impacted size and low power consumption solution. For study, research and experimentation, the emerging technology of FPGA made VGA controller design accessible and suitable.[4]

In this paper, the Altera's FPGA is used for the hardware circuit. We take top-down programming methodology and adopt the integrated tools (Quartus version 13.0). After designing, compilation, function simulation, layout and timing simulation done and each module can be downloaded into FPGA. This method can reduce the size of the circuit board and enhance reliability of system and design flexibility. As a result, it can reduce the system cost.[7]

II. FPGA (Field Programmable Gate Arrays)

FPGAs are a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions.

FPGAs are also known as reconfigurable devices. These reconfigurable FPGAs are generally favored in prototype building because the device does not need to be thrown away every time a change is made. This allows one piece of hardware to perform several different functions.

FPGAs have compensating advantages, largely due to the fact that they are standard parts. There is no wait from completing the design to obtaining a working chip. The design can be programmed into the FPGA and tested immediately.[4]

2.1. Altera DE2-115 Development and Education Board

The Altera DE2-115 Development and Education board was designed. It is an ideal vehicle for learning about digital logic, computer organization, and FPGAs. Featuring an Altera Cyclone® IV 4CE115 FPGA, the DE2-115 board is designed for university and college laboratory use. It is suitable for a wide range of exercises in courses on digital logic and computer organization, from simple tasks that illustrate fundamental concepts to advanced designs.[6][7]

2.3 VGA Controller

The monitor screen for a standard VGA format contains 640 columns by 480 rows of picture elements called pixel. An image is displayed on the screen by turning on and off individually pixels. Turning on one pixel does not represent much, but combining numerous pixels generates an image. The monitor continuously scans

through the entire screen, rapidly turning individual pixels on and off. Although pixels are turned on one at a time, we get the impression that all the pixels are on because the monitor scans so quickly.[8]

The major component inside VGA monitor is color Cathode Ray Tube (CRT). The electron beam must be scanned over the viewing screen in a sequence of horizontal lines to generate an image. Light is generated when the beam is turned on by a video signal and it strikes a color phosphor dot on the face of the CRT. The video signal must redraw the entire screen at least 60 times per second to provide motion in the image and to reduce flicker.[8]

The VGA monitor is controlled by 5 signals: red, green, blue, horizontal synchronization, and vertical synchronization. VGA controller generates two synchronizing signals – Horizontal Sync (HS) and Vertical Sync (VS) to control the raster pattern and video data delivery. The VS signal defines the refresh frequency of the display (the frequency at which all information is redrawn). The HS signal defines the number of horizontal lines displayed at a given refresh rate. Both signals have the same waveform (Figure2.1), but their timing is different. The pixel clock defines the time available to display one pixel of information.[8].

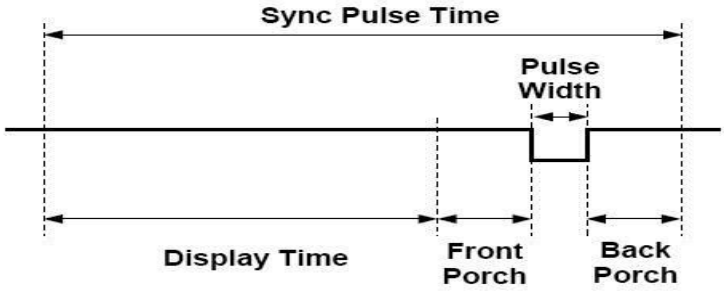

Figure 2.1: Sync Signal Waveform

To obtain the 640 × 480 screen resolution, a clock with a 25.175 MHz frequency is used.[3] A higher clock frequency is needed for a higher screen resolution. For the 25.175 MHz clock, the period is as below:

$$\frac{1}{25.175\ MHz} \approx 0.0397\,\mu s \text{ per clock cycle} \qquad (1)$$

Table 2.1 provides timing information for driving a CRT monitor in 640-pixels by 480-rows mode, using 25MHz pixel clock and 60Hz refresh frequency. LCD displays can also be controlled using the same synchronization timing. Note that during the front and back porch intervals information can not be displayed (RGB signals must be set to zero).Generally, a counter clocked by the pixel clock could control the horizontal timing. From its value current pixel display location on a given row can be easily tracked, as well as thecorrect time for HS signal transitions. A separate counter can could do the same to control the vertical timing.

It increments with each HS pulse, tracks the current display row and can be used to control the VS signal transitions. Values of these two constantly running counters can be used to form a Video Memory address for the currently displayed pixel.[8]

Parameter	Vertical Sync			Horizontal Sync	
	Time	Clocks	Lines	Time	Clocks
Sync Pulse Time	16.7 ms	416800	521	32 µs	800
Display time	15.36 ms	384000	480	25.6 µs	640
Pulse Width	64 µs	1600	2	3.84 µs	96
Front Porch	320 µs	8000	10.	640 ns	16
Back Porch	928 µs	23200	29	1.92 µs	48

Table2.1: 640x480 60Hz Mode Synchronization Timing

III. Proposed Architecture

3.1 Proposed Block Diagram

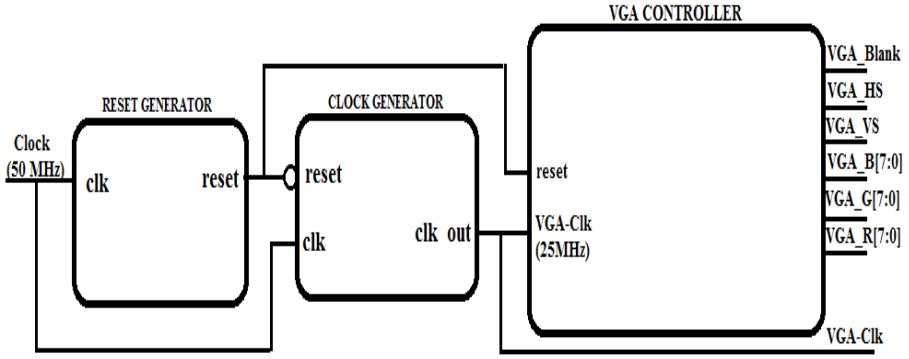

Fig3.1. Proposed Block Diagram

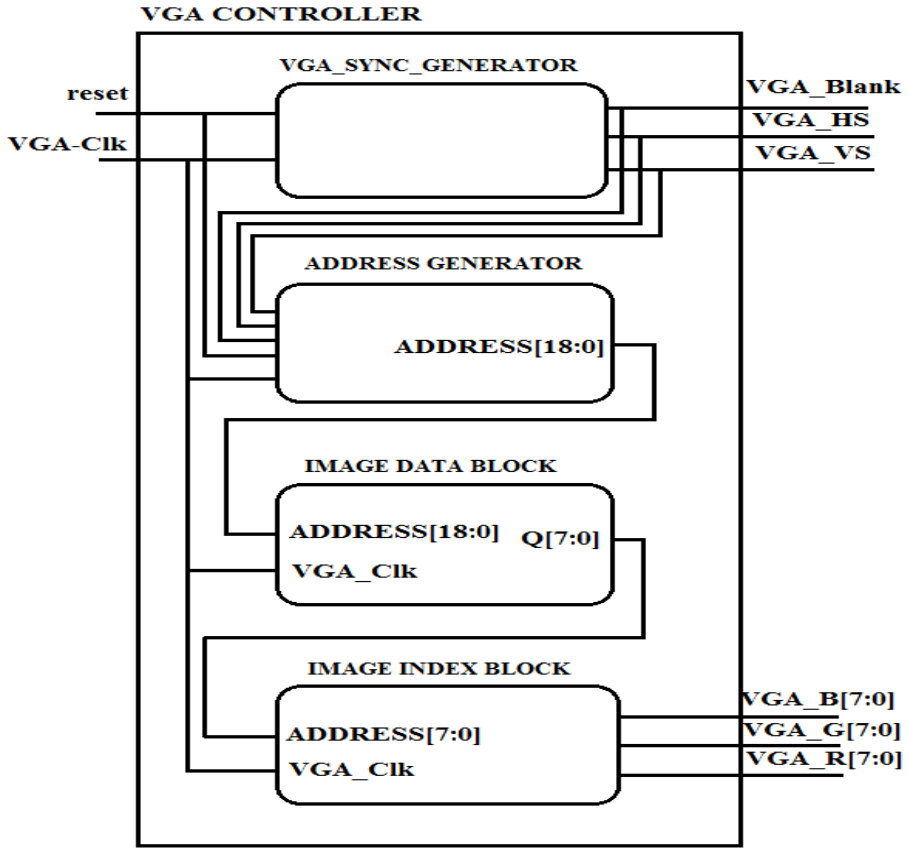

Fig.3.2. Internal Block Diagram of VGA Controller.

Figure 3.1 & 3.2 shows, the proposed block diagram of VGA Controller, which consist reset, clock generated block and VGA Controller block. And the internal block diagram of VGA Controller which consists VGA synchronization block, address generator block, image data block, and image index block. As input we have to give clock pulse and reset signal and at output, we will get RGB (red, green, blue), horizontal synchronization, vertical synchronization and blanking signals.

From Fig. 3.1 & 3.2, the function of reset block is to generate the reset signal and the function of "clock generator" block is to reduce the frequency of input clock from 50 MHz to 25 MHz, as to achieve 640 x 480 resolution. Meanwhile, "vga_sync" block is used to generate timing and synchronization signals. while the "h_sync" signal specifies the required time to scan a row, and the "v_sync" signal specifies the required time to scan the entire screen. "vga_sync" block also generates the "blank" signal which indicates retrace period of the display.

IV. Implementation and Results

Steps of Implementation:

I. Take DE2-115 Development Board.
II. Connect 12V supply through adapter to turn ON/OFF the board.
III. Connect USB cable to laptop/computer and also to the USB Blaster of the Board.
IV. Open Quartus II software, by double clicking on Quartus II icon.
V. Compile Verilog code in Quartus II.
VI. Assign a pins at pin planner, by using user manual of DE2-115 board.
VII. For program dumping on board, click Tool > Programmer.

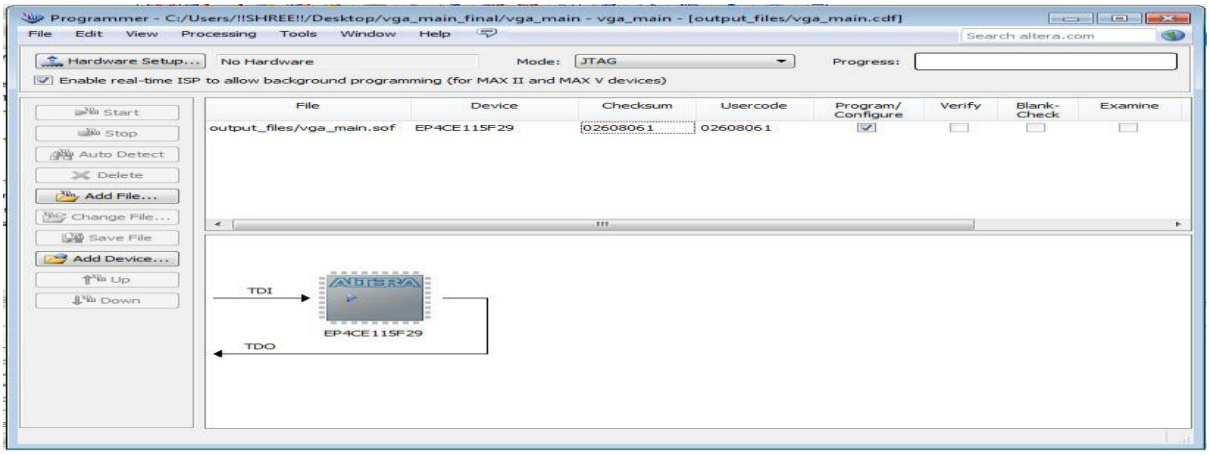

Fig.4.1. Quartus II Programmer Window[7]

VIII. Select AS programming mode

AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non volatile storage of the bit stream, so that the information is retained even when the power supply to the DE2-115 board is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

IX. Click Start

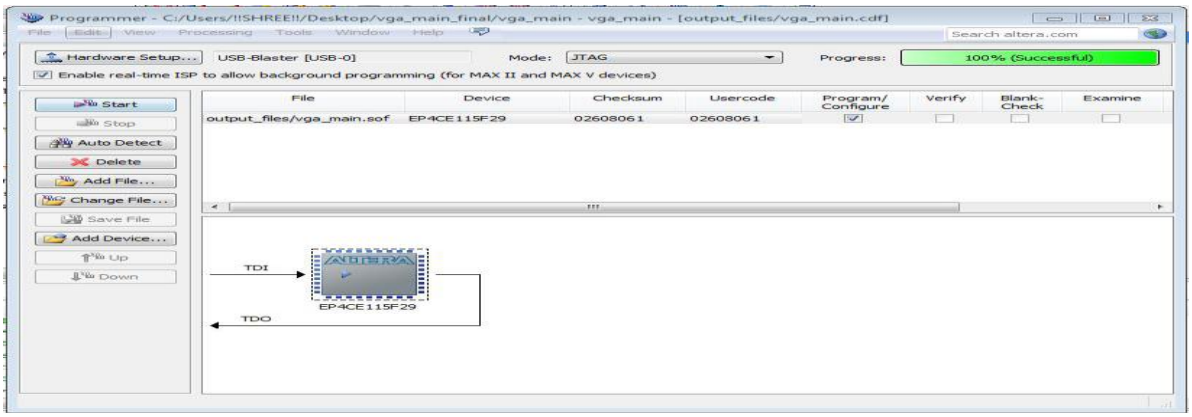

Fig 4.2. Connections between FPGA and VGA.[6]

XI. After successful downloading, connect board with moniter by using VGA cable.
XII. And observe the image on screen

4.1. Simulation Results of VGA Controller

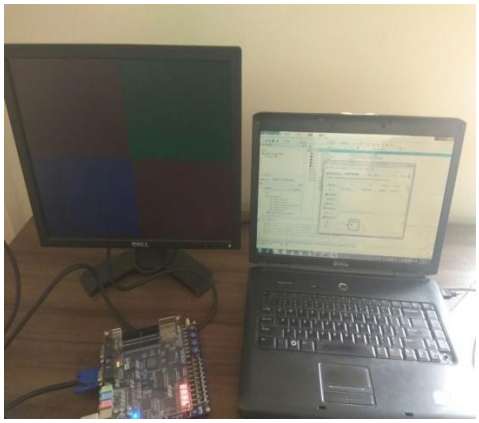

Fig.4.1.1. Implementation of VGA Controller

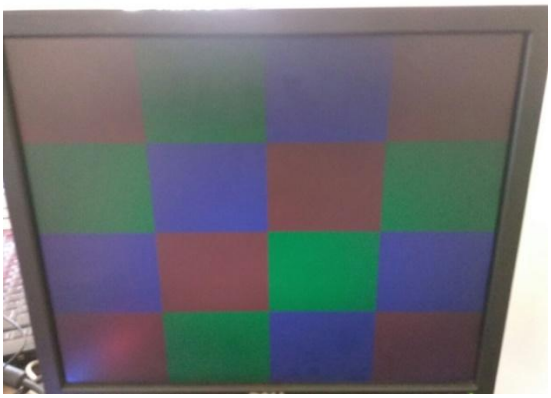

Fig.4.1.2. Final output Image for 4×4 dimension And final output Image for 2×2 dimension

Fig.4.1.3. Final output Image for 8×8dimension

In order to be able to see the results obtained from the proposed algorithms on an FPGA, a standard VGA monitor may be chosen. The system can be connected to any VGA port LCD (Liquid Crystal Display) or CRT (Cathode Ray Tube) monitor. After compilation is completed, download the Verilog Program into the target device (EP4CE115F29C7). After successfully downloading, choose working mode of electric circuit and observe image on the monitor.

V. Conclusion

The proposed architecture used in any FPGA device regardless of the brand or model. In this algorithms, Programming in Verilog HDL makes the design flexible and convenient. The VGA controller is used for image processing and its results are better than conventional method. The 8×8 output displays image or information in better resolution than 4×4 and 2×2 output and Verilog code is implemented on FPGA board. Further, a CMOS digital camera can be developed using this VGA controller algorithms.

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