IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 6, Ver. II (Nov. - Dec. 2016), PP 48-64
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Reversible Logic-MUX-Multiplier based Face Recognition using Hybrid Features

Sujatha B M[1], Shubhangi Lagali[2], Nayina Ramapur[2], K Suresh Babu[3], K B Raja[3], Venugopal K R[3]

[1]*Acharya Institute of Technology, Bangalore, India.*
[2]*Saitektronix Private Limited, Bangalore, India*
[3]*University Visvesvaraya College of Engineering, Bangalore University, Bangalore, India.*

Abstract: *The face recognition is used to identify a person for access into work place, home, electronic gadgets etc. In this paper, we propose Reversible Logic MUX-Multiplier (RLMM) based Face Recognition using Hybrid Features. The novel concept of RLMM is introduced in designing multiplier for edge detection of face images using reversible logic gates. The steganography is used to convert two images of same person into one image. By using Canny Edge Detection, the edge detected stegoimages are obtained in order to create the database. The resize and Gaussian filter techniques are used in preprocessing of face images. The Discrete Wavelet Transform (DWT) and Local Binary Pattern (LBP) coefficients are computed from images and are fused to extract initial features. The final features are obtained from the output of Self Organizing Map (SOM) for the input of initial features. The Euclidian Distance (ED) is used to compare final features of face database images and test images to compute performance parameters. It is observed that the performance of the proposed method is better compared to existing methods. The proposed Multiplier and canny edge detection is coded using VHDL, synthesized and simulated using Xilinx ISE 14.5i tool. The face recognition is performed using Matlab 2012*

Keywords - Biometrics, Canny Edge Detection, DWT, Face recognition, LBP, Steganography.

I. Introduction

The origin of biometrics is said to have been in nineteenth century, where the human beings were identified using face, voice and gait. The biometric authentication technology is used to identify persons based on the physiological and behavioral traits in recent years. The physiological traits are human body parts such as face, fingerprint, palm print, iris etc. The behavioral traits of persons are based on behavior and examples are voice, keystroke, gait etc., which vary based on circumstances and mood of a person. The biometric recognition is broadly classified as i) The biometric identification: The identification of individuals carried out by using their physiological and behavioral traits and ii) The biometric verification: A person can be identified uniquely by evaluating one or more different biological traits.

The biometric system has three sections viz., (i) Enrollment section (ii) Test section and (iii) Matching section. (i) *Enrollment section*: The face images of different angles, illuminations, and sizes are considered from different available databases or the face images captured through camera to create face database. In order to create database of large number of persons with number of images per person and variations in pose, illumination are considered. The preprocessing techniques are used to resize face images to obtain uniform size of face images, and also filters are used to enhance quality of images. The features are extracted from preprocessed images for comparison to identify a person. The spatial domain features such as standard deviation, mean and variance are computed to extract features. Principal Component Analysis (PCA), Singular Value Decomposition (SVD), etc., are used to obtain spatial domain features. The frequency domain features are extracted using Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Short Time Fourier Transform (STFT), Discrete Wavelet Transform (DWT). The hybrid features which are the combinations of spatial domain and frequency domain are extracted. (ii) *Test section*: In this section, the preprocessing and feature extraction techniques are similar to that of enrollment section. The database in the enrollment section is replaced by test images by considering single image per person. (iii) *Matching section*: In this section, the features of enrollment and test sections are compared to compute performance parameters such as Total Success Rate (TSR), False Rejection Ratio (FRR), False Acceptance Ratio (FAR), Equal Error Rate (EER) and Optimum TSR of a biometric system. The Euclidian Distance (ED), Hamming Distance (HD), Chip square, Neural Network, Support Vector Machine (SVM), Self Organizing Map (SOM), etc., are used in the matching section.

The advantages of biometrics are, the passwords cannot be stolen or forgotten, very high security, it acts like a key which cannot be transferred, user friendly and safe. The limitations of biometrics are, it costs

high to implement and manage the database and the supporting system. Biometrics such as face and fingerprints can be easily recorded and may be misused by biometric experts without the presence of user. Lot of memory may be required for database storage.

Applications of Biometrics are (i) To identify criminals and intruders. (ii) It is used in forensic to identify criminals, surveillance etc. (ii) Government organizations for identification cards, driving licenses, employee identification etc. (iii) Military programs for national security. (iv) Commercial such as account access, ATM's online banking etc. (v) Health care for patient identification and to save personal information.

The computers have evolved in the market are faster, smaller and more complex than their predecessors. The speed and complexity are the main things that contribute for cost. There is always an increasing demand for Embedded Digital Signal Processing (EDSP) systems which are portable with the advancement in the VLSI technology. The irreversible logic circuits used for adders and multipliers in EDSP consume more power. The reversible logic gates are used in adders and multipliers to save the power consumption. The Vedic multipliers and MUX based multipliers are used in place of conventional multipliers to save power and increase the speed of computation.

Contribution: In this paper RLMM based face recognition using hybrid features is proposed. The reversible logic MUX based Multiplier is designed for edge detection of face images. The steganography is introduced to reduce the number of face images of a person. The features are extracted using DWT, LBP and SOM. The performance parameters are computed by comparing features of face database and test image using ED.

Organization: The rest of the paper is organized as follows, the literature survey of existing techniques are discussed in section II. Section III provides the design of proposed RLMM. Section IV provides the proposed RLMM based face recognition using steganography, edge detection and hybrid features. Section V provides the performance analysis of proposed reversible multiplier. Section VI gives the performance analysis of face recognition using proposed multiplier. Finally, the conclusion is given in section VII.

II. Literature Survey

Himanshu Thapliyal and Srinivas[1] proposed NxN reversible multiplier using TSG gate. In this Fredkin Gates are used to generate partial products in parallel with delay and the addition is reduced to $\log_2 N$ steps using designed reversible multiplier with TSG gate. They have also designed 4x4 architecture using this reversible multiplier. Nidhi Pokhriyal et al., [2] proposed a 8x8 Vedic multiplier using 4: 3, 5: 3, 6: 3 and 7: 3 compressors to obtain sum of partial products. A robust area and power efficient multiplier architecture has been obtained by combining Vedic sutras- Urdhwa Triyakbhyam and efficient compressors. The synthesis and analysis has been done using cadence tool in 180 nm technology. Maryam Ehsanpour et al., [3] have designed reversible 4-bit binary multiplier circuit using Modified Full Adder (MFA) with less hardware complexity. They have also shown that the designed reversible circuits can also work as a reversible full adder and demonstrated that the circuit requires few garbage outputs and constant inputs. Madhusmita Mahapatro et al., [4] designed arithmetic circuits using reversible logic gates. They have developed arithmetic circuits using 0.25 micrometer technology to simulate and synthesize. Reversible full adders and half adders are designed using reversible logic. A 4-bit binary parallel adder and 4x4 multiplier circuits have been designed using the reversible full adders and half adders.

Anindita Banerjee and Anirban Pathak [5] designed reversible multiplier circuit through NCT gate (NOT, CNOT, Toffoli). This is based on generating all partial products and adding partial products using binary tree network. Reversible partial products generation circuits and parallel adder circuits are designed. This design has minimum number of garbage outputs, gate count and quantum cost. Jenath and Nagrajan [6] designed a reversible single precision floating point multiplier. Peres gates are used to design multiplier. Multiplier operands are decomposed into three portions of 8 bits each. Reversible multiplier of 24x24 bits is performed using nine 8x8 bit multipliers. Efficient multiplier is designed in terms of quantum cost, delay and garbage outputs. This is designed using VHDL code and simulation is done using Xilinx 9.1 simulation tool. Kartikeya Bhardwaj and Bharat M Despande [7] proposed an improved Booth's Recoding Algorithm also called K-algorithm for signed multiplication to reduce the hardware complexity. To implement this algorithm, efficient multiplier architecture is also proposed. They have designed 4-bit reversible multiplier with and without fault tolerance based on Booth's Recoding algorithm. They have analyzed garbage values, number of gates used, constant inputs and quantum cost using this method. The quantum cost is reduced by 33% compared to existing methods using this approach.

Pradip Panchal et.al, [8] presented a work on face recognition using LBP. Locally enhanced LBP is generated by dividing face images into sub regions to provide features information. GLBP image is obtained by concatenating all individual local histograms. The performance of this technique is tested for face illumination and expression variations. With this method they have achieved a recognition rate of 80%. Bilel Ameur et.al, [9] proposed a work face recognition. Feature extraction is done using Gabor wavelets and LBP. The dimension reduction technique is used to reduce the pattern vector. This method is applied on LFW database and obtained

recognition rate of 94.16%. Paitoon yodkhad et.al [10] proposed a face recognition using SOM. PCA and SOM techniques are used for feature extraction. The effective features are extracted and applied to SOM. All sample training sets are grouped based on nearest prototype. In the local feature selection useless features are removed to reduce classification time. Nearest neighbor classifier is used for feature classification.

Vojtech Jirka et.la,[11] presented a work on face recognition using PCA and SVM. Preprocessing of input images is carried out using histogram equalization (HE) and contrast limited adaptive histogram equalization (CLAHE). PCA is used for feature extraction to reduce number of features in the data and SVM is used for classification. Amir Benzaoui et.al, [12] proposed an automatic biometric system using 2D face images. One Dimensional Local Binary Pattern (1DLBP) texture descriptor is used for feature extraction. The performance of the features is improved using wavelets to reduce dimensionalities of vectors. Better recognition rates are obtained against different illumination variations, occlusions and noise. Swati Jadon et. al, [13] presented face recognition method using different feature extraction techniques. Directional Discrete Cosine Transform (DDCT), Discrete Wavelet Transform (DWT), Discrete Cosine Transform (DCT) and Sobel Edge Detection (SED) techniques are used for feature extraction and SOM is used for training database. Better recognition rates are obtained for DDCT method compared to DWT, DCT and SED methods.

III. Design of Proposed Reversible Logic Mux-Multiplier (RlMM)

3.1 4x4 Reversible Logic Multiplier Using 8x8 Multiplexer based Multiplier

The Vedic concept of MxN bit multiplication based on multiplexer will reduce the delay by using Urdhva Tiryakbyham sutra [14]. The direct multiplication used in 1Vedic concept will cause more delay for higher order bits as more number of carry propagation is carried out. Therefore the use of multiplexer based multiplier reduces delay as well as minimizes power dissipation since reversible logic is used.

The proposed 4x4 MUX based multiplier is designed using reversible logic and the block diagram is shown in Figure 1. The multiplier uses 16x1 MUX and the operations shift left by 1, shift left by 2 and shift left by 3. In this multiplier the four select lines S3S2S1S0 will act as 4- bit multiplicand and the input I1 to I16 acts as multiplier. Depending on the select line any one of sixteen inputs will be passed as the output. The output of the multiplexer will be the product obtained by the multiplication of multiplier and multiplicand.

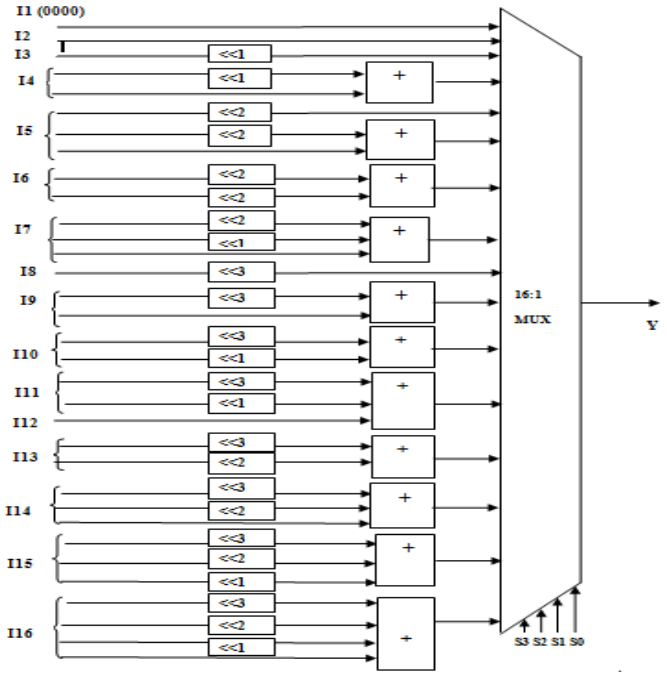


Figure 1: Block diagram of 4x4 Reversible Logic MUX-Multiplier (RLMM)

3.1.1 Shift left operations using reversible logic gates

(a) Reversible Shift left by 1

The four bit binary input say x (3:0) is considered with x (0) as the LSB and x (3) as the MSB. Five PG's with three inputs and three outputs are considered for shift left by 1 operation as shown in the Figure 2. For PG1 first two inputs are assigned as zero values and LSB x (0) is given to the third input. The first output of every PG (Peres Gate) is zero and it acts as first input to the successive PG's. The second output of every PG acts as output of shift left by 1 operation for the given input. The third output of every PG acts as second input

to the successive PG's. The third input to PG2, PG3 and PG4 are x(1), x(2) and x(3) respectively. The third input to PG5 is zero.

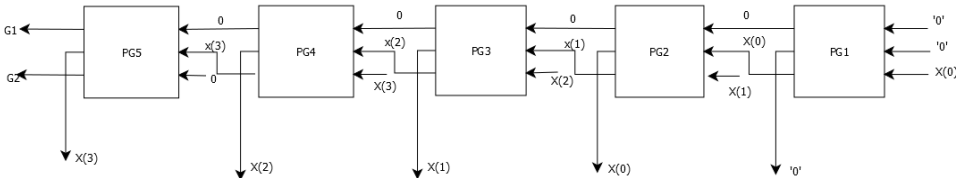


Figure 2: Reversible Shift left by 1

(b) Shift left by 2

The Shift left by 2 operation is implemented by using six PG's as shown in Figure 3. The three inputs to PG1 are assigned as zeros. The gates PG2, PG3, PG4, PG5 and PG6 connections are similar to that of the shift left by 1 operation.

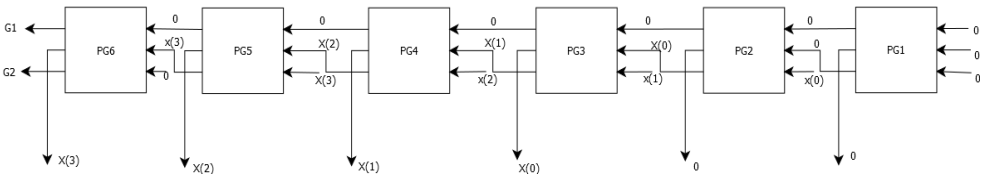


Figure 3: Reversible Shift left by 2

(c) Shift left by 3

The operation is implemented using seven PG's as shown in Figure 4. The three inputs to PG1 and PG2 are assigned as zeros. The gates PG3, PG4, PG4, PG5, PG6 and PG7 connections are similar to that of shift left by 1 operation.

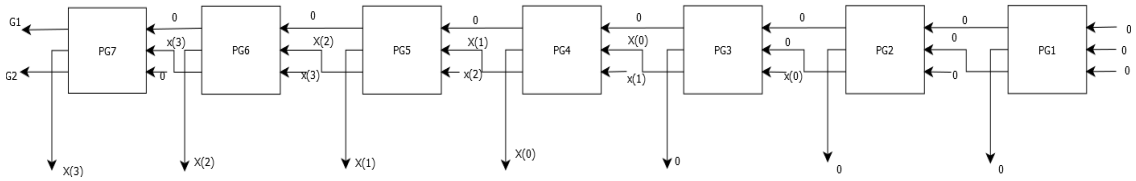


Figure 4: Reversible Shift left by 3

3.1.2 Reversible Logic Adder

A single HNG (Haghparast Navi Gate) is configured as full adder when the last input is set to zero. Among four outputs, two are the adder outputs sum = A⊕B⊕Cin, carry out = (A⊕B)Cin⊕AB, remaining two G1 and G2 are garbage outputs. The four bit full adder is implemented using three HNG gates and one PG gate as shown in Figure 5.

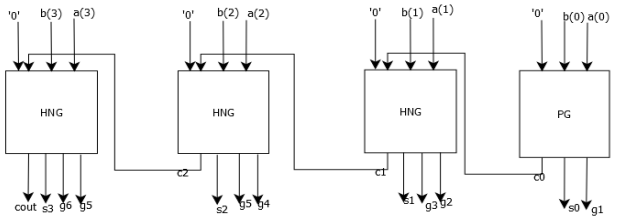


Figure 5: Design of 4-bits full adder using HNG gate

3.1.3 Reversible Logic Multiplexer

The 2:1 MUX is designed using FRG (Fredkin Gate) gates [15] as shown in the Figure 6. Among the 3 inputs of FRG, first input is the select line of multiplexer and other two are I0 and I1. Depending on the value of select line, either of the remaining two inputs will be selected as the output. If the select line is '0' the I0 is sent as output or if the select line is '1', I1 is sent as output of multiplexer. Using three FRG's 4:1 multiplexer is built. It is extended to 8:1 MUX and 16x1 MUX by using seven FRG's and fifteen FRG's respectively. The unused values are treated as garbage values.

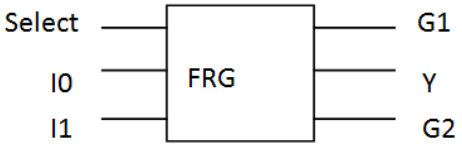


Figure 6: Multiplexer 2:1 using FRG gate.

.

3.2 8x8 Reversible Logic Multiplier Using 4x4 Multiplexer based Multiplier with Vedic concept

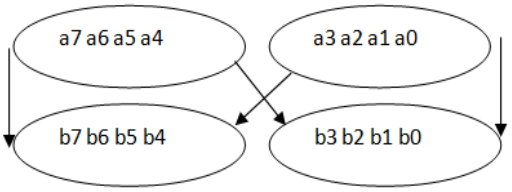


Figure 7: Vertically and crosswise Vedic concept

The proposed 8-bit multiplier is designed using four 4x4 MUX based Vedic multipliers [16] i.e., by using reversible logic gates in shift left operations and multiplexers. Figure 7 shows vertically and crosswise Vedic concept**.** The outputs of the 4x4 MUX based Vedic multipliers are given to ripple carry adders which are also built using reversible logic gates. The proposed 8x8 multiplier block diagram is shown in Figure 8.

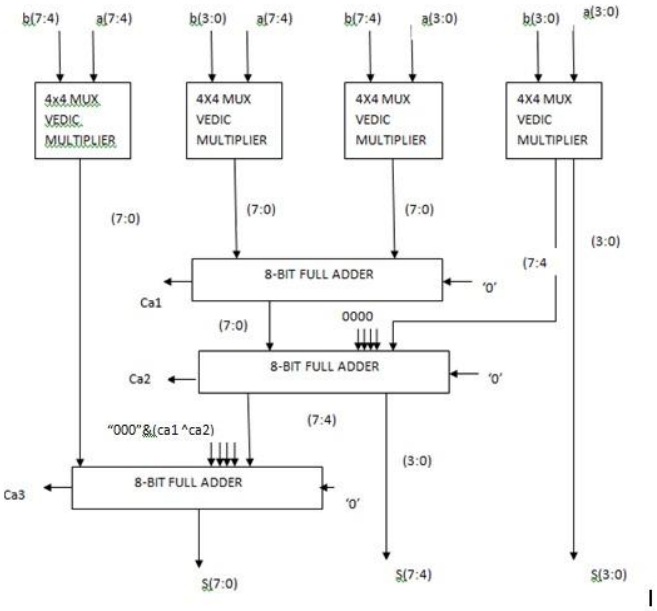


Figure 8: 8x8 Vedic multiplier using 4x4 Vedic concepts.

The 8-bit data is divided into two 4-bit numbers such as [a(7:4) & b(7:4), a(3:0) & b(7:4), a(7:4) & b(3:0), a(3:0) & b(3:0)] and given as inputs to the 4-bit MUX based multiplier blocks. The outputs of four MUX based multiplier blocks represent 8- bit products which are added using 8-bit full adder which is built by reversible logic HNG gates.

3.3 16x16 Reversible Logic Multiplier Using 8x8 Multiplexer based Multiplier

The partial products obtained from the four 8x8 Vedic multipliers are demarcated into four regions as in Figure 9. The eight LSB bits are taken as product bits S [7:0] and it is obtained from one of the multipliers. The product obtained from second and third multiplier is added using 16-bit ripple carry adder. The next higher order bits of first multiplier block is added to the next 16-bit ripple carry adder which gives the product bits S[15:8]. Then the MSB product bits S [31:16] are obtained by adding the fourth multiplier output to the next 16-bit ripple carry adder. Finally, 32-bit product is obtained for 16 x16 multiplier.

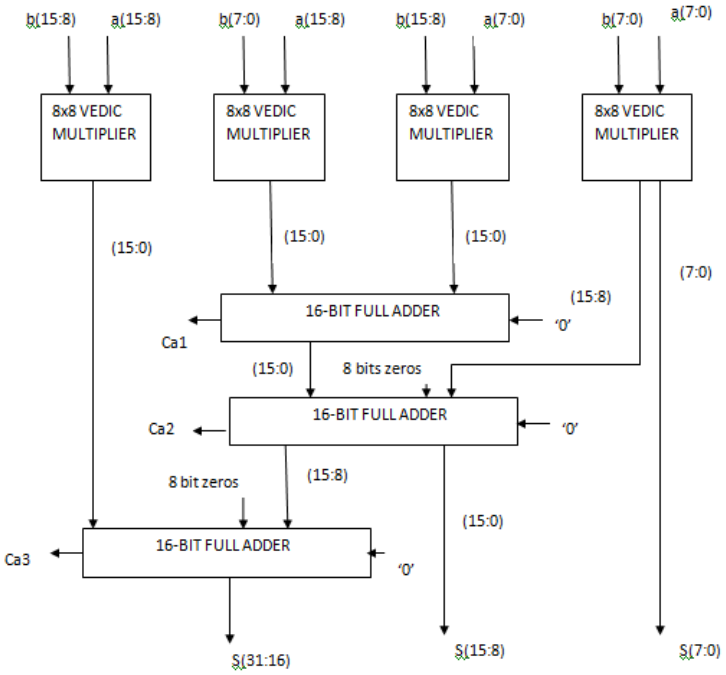


Figure 9: 16×16 Vedic multiplier using 8×8 Vedic multiplier

3.4 32x32 Reversible Logic Multiplier Using 16x16 Multiplexer based Multiplier

The partial products obtained from the four 16 x16 multipliers are demarcated into four regions as in Figure 10. The sixteen LSB bits are taken as product bits S [15:0] and it is obtained from one of the multipliers. The product obtained from second and third multiplier is added using 32-bit ripple carry adder. The next higher order bits of first multiplier block is added to the next 32-bit ripple carry adder which gives the product bits S [31:16]. Then the MSB product bits S[63:32] are obtained by adding the fourth multiplier output to the next 32-bit ripple carry adder. Finally, 64-bit product is obtained for 32x32 multiplier.

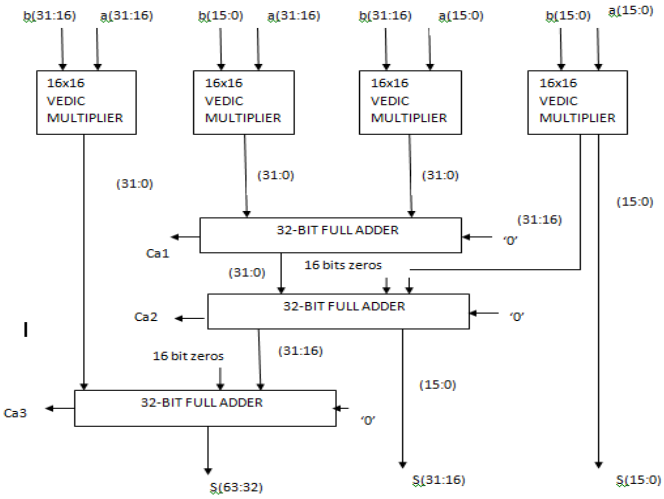


Figure 10: 32×32 Vedic multiplier using 16×16 Vedic multiplier

IV. Proposed RLMM Based Face Recognition Using Steganography, Edge Detection and Hybrid Features

The Face recognition using the proposed Reversible Logic MUX-Multiplier (RLMM) in the canny edge detection using the steganography technique based on DWT, LBP and SOM is shown in the Figure 11. The proposed RLMM is used in the canny edge detection. Firstly, using steganography technique fifty percent of the total number of images per person is reduced. By fusing DWT and LBP features the initial features are obtained. The final features are generated by using SOM to which initial features are fed as input.

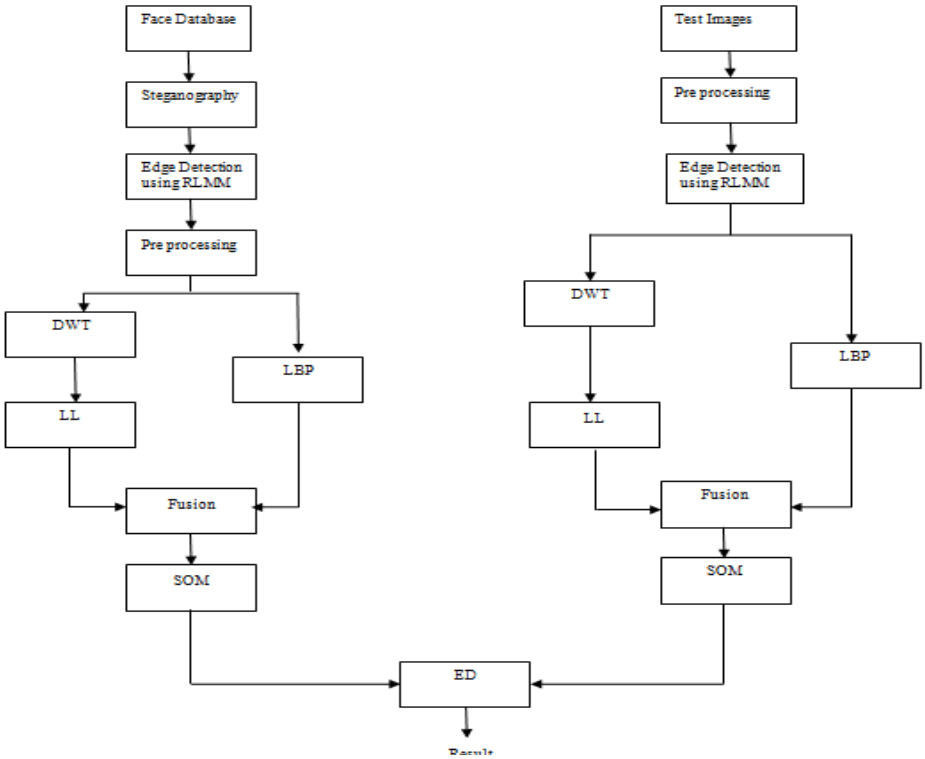


Figure 11: Block diagram of proposed Face recognition using RLMM

4.1 Face databases

The various performance parameters are measured using available face databases such as Olivetti Research Laboratory (ORL), Indian Male, Indian Female, Near Infra Red (NIR) and Yale Database in the proposed method.

(a) ORL Face database

These are captured in April 1992 and April 1994 at AT & T laboratories, Cambridge. It has 40 persons and each person has ten samples [17].

(b) Indian Male Database

The database is created at Indian Institute of Technology, Kanpur [18]. In this database there are twenty persons in which each person has eleven face images with different poses. Images have resolution of 640X480.

(c) Indian Female Database

This database has twenty two persons and each has eleven images [18]. The images have resolution of 640X480 each are with different facial expressions and different poses.

(d) NIR Database

In order to avoid misinterpretation due to the variation of luminance intensity and to reduce illumination effect this database is introduced. It has 120 persons and each person has 15 different pose variations [19].

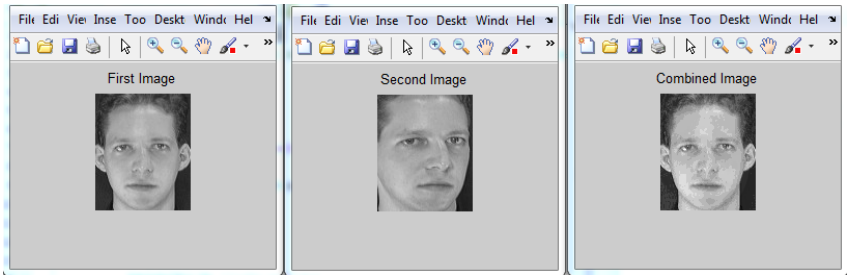
(e) YALE Database

The database is generated at Yale Center for Computational Vision and Control [20]. It has 15 persons and each has 10 images with different facial expressions like with and without glass right sided, left sided, happy, sad, sleepy, surprised and wink. Each image has a resolution of 240X320.

4.2 Steganographic Image Reduction

In order to save memory and increase the speed, the number of face images of a person in the face database are reduced to fifty percent by making use of steganographic technique [21]. Using spatial domain steganography technique every two images of size 112x92 of a person are converted into one image. The MSB's of second image is replaced by the corresponding LSB's of the first image to obtain stegoimage which is same as first image.

Example: The first image has first pixel intensity value say 42 and the corresponding binary is 0010 1010 which has MSB 0010 and LSB 1010. The second image has first pixel intensity value say 202 and the corresponding binary is 11001010 which has MSB 1100 and LSB 1010. A single image (stegoimage) is formed by using the first and second images based on steganography technique. Now the stegoimage has first pixel intensity value as 44 and binary is 00101100 which is obtained by replacing the LSB's of the first image with the MSB's of second image.The pixel intensity value 44 in the stegoimage is almost same as that of first image. The significant information of both first and second images are in the stegoimage. Therefore the steganography technique is used in order to reduce the number of images in the database by fifty percent. The pair of images of one person is considered and converted into one stegoimage by using LSB replacement technique as shown in Figure 12.



(a) (b) (c)

Figure 12: One stegoimage from two images

4.3 Canny Edge Detection

Canny edge detection [22] technique extracts useful structural information from images and reduces the amount of data to be processed. The required edge detection coefficients for the calculation of gradients in x and y direction are Gx and Gy respectively.

$$Gx=\begin{pmatrix} -1/4 & -1 & -1/4 \\ 0 & 0 & 0 \\ 1/4 & 1 & 1/4 \end{pmatrix} \qquad Gy=\begin{pmatrix} -1/4 & 0 & 1/4 \\ -1 & 0 & 1 \\ -1/4 & 0 & 1/4 \end{pmatrix}$$

The edge detection is used to generate new databases from the available databases like ORL, JAFEE YALE etc and these are further used in Face Recognition.

4.4 Pre-Processing

The various face images of different sizes are resized and the quality of image is improved using filters in preprocessing unit.

4.4.1 Face Image Resize

The edge detected ORL face database images of size 256*256 has been resized to 112 *92. The test images are also resized in order to test the performance of the proposed algorithm.

4.4.2 Gaussian Filter

The presence of noise in the image due to camera quality and the surrounding environment needs to be filtered. Gaussian Filter [23] is most suitable to remove Gaussian noise. The impulse response of the Gaussian filter is given in equation (1).

$$g(x,y)=\frac{1}{2\pi\sigma^2}e^{-\left(\frac{x^2+y^2}{2\sigma^2}\right)} \qquad \text{(1)}$$

Where σ is standard deviation of Gaussian distribution
x is the distance in the horizontal direction from origin
y is the distance in the vertical direction from the origin.

For σ=1, the impulse response is given in equation (2).

$$g(x,y)=\frac{1}{2\pi}e^{-\left(\frac{x^2+y^2}{2}\right)} \qquad \text{(2)}$$

The values of x and y are ranging between -1 and 1 as shown in Table 1.

Table 1: x and y coordinates

(-1,1)	(0,1)	(1,1)
(-1,0)	(0,0)	(1,0)
(-1,-1)	(0,-1)	(1,-1)

By substituting the different combinations of x and y values of Table 1 in equation (2), the approximate numerical values are computed which yields Gaussian mask as given in Table 2.

g (-1,-1) = 0.0585≈0.0625=g(1,1) =g(-1,1)= g(1,-1)
g(0,1) = 0.096 ≈0.125=g(-1,0)= g(1,0)= g(0,-1)= g(0,1) g (0,0) = 0.159 ≈ 0.25

Table 2: Gaussian mask

(1/16)

1	2	1
2	4	2
1	2	1

In order to obtain the filtered image, the image is segmented into 3X3 overlapping block. Along with the 3X3 Gaussian mask, the pixel values of each block of an image are multiplied position wise to obtain equivalent 3*3 matrix.

4.4.3 Feature Extraction

By fusing spatial and transform domain techniques such as LBP and DWT, the initial features are obtained. The initial features are fed to SOM and the final features for the biometric system are generated.

(a) Local Binary Pattern

In order to identify face images effectively the spatial domain texture pattern features are generated using LBP [24]. The face image matrix pixel intensity values are divided into 3*3 overlapping matrices. The center pixel value in the 3*3 matrix is converted into new value based on binary pattern of the eight surrounding pixel values using equation (3) and which shows the binary pattern of surrounding pixels generated.

$$X_i = \begin{cases} 1 & I_p \geq M_{avg} \\ 0 & I_p \geq M\_avg \end{cases} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where, X_i is the binary bit obtained after comparing of i^{th} pixel
I_p is the center pixel value in the 3X3 matrix.
M_{avg} = Average absolute value of eight surrounding pixel values

$$= \frac{(|m1|+m2|+|m3|+\cdots+|m8|)}{8}$$

m_1 to m_8 = pixel intensity values of surrounding eight pixels.

(a) 3X3 Matrix

106	108	103
113	116	110
116	114	118

(b) Binary Values

0	0	0
1	-	0
1	1	1

(c) Decimal weights for Binary position

128	64	32
16		8
4	2	1

Figure 13: Local Binary Pattern Generation for 3X3 Matrix

Figure 13 shows an example of LBP on 3*3 matrixes. The average value of boundary pixel values of 3*3 matrix excluding the centre pixel value is equal to 111. Each neighboring pixel values are compared with pixel intensity value 111 and the corresponding binary values are assigned. Figure 13 (c) shows the decimal weights. The decimal equivalent of 23 from binary value 00010111 is used to replace the center pixel intensity

value of 3*3 matrix. Similarly the centre pixel value of each 3*3 overlapping matrix of entire image is converted into new values based on surrounding eight pixels to extract texture features of an image. Figure 14 shows the LBP generated image from the preprocessed image.

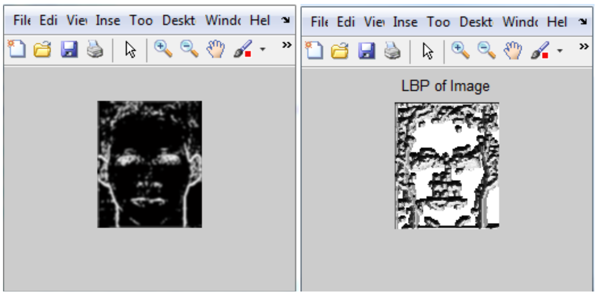


Figure 14: Preprocessed image and LBP generated image

(b) Discrete Wavelet Transform

This transformation gives information of frequency and time locality which is used to extract face image features effectively [25]. The DWT decomposes an image into LL, LH, HH and HL .The LL i.e., low frequency band in both horizontal and vertical direction has significant information of an image. The detailed insignificant information of an image is present in LH, HL and HH bands.

(c) Self Organizing Map

The SOM is a kind of unsupervised learning Artificial Neural Network (ANN) which is used for image compression and classification [26]. The memory is reduced and speeds up operation based on the number of features.

Each sample is treated as an input vector in the input which consists of number of samples. The number of neurons in the hidden layer is specified by the user. Every neuron in the hidden layer is connected with every input neuron and also with the every output neuron. The random weight is assigned to the every hidden neuron and the dimension of weight vector is same as input vector. It is then compared with the input vector. Euclidean distance is used in comparison and is calculated between the input vector and the hidden neuron weight. The similar distances forming input vectors are considered as one class. In order to obtain different classes all the input vectors are compared with the every hidden neuron weight. This method is called training phase and for different set of input samples the SOM is trained.

The number of neurons available in the hidden layer indicates the dimension of the SOM and the block diagram is shown in Figure 15. The dimension PXQ is the input matrix to the SOM and dimension of hidden neurons is NXN. The input has Q samples, in each sample, P elements are available that constitutes a vector given as input to SOM, and then the SOM will give two outputs classes and weights. The class indicates the position of winning neuron; weights represent the weight vector of respective hidden neurons. The classes has dimension of 1x Q and weights has the dimension of $N^2 \times P$.

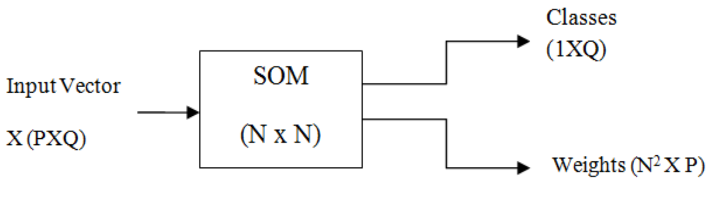


Figure 15: Example of SOM

(d) Matching Unit

The database images features are compared with test image features by using Euclidian distance (ED) using equation (4).

$$ED = \sqrt{\sum_{i=1}^{N} |(D_i - T_i)|^2} \quad \text{.......} \quad (4)$$

Where, N = The total Number of feature

D_i = The database images feature coefficient values

T_i = The test image feature coefficient values

V. Performance Analysis of Proposed Reversible Multiplier

In this section, Performance Evaluation, performance comparison and simulation results of proposed multiplier are discussed.

5.1 Performance Evaluation of proposed multiplier

The performance metrics such as garbage values, constants, number of gates used in reversible logic and quantum cost for various reversible logic designs are given in Table 3. The reversible logic designs shift left by 1, 2 and 3 use reversible PG gates 5, 6 and 7 respectively. The 4:1 MUX and 8:1 MUX use 3 and 7 reversible FRG gates respectively.

Table 3: Performance metrics for reversible logic designs used in proposed MUX based Vedic multipliers

Reversible logic designs	Garbage values	Constants	Number of gates used	Quantum cost
Shift left by 1	2	3	5	(PG)5x4=20
Shift left by 2	2	4	6	(PG)6x4=24
Shift left by 3	2	4	7	(PG)7x4=28
Mux16:1	19	0	15	(FRG)15x5=75
8-bit adder	15	8	6	(HNG)7x6+(PG)1x4=46

5.2 performance comparison of proposed multiplier

The power comparison for irreversible and reversible multiplier is shown in Table 4. The leakage, dynamic and total power for conventional and reversible logic 4 x 4 multipliers are computed using cadence 180 nm technology. It is observed that the power dissipation is more in the case of reversible logic multipliers compared to conventional multipliers. The proposed 4 x 4 multiplier uses seven shift left by 1, nine shift left by 2, eight shift left by 3, 16:1 MUX and eleven full adders. The total number of reversible logic gates used to implement is 473. The number of gates used in proposed reversible logic multiplier is high compared to conventional multiplier; hence the power dissipation is more in the proposed multiplier.

Table 4: Comparison of power for 4x4 irreversible (conventional) and reversible multiplier.

4x4 multiplier	Leakage power (nW)	Dynamic power(nW)	Total power(nW)
Reversible logic	231.360	223540.849	223772.208
Conventional	150.362	164106.658	164256.946

The performance parameters such as path delay, logic delay and route delay are computed for proposed multiplier using XC3S500E device and the parameter values are compared with the existing reversible logic multiplier presented by Koti Lakshmi et al., [27]. The delays of the proposed multipliers with dimension varies from 4x4 to 32x32 are tabulated in Table 5. The delays of the proposed multipliers are less compared to existing multipliers. The limitation of proposed method in power consumption is compensated by various delays.

Table 5: Comparison of proposed Multipliers with the existing reversible multiplier

	4x4 multiplier		8x8 multiplier		16x16 multiplier		32x32 multiplier	
Device:XC3S500E	proposed	existing	proposed	existing	proposed	existing	proposed	existing
Path delay(ns)	11.953	15.36	21.636	25.54	41.565	49.101	77.658	87.587
Logic delay(ns)	8.225	10.12	13.733	15.75	24.137	28.426	43.443	50.25
Route delay(ns)	3.728	5.24	7.903	9.78	17.428	20.625	34.215	40.43

5.3 Simulation Results of proposed multiplier

The simulations are carried out using Xilinx 14.5 and synthesized for Family Spartan 3, device XC3S500E and package CP132 with the speed -5. The simulation result of the 8x8, 16x16 proposed multiplier using reversible logic are obtained.

The simulation result of the 32x32 proposed multiplier using reversible logic is shown in Figure 16. The two decimal numbers say 8388607 and 122227651 are considered and assigned to a [31:0] and b [31:0] to test the multiplier. The multiplication of two numbers resulted into 1025319728772157.

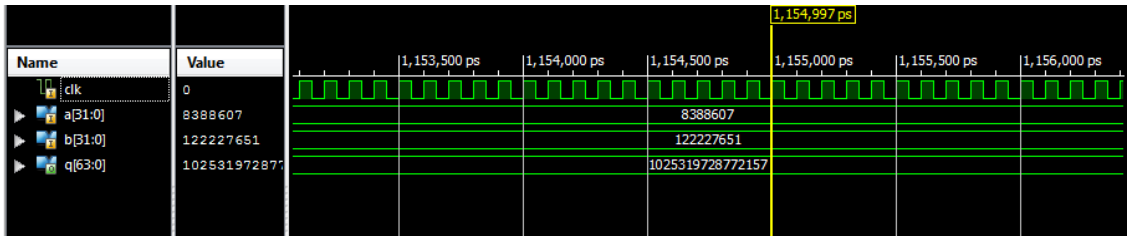


Figure 16: Simulation result of 32x32 proposed multiplier

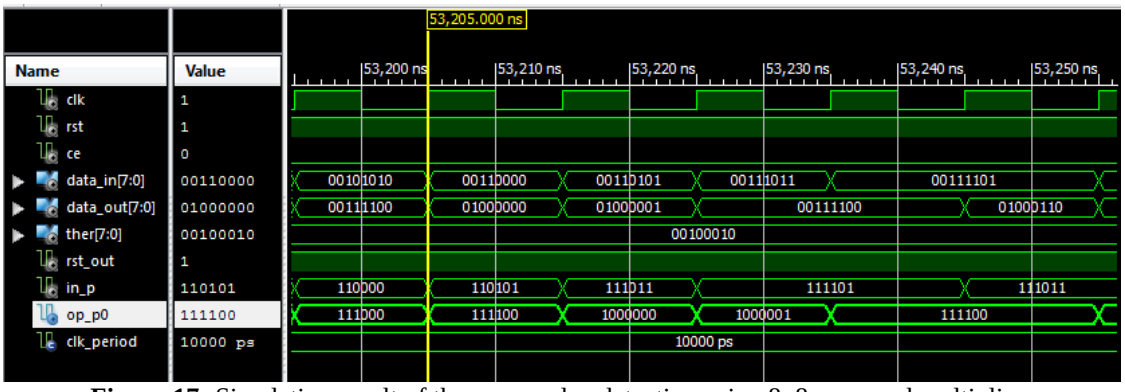


Figure 17: Simulation result of the canny edge detection using 8x8 proposed multiplier

The simulation result of the canny edge detection using proposed multiplier is shown in Figure 17. The text file of the image is fed as input to the canny edge detection. The data in [7:0] represents the input pixel values. The 3x3 non-overlapping image pixel values are multiplied with the 3x3 gradient in x-direction i.e., Gx. The obtained values in the image gradient in x-direction will be added to get a single value. The similar procedure is followed to obtain the image gradient in y- direction using the gradient in y direction i.e., Gy. In order to obtain gradient magnitude, the image gradient in x and y-direction are added. The magnitude is compared is compared with the threshold. The threshold value is set by trial and error. If the magnitude value is less than threshold it is sent as zero and if it is more than threshold then the pixel values are sent as it is to the output.

VI. Performance Analysis of Face Recognition Using Proposed Multiplier

In this section, performance evaluation and the comparisons of proposed method with the existing methods are discussed.

6.1 Performance Evaluation

6.1.1 ORL Face database

In order to test the proposed algorithm for different combinations of Persons outside Database (POD) and the Persons Inside Database (PID) are considered. Figure 18 shows the variations of FRR, FAR and TSR for PID: POD of 30:10. The variations of FRR and TSR decreases with increasing threshold, whereas FAR increases with increase in threshold for all combinations of PID and POD.

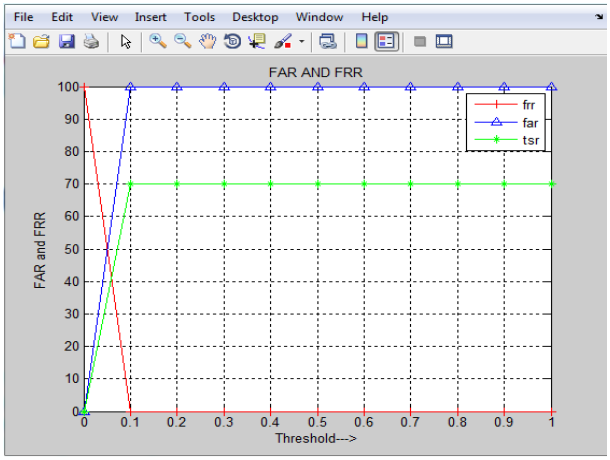


Figure 18: Variations of FRR, FAR and TSR for PID: POD, 30:10

The variations of performance parameter such as EER, Opt. TSR and Max.TSR for different combination of PID and POD for ORL face database are given in Table 6. It is observed that the percentage optimum TSR values decreases with increase in PID values, whereas the EER values are constant.

Table 6: Variations of performance parameters for different combinations of PID and POD

PID	POD	Opt. TSR	EER	Max. TSR
10	30	50	0.5	100
20	20	45	0.5	85
30	10	39	0.5	70

6.1.2 Indian Male Database

The different combination of PID and POD are used to test proposed method. Figure 19 shows Variations of FRR, FAR and TSR for PID: POD of 2:18. The FRR and TSR values decreases, whereas FAR increases with threshold. The EER value is 0.32 for PID and POD combination of 2 and 18, whereas EER value is 0.44 for all other combinations of PID and POD.

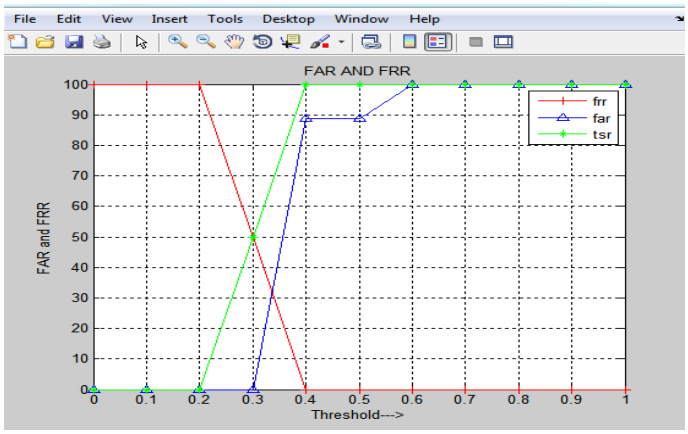


Figure 19: Variations of FRR, FAR and TSR for PID: POD, 2:18

The percentage maximum TSR, optimum TSR and EER values for different combinations of PID and POD are given in Table 7. It is observed that, the percentage TSR values decreases with the increase in PID values. The value of EER obtained increases and then remains constant.

Table 7: Variations of performance parameters for different combinations of PID and POD

PID	POD	EER	%Opt.TSR	%Max.TSR
2	18	0.32	70	100
5	15	0.44	49	80
10	10	0.44	39	60
15	5	0.44	44	60

6.1. 3 Indian female database

The different combination of PID and POD are used to test proposed method. Figure 20 shows the variations of FRR, FAR and TSR for PID: POD of 2:20.

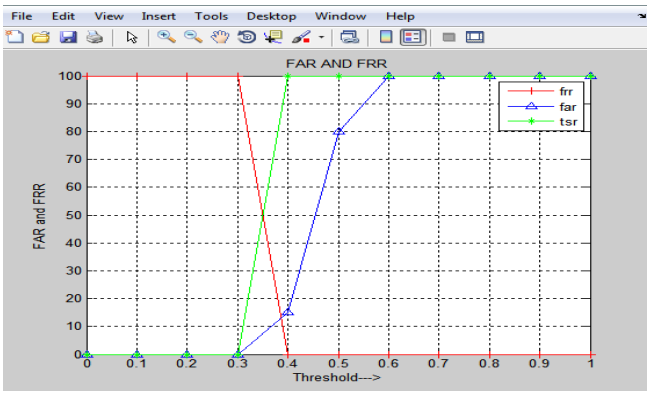


Figure 20: Variations of FRR, FAR and TSR for PID: POD, 2:20

The percentage values of maximum and optimum TSR values along with EER values for different combinations of PID and POD are given in Table 8. It is observed that the maximum TSR of 100% is obtained for PID values between 2 and 8 and POD values of 20 and 14. The average value of optimum TSR is around 75% for all combinations of PID and POD.

Table 8: Variations of performance parameters for different combinations of PID and POD

PID	POD	EER	%Opt.TSR	%Max.TSR
2	20	0.12	70	100
6	16	0.19	80	100
8	14	0.27	71	100
10	12	0.21	65	80
12	10	0.28	72	83.33

6.1.4 NIR database

The percentage TSR, FRR and FAR are computed for different combinations of PID and POD using NIR face database to test the proposed face recognition method. The variations of performance parameters for different combinations of PID and POD. Figure 21 shows the variations of FRR, FAR and TSR for PID: POD of 5:15.

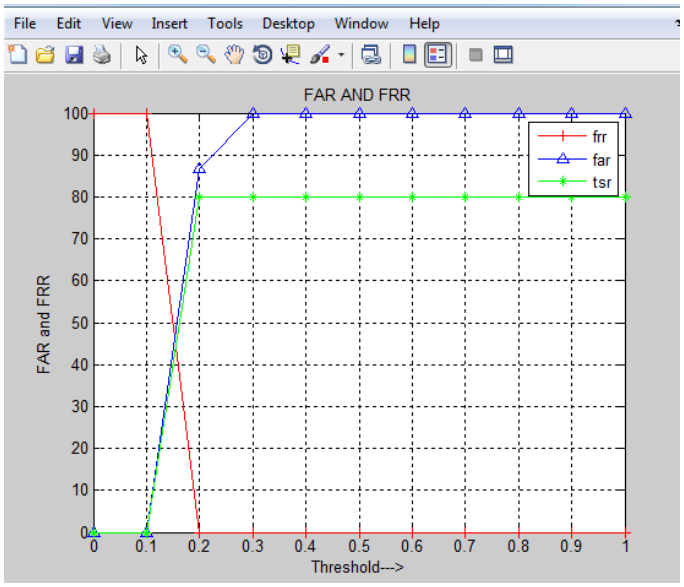


Figure 21: Variations of FRR, FAR and TSR for PID: POD, 5:15

The percentage values of maximum and optimum TSR values along with EER values for different combinations of PID and POD are given in Table 9. It is observed that the values of TSR and FRR decreases with threshold, whereas FAR increases with the threshold. The values of EER are 0, 0.45, 0.39, 0.48 and 0.37 are obtained for PID and POD combinations of 2:38, 5:15, 10:30, 20:20 and 30:10 respectively. The percentage maximum and optimum TSR values decreases with increase in PID values.

Table 9: Variations of performance parameters for different combinations of PID and POD

PID	POD	EER	%Opt.TSR	%Max.TSR
2	38	0	100	100
5	15	0.45	45	80
10	30	0.39	55	70
20	20	0.48	52	70
30	10	0.37	37	48

6.1.5 Yale database

The variations of performance parameters for different combinations of PID: POD. Figure 22 shows the variations of FRR, FAR and TSR for PID: POD of 5:10.

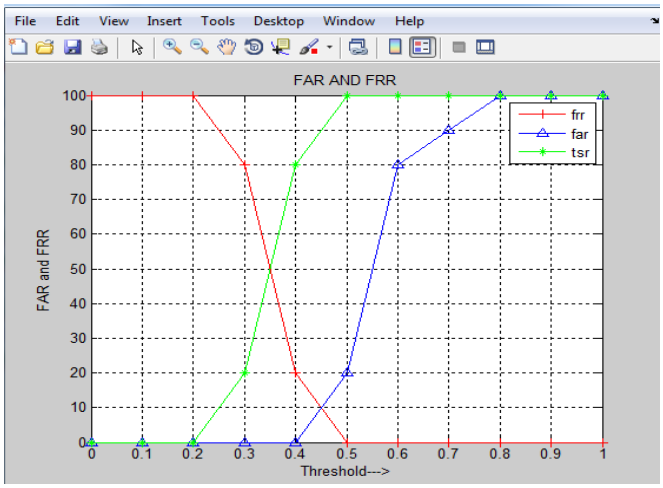


Figure 22: Variations of FRR, FAR and TSR for PID: POD, 5:10

The percentage maximum TSR, optimum TSR and EER values for different combinations of PID and POD are given in the Table 10. It is observed that the percentage maximum and optimum TSR values decreases with increase in PID. The peak values of maximum and optimum TSR values are 100 % and 90 % respectively.

Table 10: Variations of performance parameters for different combinations of PID and POD

PID	POD	EER	%Opt.TSR	%Max.TSR
5	10	0.1	90	100
7	8	0.19	80	100
8	7	0.28	72	100
10	5	0.28	75	90
12	3	0.26	75	91.667

6.2 Comparison of proposed method with existing method

The percentage recognition rate of proposed method is compared with existing methods using YALE and ORL face databases. The percentage recognition rate using YALE face database of proposed method is compared with existing methods presented by Ganesh Linge and Meenakshi Pawar [28], Ripal Patel et al., [29], Azam et al., [30] and Jing and Zhang [31], is given in the Table 11. It is observed that, the recognition rate is high in the case of proposed method compared to existing methods.

The percentage recognition rate using ORL face database of proposed method is compared with existing methods presented by Ramesh and Raja [32] and Gupta and George [33], is given in Table 12. The recognition rate of proposed method is high compared to existing methods.

Table 11: Comparison of Proposed method with the existing methods for YALE Data Base

Authors	% Recognition Rate
Ganesh Linge and Meenakashi Pawar [28]	98.7879
Ripal Patel, et al.,[29]	75
M. Azam, et al., [30]	92.77
X. Y. Jing and Zhang [31]	90.14
Proposed	100

Table 12: Comparing the existing methods with the proposed methods for ORL Database

Authors	% Recognition Rate
K. Ramesha and Raja [32]	83.30
P. Gupta and George [33]	88.75
Proposed	100

The novel concepts introduced in the face recognition are as follows for better performance.

1. Two images of single person are converted into a single image to reduce total number of images per person to around 50% by introducing steganography concept.
2. The new multiplier for edge detection of face images is designed using Reversible Logic gates, MUX and Vedic multiplication concept.

3. The LL coefficients and LBP coefficients are combined using arithmetic addition to generate initial set of features.
4. The final set of features is generated from the output of SOM for initial feature input.

Advantages of proposed method

1. The total numbers of face images per person are reduced to fifty percent by using steganography concept.
2. The path delay, logic delay and route delays are less in the proposed multiplier compared to the existing multiplier. The MUX output used as multiplication result, than computing direct multiplication, which results in less delay.
3. The three types of compression techniques such as steganography, DWT and SOM are used to increase the speed of computation.
4. The algorithm may be implemented using hardware for real time applications, since algorithm is compressed.

VII. Conclusion

The face image is a physiological biometrics used to identify a person for variety of applications. The novel concept of converting two face images of a person into single image using steganography is introduced. The multiplier for edge detection of face image is designed based on the new concept techniques of reversible logic, MUX and Vedic multiplication. The resize of face images and Gaussian filter are used in preprocessing unit. The coefficient of DWT and LBP of face images are fused and applied to SOM input. The final features are obtained from the output of SOM. The final features of face database and test face images are compared using ED to compute performance parameters. It is observed that the performance parameters of proposed method are better compared to existing methods. In future, SOM may be replaced by Support Vector Machine (SVM) and implemented on hardware for real time testing.

References

[1] Himanshu Thapliyal and M.B Srinivas, *"*Novel Reversible Multiplier Architecture Using Reversible TSG Gate*", IEEE International Conference on Computer Systems and Applications, pp.100 - 103, 2006.*

[2] Nidhi Pokhriyal, Harsimranjit Kaur and Neelam Rup Prakash, "Compressor Based Area-Efficient Low-Power 8x8 Vedic Multiplier", *International Journal of Engineering Research and Applications, Vol. 3, Issue 6*, pp.1469-1472, 2013.

[3] Maryam Ehsanpour, Payman Moallem and Abbas Vafaei, "Design of a Novel Reversible Multiplier Circuit using Modified Full Adder", *IEEE International Conference on Computer Design and Applications,* Vol. 3, pp. 230-234, 2010.

[4] Madhusmita Mahapatro, Sisira Kanta Panda, Jagannath Satpathy, Meraj Saheel , M.Suresh, Ajit Kumar Panda and M K Sukla, "Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation" *International Symposium on Electronic System Design*, pp. 85 - 90, 2010.

[5] Anindita Banerjee and Anirban Pathak, "Reversible Multiplier Circuit" *Third International Conference on Emerging Trends in Engineering and Technology.* pp.781-786, 2010.

[6] M. Jenath and V. Nagarajan **"**FPGA Implementation on Reversible Floating Point Multiplier **"**, *International Journal of Soft Computing and Engineering, Vol.2, Issue-1,* pp. 438-443, 2012.

[7] Kartikeya Bhardwaj and Bharat M. Deshpande, "K-Algorithm: An Improved Booth's Recoding for Optimal Fault-Tolerant Reversible Multiplier", *IEEE International Conference on VLSI Design*, pp. 362-367, 2013.

[8] Pradip Panchal, Palak Patel,Vandit Thakkar and Rachna Gupta, "Pose, illumination and expression invariant face recognition using Laplacian of Gaussian and Local Binary Pattern", 5th Nirma University, *IEEE International Conference on Engineering (NUiCONE)*, pp. 1-6, 2015.

[9] Bilel Ameur, Sabeur Masmoudi, Amira Guidara Derbel,and Ahmed Ben Hamida "Fusing Gabor and LBP feature sets for KNN and SRC-based face recognition", *2nd IEEE International Conference on Advanced Technologies for Signal and Image Processing (ATSIP),* pp 453 - 458, 2016.

[10] Paitoon Yodkhad, Aram Kawewong and Karn Patanukhom "Approximate nearest neighbor search using self-organizing map clustering for face recognition system", *IEEE International Conference on Computer Science and Engineering Conference (ICSEC*), International , pp 151 - 156, 2014

[11] Vojtech Jirka, Matej Feder, Jarmila Pavlovicova and Milos Oravec "Face recognition system with automatic training samples selection usingself-organizing map", *IEEE Proceedings ELMAR,* pp. 1 - 4, 2014.

[12] Amir Benzaoui, Abdelhani Boukrouche, Hakim Doghmane and Houcine Bourouba "Face recognition using 1DLBP, DWT and SVM", *3rd IEEE International Conference on Control Engineering & Information Technology (CEIT*), pp. 1-6 , 2015.

[13] Swati Jadon, Mahendra Kumar and Yogesh Rathi "Face recognition using Som Neural Network with Ddct facial feature extraction techniques", *IEEE International Conference on Communications and Signal Processing (ICCSP),* pp.1070 – 1074, 2015.

[14] S Bhairannawar , Raja K B, Venugopal K R and L M Patnaik, " Efficient FPGA Based Matrix Multiplication Using Mux and Vedic Multiplier", *International Journal of Computers & Technology,* Vol. 12, No. 5, pp. 3452-3463, 2014.

[15] Rakshith Saligram, Shrihari Shridhar Hegde, Shashidhar A Kulkarni, H R Bhagyalakshmi and M K Venkatesha, "Design of Fault Tolerant Reversible Multiplexer based Multi-Boolean Function Generator using Parity Preserving Gates" *International Journal of Computer Applications, Vol.66, No.19*, pp. 20-24, 2013.

[16] R. Anitha, Neha Deshmukh, Sarat Kumar Sahoo, S. Prabhakar Karthikeyan "A 32 bit MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate" IEEE *International Conference on Circuit, Power and Computing Technologies [ICCPCT],* pp. 1-6, 2015.

[17] The ORL database, http://www.cam-orl.co.uk

[18] Indian Face Database, http://viswww.cs.umass.edu/~vidit/Indian Face Database.

[19] The NIR database, http://www.cbsr.ia.ac.cn/english/NIR-VIS-2.0-Database.html

[20] Yale database, http://vision.ucsd.edu/content/yale-face-database.
[21] KB Raja, CR Chowdary, KR Venugopal and LM Patnaik, *"*A Secure Image Steganography using LSB, DCT and Compression Techniques on Raw Images*", IEEE 3rd International Conference on Intelligent Sensing and Information Processing*, pp. 170-176, 2005.
[22] Raman Maini & Dr. Himanshu Aggarwal,"Study and Comparison of Various Image Edge Detection Techniques", *International Journal of Image Processing (IJIP), Vol. 3*, pp.1-12, 2009.
[23] Sateesh Kumar H.C., Sayantam Sarkar, Satish S Bhairannawar, Raja K.B. and Venugopal K.R, "FPGA Implementation of Moving Object and Face Detection using Adaptive Threshold", *International Journal of VLSI design & Communication Systems (VLSICS) Vol.6, No.5*, pp. 15-35, 2015.
[24] Tojala, M. Pietikainen and D. Harwood "Performance Evaluation of Texture measured with classification based on Kullback discrimination of distributions", *12th IAPR IC on Pattern Recognition, Vol. 1*, pp 582-585, 1994.
[25] Sujatha BM, Chetan Tippanna Madiwalar, Suresh Babu K, Raja K B, and Venugopal KR, "*Compression Based Face Recognition using DWT and SVM"* Signal & Image Processing : An International Journal (SIPIJ) Vol.7, No.3, pp.45-62, 2016.
[26] W. Zhao, R. Chellappa, P. J. Phillips, and A. Rosenfeld, "Face recognition: a literature survey," *ACM Computing Surveys, vol. 35*, pp. 399–458, 2003.
[27] P. Koti Lakshmi, B Santhosh Kumar and Prof.Rameshwar Rao," Implementation of Vedic Multiplier Using Reversible Gates" *Computer Science & Information Technology (CS & IT)*, pp. 125–134, 2015.
[28] Ganesh Linge and Meenakshi Pawar, "Neural Network Based Face Recognition Using PCA", *International Journal of Computer Science and Information Technologies, Vol. 5, Issue 3*, pp. 4011-4014, 2014.
[29] Ripal Patel , Nidhi Rathod , Ami Shah and Mayur Sevak, "Face Recognition using Eye Distance and PCA Approaches" *International Journal of Computer Science and Information Technologies, Vol. 5, Issue 1*, pp. 84-87, 2014.
[30] M. Azam, M. A. Anjum and M. Y. Javed, "Discrete Cosine Transform based Face Recognition in Hexagonal Images", *IEEE International Conference on Computer and Automation Engineering (ICCAE), vol. 2*, pp. 474-479, 2010.
[31] X. Y. Jing and D. Zhang, "A Face and Palm print Recognition Approach Based on Discriminant DCT Feature Extraction", *IEEE transactions on systems, man, and cybernetics. Part B, Cybernetics, vol. 34, No. 6*, pp. 2405-2415, 2004.
[32] K. Ramesha, and K. B. Raja, "Dual Transform based Feature Extraction for Face Recognition", *International Journal of Computer Science Issues, vol. 8, Issue 5, No. 2*, pp.115-124, 2011.
[33] P. Gupta and N. V. George, "An Improved Face Recognition Scheme using Transform Domain Features", *International Conference on Signal Processing and Integrated Networks*, pp. 82-84, 2014.