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Energy Aware IP Shifter for DSP Processors using MTD^{3}L Asynchronous Approach

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Abstract: *The purpose of the paper is to design the shifter by using different asynchronous logics to optimize the power dissipation and better performance. Power dissipation is a most important consideration as performance and area of Very Large Scale Integration (VLSI) design. The shifter in a digital circuit is frequently utilized by embedded digital signal processors and ALU of microprocessors to manipulate data. This paper explores design for the shifter to perform 1-bit right shift operation. The architecture of shifter is designed by a sequence of multiplexers (2:1 MUX) and in such an implementation the output of a MUX is connected to the input of the next MUX. The shifter was implemented in two different clock-less logics which are Multi-Threshold Null Conventional Logic (MTNCL) and proposed Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L). All the simulations are done in Mentor Graphics tool. In this paper, we present a comparative study of various parameters like delay, power and energy savings. The proposed logic of shifter implementation shows better performance.*

Keywords: *Intermediate product shifter, clockless logic, 2:1 MUX, dual spacer, dual rail.*

I. Introduction

Reduction of power dissipation and attaining best performance in Very Large Scale Integration (VLSI) design has become an interesting research area. In CMOS circuits, energy consumption is directly proportional to the supply voltage. If we use low supply voltage, then the energy consumption can be reduced and dissipates less power. The best performance or metric levels of power delay product provide in asynchronous (clockless) design. So, the intermediate product shifter was implemented in various asynchronous designs [1].

The shifter is a basic and logic component that performs 1-bit right shift or left shift operation. It has essential elements in the design of data paths for Digital Signal Processors and general purpose processors. The architecture of shifter is designed by using a sequence of multiplexers (2:1 MUX). The implementation of a shifter is designed by connecting the output of one multiplexer to the input of next multiplexer. The shifter is designed to shift the data bits arithmetically or logically (shift right or shift left). In a left shift operation, the specified number of a data bit is shifted to the left side and the results of least significant bits are placed with zeros. In right shift operation, the specified number of a data bit is shifted to the right side and results of most significant bits are placed with zeros.

The shifter in a digital circuit which can be designed with the help of asynchronous logics (each single bits acts as a dual rail). Mostly asynchronous design is used because it provides low power consumption, less Electro-Magnetic Interference (EMI), high robustness compared to the clocked circuits (synchronous logic) [2]. This paper deals with the two asynchronous logics which are Multi-Threshold Null Convention Logic (MTNCL) and proposed Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L) [3,4]. The basic component to design the shifter architecture is 2:1 MUX.

1.1 Basic 2:1 Multiplexer

A 2:1 multiplexer is a device that selects one of the two digital inputs and gives the selected input through the single line i.e., output signal. For 2:1 MUX, there are 2 inputs and 1 output with respect to a single selected line. A multiplexer is mainly used to increase the amount of data bits within a certain amount of time period. So, it is also called as "data selector". Let us consider the block diagram of 2:1 MUX as shown in Figure-1. Table-1 shows the truth table of 2:1 MUX.

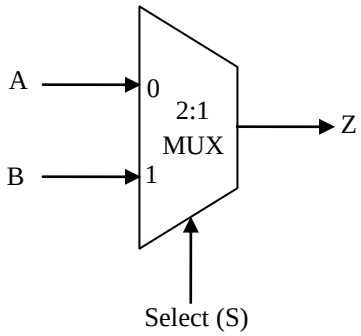

Fig.1: Architecture of 2:1 Multiplexer

The Boolean expression for the 2:1 Multiplexer is

$$Z = A\bar{S} + BS$$

Table 1: Truth table of 2:1 Multiplexer

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

II. Literature Review

2.1 Design of Asynchronous Logics

This paper deals with some asynchronous logics which are Multi-Threshold Null Convention Logic (MTNCL) and proposed Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L) [5]. To design the intermediate product shifter, we require 2:1 multiplexer. The multiplexer was implemented with some threshold gates of 27 fundamental gates. In this clockless circuits, each data bits acts as a dual rail. Let consider the implementation of 2:1 Multiplexer in clock-less logics.

2.1.1 Multiplexer

A multiplexer is a device which selects any one of inputs and forwarded to a single line (output) with respect to the select line. The 2:1 MUX consists two inputs (A and B), one output (Z) and one select bit (S). In asynchronous logics, each single input and output acts as a dual (A_0,B_0,S_0,Z_0,A_1,B_1,S_1,Z_1) as shown in Figure-2. Table-2 shows the truth table for all the possibilities of 2:1 MUX. To design the MUX in clockless circuits, three threshold gates are required out of 27 fundamental gates which are TH_{and0x0}, $TH_{24comp0}$, TH_{22}.

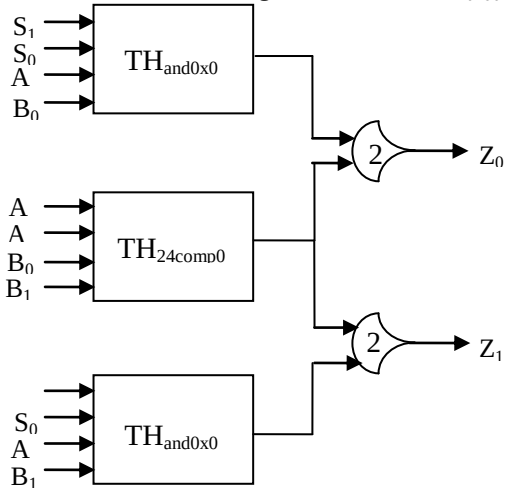

Fig.2: Design of 2:1 MUX

Table 2: Truth table of 2:1 Multiplexer in dual rail

S		A		B		Z	
S_0	S_1	A_0	A_1	B_0	B_1	Z_0	Z_1
1	0	1	0	1	0	1	0
1	0	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	0	1	0	1	0	1
0	1	1	0	1	0	1	0
0	1	1	0	0	1	0	1
0	1	0	1	1	0	1	0
0	1	0	1	0	1	0	1

2.1.2 Multi-Threshold Null Convention Logic

The MTNCL logic is a combination of basic Null Convention Logic (NCL) and Multi-Threshold Complementary Metal Oxide Semiconductor (MTCMOS).The basic NCL logic consists of SET, RESET blocks for circuit operation and $Hold_0$, $Hold_1$ blocks for state holding capacity. The basic MTCMOS circuit will operate with the sleep signal. Figure-3 shows the block diagram of MTNCL with the combination of NCL and MTCMOS [6,7]. The circuit of MTNCL consists only $Hold_0$ and SET blocks with few high V_{th} transistor. By using high V_{th} and low V_{th} transistors in the circuit, it overcomes the leakage problem and gives the best performance.

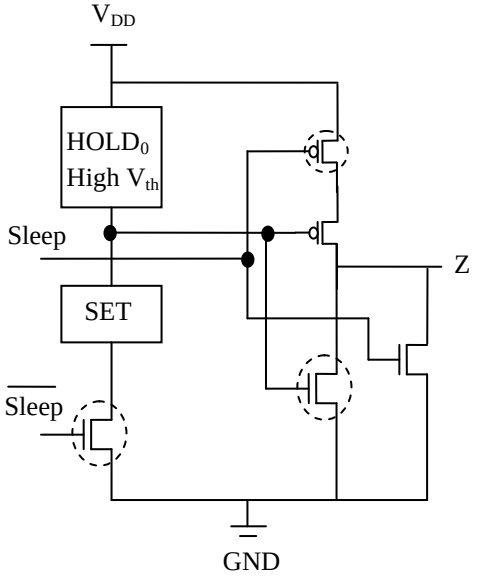

Fig.3: Block diagram of MTNCL

III. Proposed Work

3.1 Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic

The MTD^3L is the combination of basic Dual Spacer Dual Rail Delay Insensitive Logic (D^3L) and Multi-Threshold Null Convention Logic (MTNCL) [8]. The block diagram is similar to MTNCL design but the additional sleep signal is required to this logic. The MTD^3L circuit will control by the pair of the two sleep signals (sleep-to-0 and sleep-to-1) as shown in Figure-4. Table-3 represents the operation of a circuit with respect to sleep signals [9]. When the two sleep signals are de-asserted (low), then the circuit will operate in normal condition. If either of the sleep signals is asserted (high), then the circuit will respond to the appropriate sleep value (All one spacer or All zero spacer). If the two sleep signals are asserted, then the output will don't changes the state (previous state as output). The circuit consists only two sleep signals (sleep to 0 signal and negation of sleep to 1 signal).

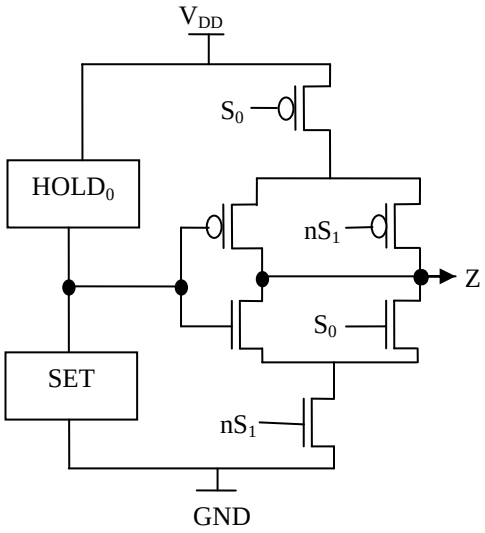

Fig.4: Block diagram of MTD^{3}L

Table 3: MTD^{3}L Sleep signals

Sleep		Output
S0	S1	
0	0	Normal operation
0	1	All-One Spacer
1	0	All-Zero Spacer
1	1	Invalid

IV. Intermediate Product Shifter

The shifter is constructed by cascading the 2:1 MUX in a series. This paper deals with the combination of multiplexers block in series for 47-bit intermediate product shifter [10,11]. The shifter operates with a 1-bit right shift, then the most significant bits are filled with zeros. The main circuit block for the shifter is build based on the multiplexers circuit as shown in Figure-5 [12,13].

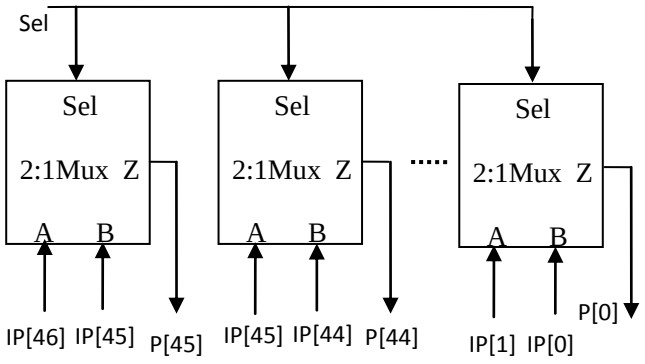

Fig.5: Design of 46-bit Intermediate product shifter

The intermediate product shifter is implemented in two asynchronous logics (MTNCL and MTD^{3}L) as shown in Figure-6 and Figure-7.

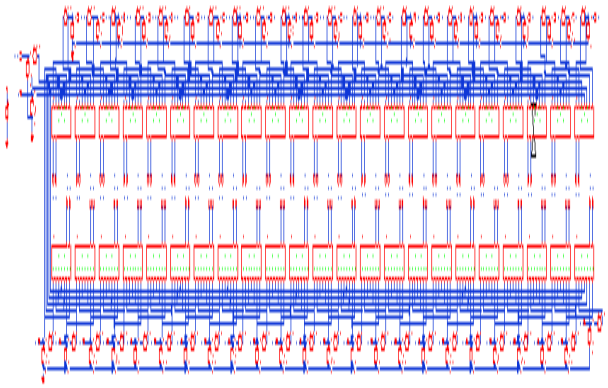

Fig.6: Schematic design of Intermediate product shifter using MTNCL Logic

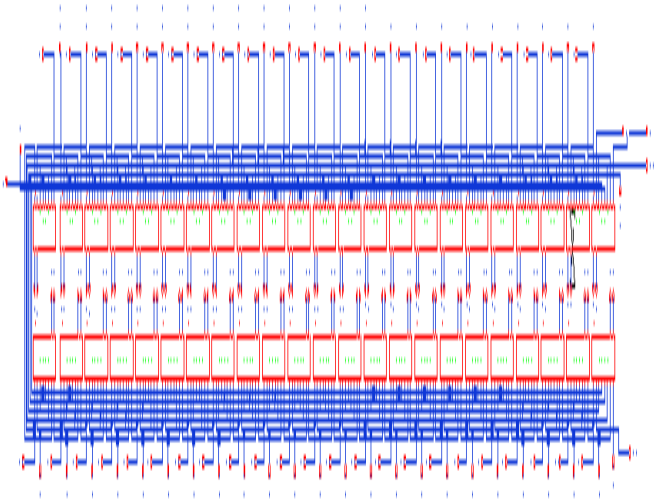

Fig.7: Schematic design of Intermediate product shifter using MTD^{3}L

The schematic of IP shifter has 47 inputs and provides 46 outputs with respect to the select line [14]. If the select bit leads to 1, then the outputs will shifts to 1-bit right side with respect to the input. The shifting process is nothing but an increment process. If the select bit is 0, then the output remains unchanged (no need of shift operation). The asynchronous logics (MTNCL and MTD^{3}L) were implemented with dual rail and dual spacer for each single data bit as shown in the schematic diagrams [15,16]. The Intermediate product shifter is mostly used in many applications like Floating Point Multiplier. In Floating point multiplier IP shifter is used to normalize the Mantissa output bits.

V. Results and Discussions

This work has been developed with Mentor Graphics tool (Pyxis product) with 130nm technology. The simulation results (output waveforms of a single rail) for the Intermediate product shifter using the two asynchronous techniques (MTNCL and MTD^{3}L) as shown in Figure-8 and Figure-9. The Figures shows some of the output bits (LSB) with sleep signals and select signal.

Input bit pattern = 00010100101001010001001010010

Output bit pattern

(i) For Select=0, Z= 00010100101001010001001010010

(ii) For Select=1, Z= 00001010010100101000100101001

Fig.8: Simulated waveforms of IP Shifter using MTNCL

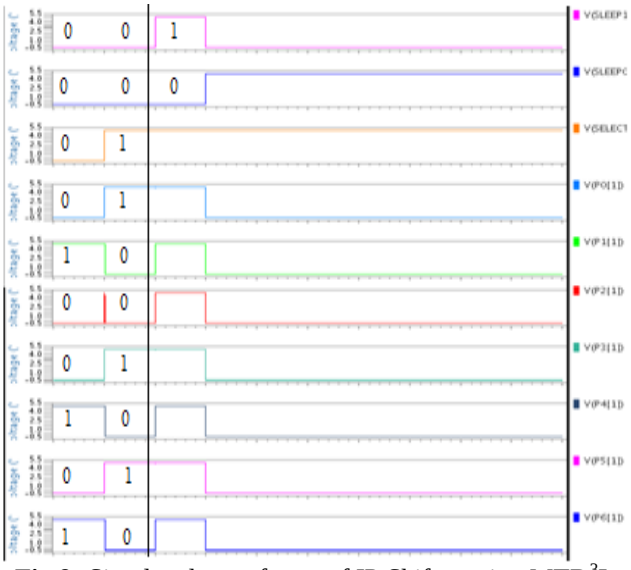

Fig.9: Simulated waveforms of IP Shifter using MTD^{3}L

Table-4 shows the comparison of two asynchronous techniques (MTNCL, MTD^{3}L). The parameters which compared on power dissipation, delay, energy and slew rate.

5.1 Power Dissipation

Power dissipation is one of the main criteria in the VLSI design. Reducing the power dissipation in VLSI design, the circuit will operate without any leakage problem and produce outputs accurately i.e., without any glitches. Average power dissipation in a digital circuit.

$$P_{Average} = P_{Static} + P_{Dynamic}$$

Where $P_{Average}$ is the average power dissipation, P_{Static} is the static power dissipation due to leakage currents and $P_{Dynamic}$ is the dynamic power dissipation due to switching of transistors.

$$\text{Power dissipation} = \propto C_L V_{DD}^2 f$$

5.2 Propagation Delay

Propagation delay or Gate delay is the time required in a digital circuit to transmit from input signal of a logic gate to the output signal. The delay must be reduced to obtain the circuit performance accurately (with high speed). It is given by

$$\text{Tpd} = \frac{\text{Tphl} + \text{Tplh}}{2}$$

5.3 Power-Delay Product

Power Delay Product is the measure of energy and is defined as the product of delay and power to measure the circuit performance. The advantage of increasing the energy is short circuit dissipation (leakages) will minimize. It is given by

$$\text{PDP} = \text{P(Power)} * \text{T(delay)}$$

Units of energy are 'Joules'.

5.4 Slew Rate

Slew rate is defined as the rate of change of voltages per unit time. It is given by

$$\text{SR} \geq 2\pi f V_{pk}$$

Where f is the frequency $(\frac{1}{T})$ and V_{pk} is the peak amplitude of the signal. The high slew rate gives a quicker response, i.e., changes the state of the output with respect to the input, especially at high frequencies. Units of slew rate are $\frac{\text{Volts}}{\text{Sec}}$.

Table 4: Comparision for two asynchronous logics

Parameters	MTNCL	Proposed MTD^{3}L
Power dissipation (u Watts)	1.454	57.949
Delay (n Sec)	99.623	15.10
Energy (n Joule)	14.483	8.75
Slew Rate (G Volt/Sec)	49.701	156.34

VI. Conclusion

The IP Shifter is designed using two asynchronous logics which are MTNCL and MTD^{3}L. Proposed MTD^{3}L gives better performance in terms of delay, % of energy saving and slew rate. With proposed method, we achieved 40% energy saving and 68% of better slew rate. The shifter design may further optimize in terms of all these metrics by using different techniques like LECTOR algorithm, sleepy approach, stack approach, sleepy stack approach and sleepy keeper approach etc., without degradation its functionality.

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