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Low Power Area Efficient VLSI Architectures for Shift Register Using Explicit Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme

[1]B. Sujita ,[2]K. Padma Vasavi
[1]*M.Tech (VLSID) Student, Department of ECE, Sri Vishnu Engineering College for Women, Bhimavaram, India*
[2]*Professor, Department of ECE, Sri Vishnu Engineering College for Women, Bhimavaram, India*

Abstract: *A register that is designed to allow the bits of its contents to be moved to left or right is known to be a shift register. Shift registers may be implemented by using pulsed latches and flip flops.However,shift register implemented by pulsed latches have power and area problems .So, flip flops are preferred over pulsed latches. In this paper, a VLSI architecture for low power area efficient VLSI architectures for shift register using explicit pulse triggered flip flop based on signal feed-through scheme is proposed. The performance of the proposed shift register is compared with that of the shift register implemented by using pulsed latches. From the experiments and the results obtained it is observed that the proposed shift register is having less area and low power when compared to the shift register using pulsed latches with 79.83% and 99.26 % for an N-bit shift register. All the Simulation results,schematic and Layouts are based on CMOS 90nm technology in HSPICE tool,Digital schematic tool (DSCH) and Micro-wind 3.1.*

Keywords: *Flip Flops, Shift Register, Pulse Triggered, HSPICE, DSCH, Micro-wind.*

I. Introduction

A Shift Register is one of the basic building blocks in a VLSI circuit. It is a sequential logic circuit that is used to store N-bits of digital data. They are commonly used in digital filters, communication receivers, image processing applications and in micro-controllers. An N-bit shift register has simple architecture and contains N-flip flops connected in the form of a chain. Therefore, as the word length of the shift register increases the parameters area and power become the point of concern. Recently, pulsed latches have replaced conventional flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. However, the pulsed latch structures suffer from timing hazards and power dissipation. The timing problem could be solved by using multiple non-overlap delayed pulsed clock signals instead of using single pulsed clock signal.In order to overcome the problems mentioned above,the pulsed latches may be replaced by explicit pulse triggered flip flops.This paper evaluates the performance of various explicit pulse triggered flip flops and for their efficiency with respect to power and area.

Generally, shift registers can also be used for serial and parallel data transformation, data computing, data processing.so the study of shift register is of great significance.Several researchers have proposed different types of shift register. In 1996, 1998 and 2004 there were three works related on parallel architecture of linear feedback shift register, first one by M. Lowy [1], second one by M. E. Hamid and C. I. H. Chen [2], and the third one was done by Abdullah. M and Rajendra. K [3] where the power was significantly reduced when compared to the conventional architectures [1], [2] and showed way to generate multiple outputs. Thus, in2006 R. S. Katti, X. Ruan, and Hareesh. K, proposed multiple output low power linear feedback shift register [4].Similarly, many works on low-power CMOS image sensors have been published such as In 2003,one by L. J. Cheng and Y.H.Zhong proposed low power readout shift register[5] and another by X.L. Jin and J. Chen proposed a novel low power quasi-dynamic shift register used as the readout scan circuit[6].But the further reduction of area and power was done by Alexander.F, Vladislav. M, Vitali. L and OrlyY.P by proposing ultra-low-power DFF based shift registers design for CMOS image sensors applications in 2006[7].Recently,conventional flip-flops such as power PC flip flop (PPCFF) are replaced by pulsed latches and Some of the researchers such as B.D. Yanghave designed shift registers using pulsed latches for area and power efficiency in 2015[8].But this area and power can be still reduced when compared to all the previous methods discussed above by simply replacing the latches with the explicit pulse triggered flip flop.

In this paper, implementation of shift register using Explicit Pulse Triggered Flip Flop based on Signal Feed-Through Scheme to obtain low power and less area is presented.

A. Architecture of the shift register using latches

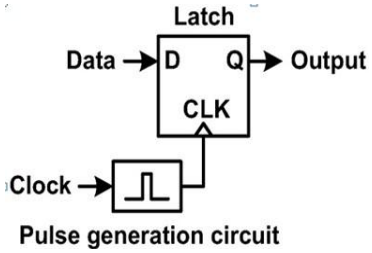

Fig.1: Pulsed latch

The architecture of the shift register using Pulsed latch is shown in Fig.1.It consists of a Pulse generation circuit and a D-latch, A N-bit shift register using pulsed latches is shown in Fig.2.

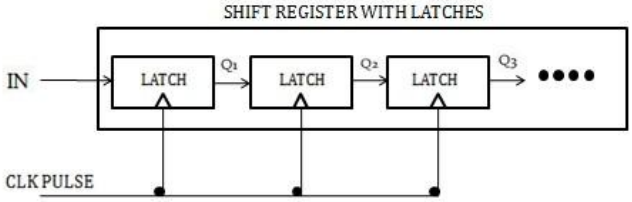

Fig.2: Shift register with latches and a pulsed clock signal.

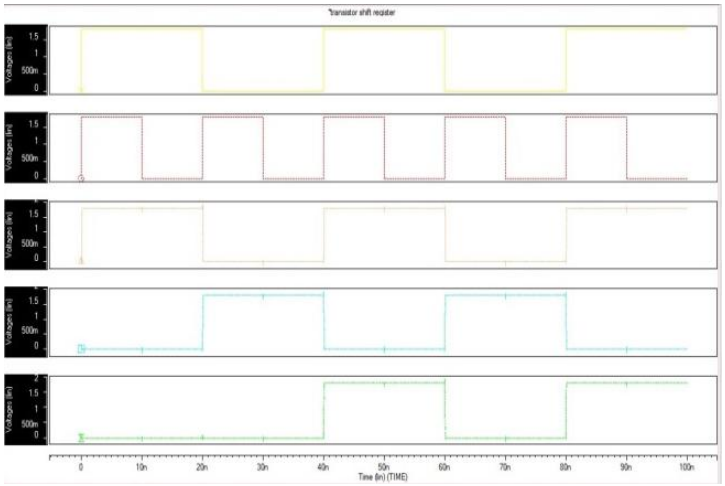

Fig.3: Waveform of Shift register with latches and a pulsed clock signal.

The output obtained from Shift register with latches and a pulsed clock signal shown in Fig.2 is described in Fig.3. From Fig.3,it is observed that the output gets delayed by one-bit because of usage of single clock pulse.Thus, there are two solutions available to overcome the timing problems: use of delay circuits between the latches and use of multiple non–overlap delayed pulsed clock signals instead of using single pulsed clock signal.

Shift register with Latches and Delay Circuits:

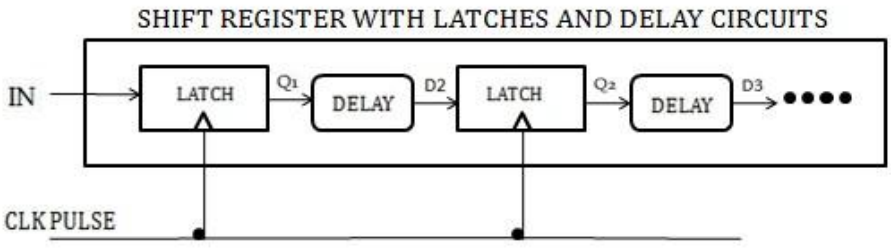

Fig.4: Shift Register with Delay Circuits Inserted Between the Latches

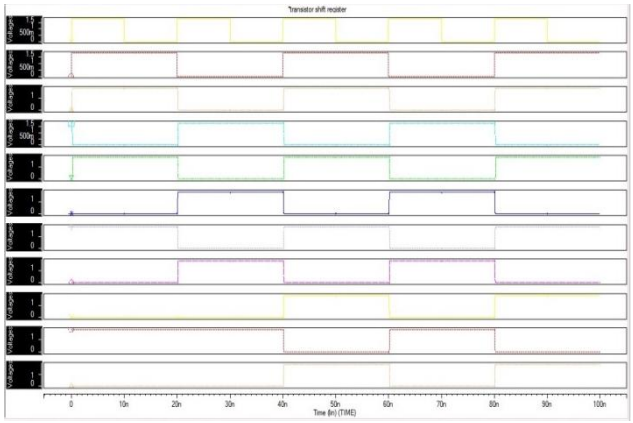

Fig.5: Waveform of shift register with delay circuits inserted between the latches

Thearchitecture of shift register with delay circuits inserted between the latches is shown in Fig.4. The output obtained from this shift register is shown in Fig.5. From Fig.5, it is observed that the timing delay is avoided and the output is obtained at the rising edge of the clock pulse. The output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. But the timing delay is avoided at the cost of area and power overheads.

Shift Register with Latches and Delayed Pulsed Clock Signal:

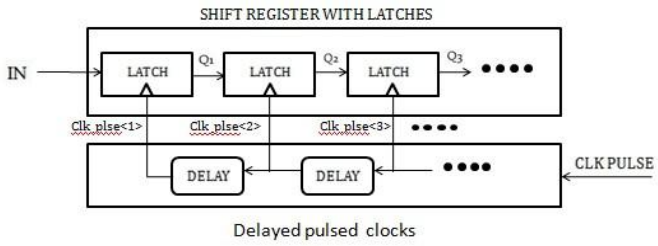

Fig.6: (a)Shift register with latches and a delayed pulsed clock signal

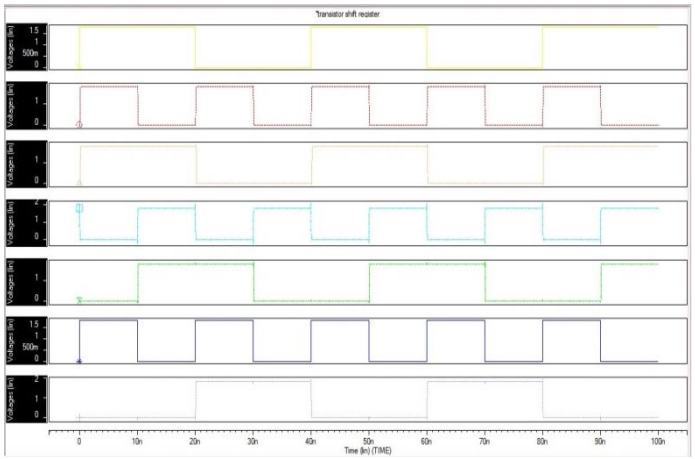

Fig.6: (b) Waveform of Shift register with latches and a delayed pulsed clock signal.

The problem of area and power overhead is reduced by using delayed pulsed clock signals as shown in Fig.6(a). The output of the circuit is shown in Fig.6(b).The delayed pulsed clock signal can be obtained by passing the pulsed clock signals through the delay circuits. In this each latch requires a clock pulse signal which is delayed from the pulsed clock signals that is used in the next latch. Here, each latch updates the data only when its next latch updates the data. Thus, no timing problem occurs between the latches.

Using the above two methods the timing problem is eliminated. Hence a shift register using pulsed latches can be implemented. The architecture of shift register using pulsed latches is shown in Fig.7.

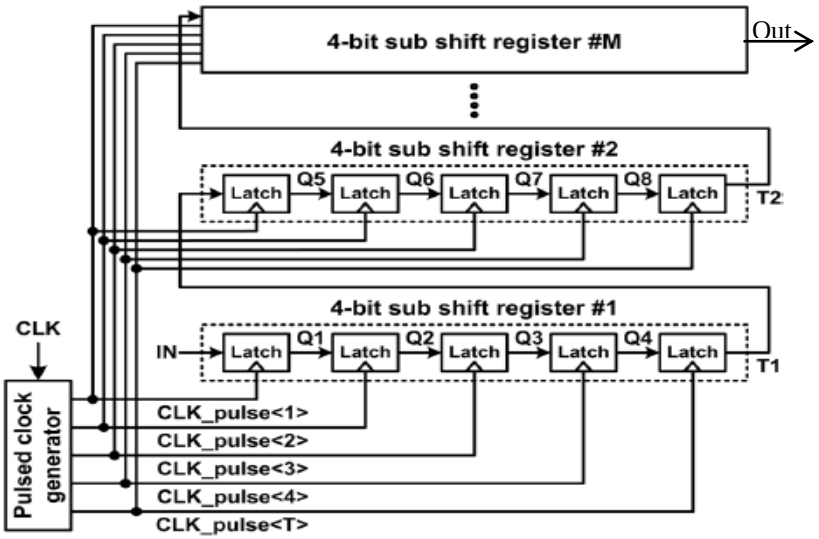

Fig.7: Shift register using pulsed latches

In the above Fig.7it can be observed that the shift register is divided into M-sub shift registers. This is done in order to reduce the number of multiple non-overlap delayed pulsed clock signals generated by the Pulsed clock generator. A 4-bit sub shift register #1 consists of five latches in which the first four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1)which will then be stored in the first latch (Q5) of the 4-bit sub shift register #2. In this shift register shifting is performed with the help of five non-overlap delayed pulsed clock signals (CLK_pulse [1:4]) and CLK_pulse [T] which are generated by the delayed pulsed clock generator. Initially forthe first latch of the sub shift register is provided with an input (IN)and then Q1 of the first latch receives data. Similarly, the latches (Q2-Q4) receive the data from their previous latches (Q1-Q3).Thus, the operations of the other sub shift registers are similar to that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

Even though the timing problem is solved between the latches by using multiple non-overlap delay pulsed clock signal generated by pulsed generator, there is an area and power overhead. This problem occurs due to the presence of delay circuits in the pulsed clock generator. To overcome this drawback an explicit pulse triggered flip flop based on signal feed-through scheme is preferred over pulsed latches.

This paper aims at enhancing the performance of shift register using explicit pulse triggered flip flop based on signal feed-through scheme in order to get better results when compared to shift register using pulsed latches.

Till now the architectural description of shift register using pulsed latches and its disadvantages are discussed. Furthermore, the need for an explicit pulse triggered flip flop in a shift register is also presented. The remaining paper is categorized in the following manner: Section I: described the architecture of the shift register using pulsedlatches;Section II: detailed architecture of Shift register using explicit pulse triggered flip flop based on signal feed-through scheme (P-FF); Section III: provides the details of results and comparisons of shift register using pulsed latches and Shift register using explicit pulse triggered flip flop based on signal feed-through scheme (P-FF) ; Section IV: provides the conclusion of the paper.

In the next section the architecture details of the shift register using explicit pulse triggered flip flop based on signal feed-through scheme (P-FF) is given in detail.

II. Architecture of Shift Register Using Explicit Pulse Triggered Flip Flop

The VLSI architecture which is to be used to build the shift register is Explicit Pulse Triggered Flip Flop based on Signal Feed-through scheme. This pulse triggered flip flop is preferred over the other pulse triggered flip flops such as Static Conditional Discharge Flip Flop (SCDFF) and Modified Hybrid Latch Flip Flop(MHLFF) because in Static Conditional Discharge Flip Flop (SCDFF) the main drawback is it experiences longer data-to-Q (D-to-Q) delay and this worst case delay is caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this draw back a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. Thus,Modified Hybrid Latch Flip Flop(MHLFF) is used .Eventhough the circuitry of Modified Hybrid Latch Flip Flop(MHLFF) is simple but it also experiences two draw backs. They are: node X becomes floating when input Data and output Q both are equal to “1” and it also

encounters a longer Data-to-Q (D-to-Q) delay. So to overcome these drawbacks the explicit Pulse Triggered Flip Flop based on Signal Feed-through scheme is used.

The architecture of Explicit Pulse Triggered Flip Flop based on Signal Feed-through scheme is shown in Fig.8

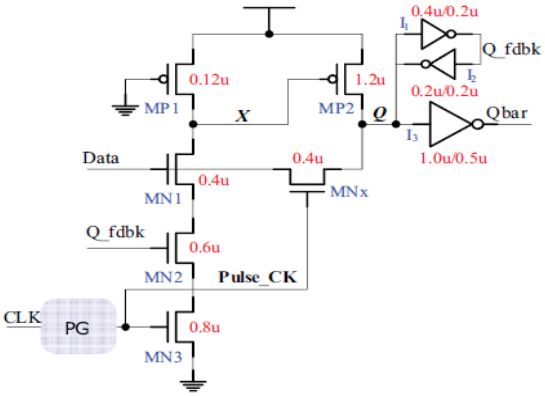

Fig.8: Pulse Triggered Flip Flop Based on Signal Feed-through scheme

The Explicit Pulse Triggered Flip Flop Based on Signal Feed-through scheme adopts a signal feed-through technique to amend the delay. When compared to other pulse triggered flip flops such as Static Conditional Discharge Flip Flop (SCDFF) and Modified Hybrid Latch Flip Flop(MHLFF) there are three major differences. First,A weakpull up pMOStransistor MP1 gate is connected to ground such that it reduces the load capacitances at node X.Second, the pass transistor MNx controlled by the pulsed clock signal is included so that the input data can drive node Q directly. Thepull up transistor MP2 provides extra passage facility for the auxiliary signals to drive from the input source to the output node Q. Third, The pull down network at the second stage of the inverter is removed and is replaced by the pass transistor MNx as it provides a discharging path. The MNx transistor plays dual role , i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions.Thus, it improves the delay and reduces the discrepancies during the rise time and fall time delays.

From the above discussion, shift register using explicit pulse triggered flip flop based on signal feed-through scheme is implemented. The architecture of 4-bit shift register is shown in Fig.9.

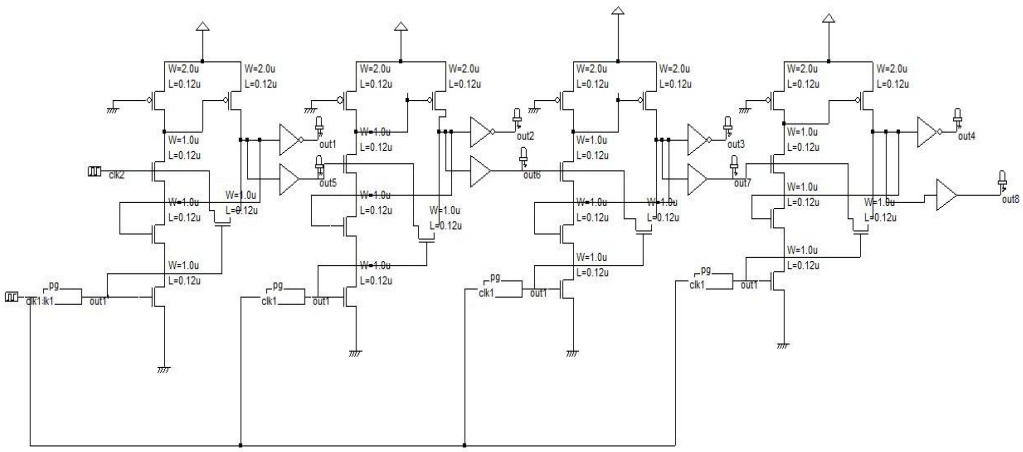

Fig.9:4-Bit Shift Register Using Explicit Pulse Triggered Flip Flop Based On Signal Feed-Through Scheme (P-FF)

The 4-bit shift register shown in Fig.9reduces the average power and area when compared to other flip flop designs. The design of a four bit serial in serial out shift register is shown above. This shift register is implemented using the explicit pulse triggered flip-flop based on signal feed through scheme. For implementing higher order applications it further reduces power and area.

Till now the details of the architecture of shift register using explicit pulse triggered flip flop based on signal feed-through scheme is presented. The next section discusses the results and the comparisons made with shift register using pulsed latches with respect to area and power is presented in detail.

III. Results and Comparisons

Results:

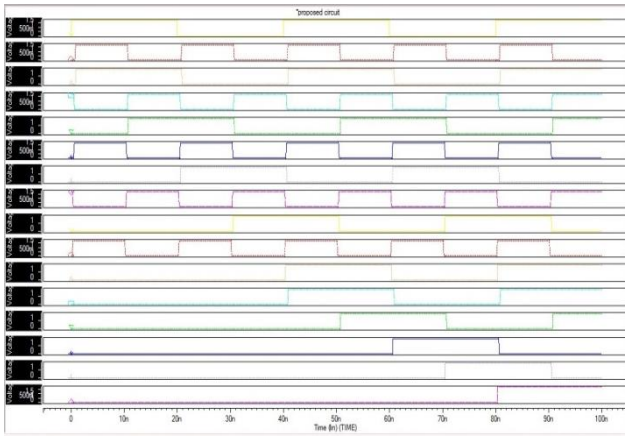

Fig.10: Shift Register using Pulsed latches

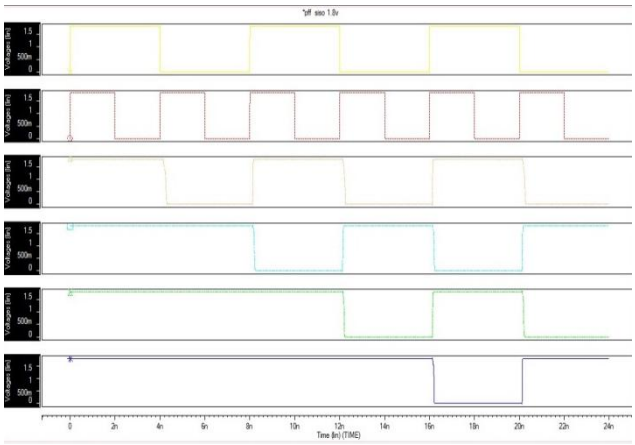

Fig.11: Waveform of 4-bit shift register using based on signal feed-through scheme (P-FF)

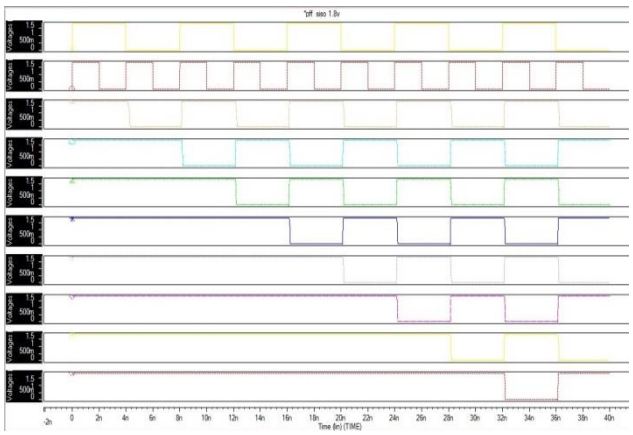

Fig.12: Waveform of 8-bit shift register using based on signal feed-through scheme (P-FF)

The results obtained for Shift register using pulsed latches, 4-bit shift registerusing Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme and 8-bit shift register using Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme are shown in Fig.10, Fig.11, and Fig.12. From the obtained waveforms we observe that the output appears at the rising edge of the clock pulse without any timing delay. The layouts for Shift register using pulsed latches, 4-bit shift register using Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme and 8-bit shift register using Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme are shown in Fig.13, Fig.14, and Fig.15.

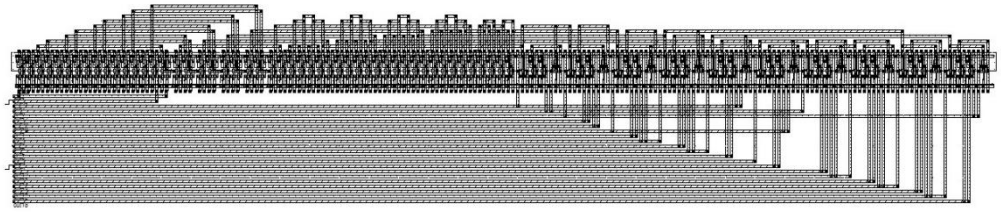

Fig.13: Layout of shift register using pulsed latches

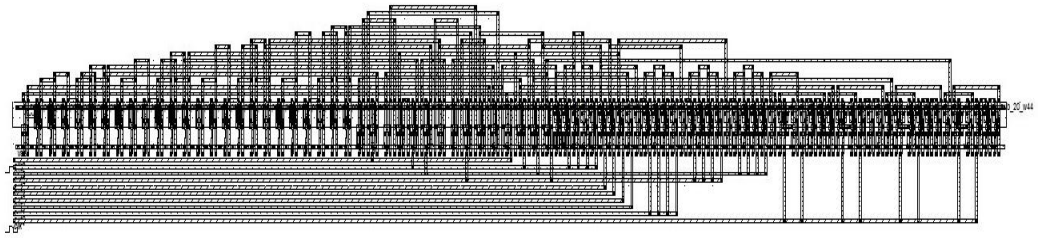

Fig.14: Layout of 4-bit shift register using based on signal feed-through scheme(P-FF)

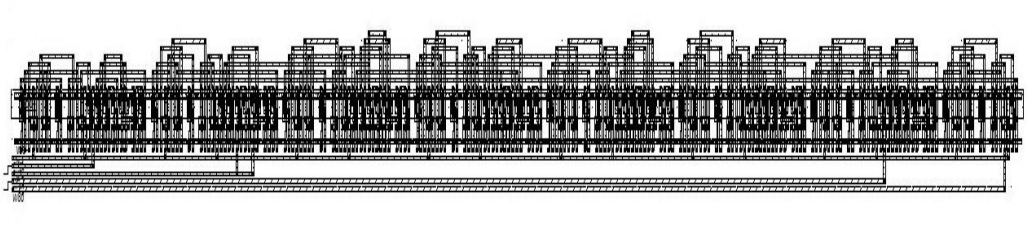

Fig.15: Layout of 8-bit shift register using based on signal feed-through scheme(P-FF)

The area and power consumed byfor Shift register using pulsed latches, 4-bit shift register using Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme and 8-bit shift register using Pulse Triggered Flip Flop Based on Signal Feed-Through Scheme are shown in Fig.16, Fig.17, and Fig.18.

```
******  transient analysis              tnom=  25.000 temp=  25.000
******
 avgval=  6.5724E-06  from=  1.0000E-08     to=  5.5000E-08
 avg_power=  7.6354E-04  from=  0.0000E+00     to=  1.0000E-07
```

Fig.16: Shift register using pulsed latches

```
******  transient analysis              tnom=  25.000 temp=  25.000
******
 avg_power=  2.4629E-05  from=  0.0000E+00     to=  1.0000E-07
 avgval=  1.1685E+00  from=  1.0000E-08     to=  5.5000E-08
```

Fig.17:4-bit shift register usingbased on signal feed-through scheme (P-FF)

```
******  transient analysis              tnom=  25.000 temp=  25.000
******
 avgval=  1.3987E+00  from=  1.0000E-08     to=  5.5000E-08
 avg_power=  5.3110E-05  from=  0.0000E+00     to=  1.0000E-07
```

Fig.18: 8-bit shift register using based on signal feed-through scheme P-FF

As the results obtainedare verified and are found to be satisfactory both with respect to functionality and timing delay, comparisons of Number of bits for both the Shift register using pulsed latches and shift register using Pulse triggered flip flop based on signal feed-through scheme are made with respect to area and power.The details of comparison are shown in Table I:

No. of bits	Shift register withPulsed latches		Shift register withP-FF	
	Area(um^2)	Power(mW)	Area(um^2)	Power(mW)
4	0.000005877	0.48	0.00000011685	0.0024629
8	6.9376	0.71815	1.3987	0.0053110
16	6.5229	0.83405	1.8000	0.10186
32	5.9462	0.87925	1.8000	0.16027
64	5.4493	1.0045	1.8000	0.28824

Table I: Comparison of Shift Register Using Pulsed Latches and Shift Register Using P-FF

Thus,a comparative parametric analysis is obtained for area between Shift register using pulsed latches and shift register using Pulse triggered flip flop based on signal feed-through schemeis shown in Fig.19.

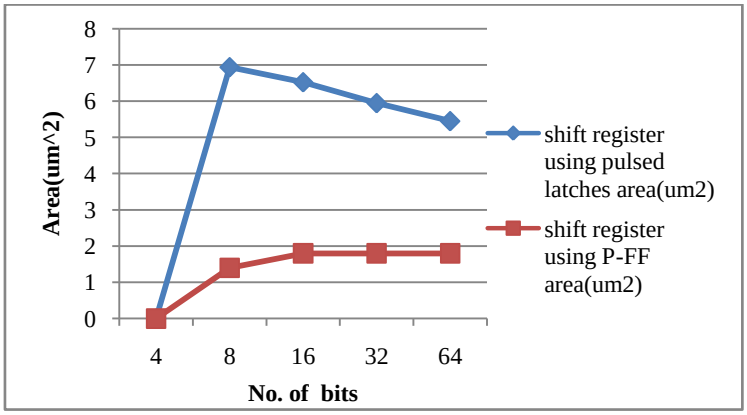

Fig.19: Comparison of Area of Shift Register Using Pulsed Latches and Shift Register Using P-FF

Generally,we know that with the increase in number of bits in shift register the areadecreases. From Fig.19a comparative analysis of area, as the number of bits in the shift registerincreases the area consumed byshift register using pulsed latches decreases but it is more when compared to the area of shift register using Pulse triggered flip flop based on signal feed-through scheme. Thus,the area consumed by shift register using Pulse triggered flip flop based on signal feed-through scheme is very much less when compared to the area consumed by shift register using pulsed latches.Similarly,a comparative parametric analysis is also obtained for power between Shift register using pulsed latches and shift register using Pulse triggered flip flop based on signal feed-through scheme is shown in Fig.20.

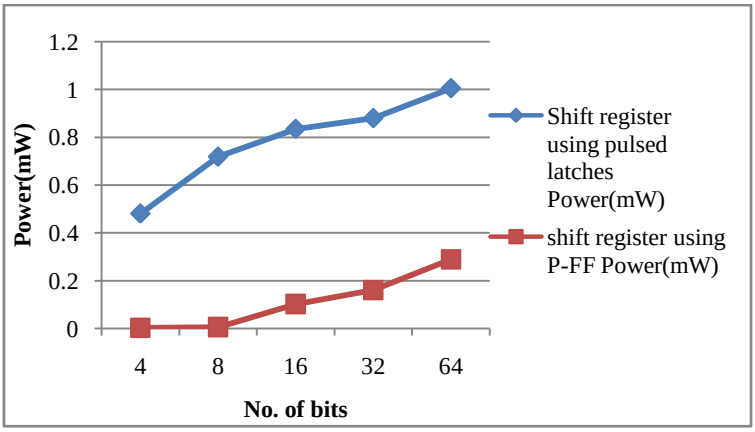

Fig.20: Comparison of Power of shift register using pulsed latches and shift register using P-FF

We know that with the increase in number of bits in shift register the power also increases. From Fig.20 acomparative analysis of power, as the number of bits in the shift register using pulsed latches increases the power consumed by more shift register using pulsed latches also increases when compared to the power of shift register using Pulse triggered flip flop based on signal feed-through scheme. Hence the Power consumed by shift register using Pulse triggered flip flop based on signal feed-through scheme is less when compared to the power consumed by shift register using pulsed latches.

Thus, from the above results and comparisons it is clear that the Shift Register Using Pulse Triggered Flip Flop Based onSignal Feed-Through Scheme (PFF) obtains low power and less area when compared to shift register using pulsed latches.

IV. Conclusion

This paper proposed a low-power area efficient Shift Register using Pulse Triggered Flip Flop based on Signal Feed-Through Scheme (PFF). The shift register reduces area and power consumption by replacing pulsed latches with Pulse Triggered Flip Flop based on Signal Feed-Through Scheme. The results obtained shows that the proposed Shift Register using Pulse Triggered Flip Flop based on Signal Feed-Through Scheme saves 79.83% of area and99.26% of power. Hence the shift register designed with Pulse Triggered Flip Flop based on Signal Feed-Through Schemeis much better when compared to the Shift Register using Pulsed Latches shown in the paper. It is observed that efficiency of the proposed shift register with Pulse Triggered Flip Flop based on Signal Feed-Through Scheme increases with number of bits.

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