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Effect of Dielectric Variations on Performance of Carbon Nanotube Field Effect Transistor Based Basic Logic Gates

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Abstract: *The continuous scaling down of feature size in Silicon technology has resulted in several technological and fundamental hindrances. The researchers started to look for new nanoscale devices those can replace CMOS transistors in digital circuits. The nanowire transistor, FinFET, Carbon Nanotube field effect transistor (CNFET), tunnel field effect transistor (TFET), and single electron transistor (SET) emerged as potential future replacement for CMOS transistors in digital circuits. CNFETs are being considered to be most promising device because of its novel properties like high current carrying capability (~ 10^{10} A/cm^2), excellent carrier mobility, scalability, high reliability for elevated temperature operation, and negligible leakage current. Moreover CNFET has structure and mode of operation similar to CMOS transistor. This paper presents design of virtual source CNFET based basic logic gates. Then, it analyzes the effect of dielectric variations on performance parameters of carbon nanotube field effect transistor based universal gates. The performance parameters computed for designed gates are delay, power consumption, and figure-of-merit power-delay product (PDP). H-SPICE simulator has been used for simulations using Stanford University Virtual-Source CNFET model. Comparison between CMOS and CNFET based logic circuits is carried out for different dielectric material at 16nm technology node.*

Keywords: *CMOS, CNT, CNFET, FinFET, NAND, NOR, SWCNT, MWCNT.*

I. Introduction

According to International Technology Roadmaps for Semiconductors (ITRS) reports shrinking of feature size following Moore's footprints in Silicon technology will reach its limit by 2020 due to device non-idealities and as channel length goes below 10nm. The silicon transistor suffers from more power consumption, low reliability and performance degradation in nanoscaled technologies [1]. The reason behind the rise in power consumption is that the feature size is not scaling at the same pace as the supply voltage and it is hard to improve circuit performance by bringing down its channel length [2]. It is observed that these hindrances can be conquered with the use of novel devices such as single electron tunneling (SET), nanowire FET, carbon nanotube field effect transistor (CNFET) and spin field effect transistor (SPINFET) which are expected to replace conventional CMOS transistors in near future [3]. In order to enhance the performance of electronic circuits such as analog and digital circuits, these new technologies are considered to be the best possible alternative to CMOS technology. CNFET is considered to be the most promising device because its operation is just similar to MOSFET and it will utilize the pre designed structures of silicon devices without any notable alterations [4]. In addition to that CNFETs shows advantages over basic CMOS platform based devices such as low power consumption, high transconductance, high speed operation, excellent current carrying capability and negligible leakage effect. Because of these remarkable advantages offered by CNFETs lot of research has been going on modeling and making its way towards digital devices such as logic gates to compute its performance [5].

Basically digital system design is associated with the binary logic [6], where digital computation is performed on two valued logic ('0' or '1') in Boolean space [7]. Universal gates such as NAND and NOR gate forms the basics of any digital circuitry. Hence the optimum design of universal gates in terms of low power, high speed and good figure of merit is desired for overall performance of digital circuit /system. Nowadays, speed and power are becoming most important issues [8]. CNFET become most promising device to be used for getting low power and low off current properties as compared to CMOS transistors [9].

This paper describes how CNFETs take over MOSFET in terms of performance in digital circuits. Therefore CNFET need to be studied in brief and used as a best alternative to CMOS technology [11]. The DC characteristics of CNFET are similar to CMOS transistors designs. Digital circuits like Inverter, NAND and NOR gates are designed and simulated using H-Spice. Comparative analysis between circuits designed using Virtual-Source CNFET model of Stanford University and Predictive Technology Model for CMOS transistors for low power applications at 16nm technology has been carried out. In order to compute performance variation with device parameters like gate dielectric material is has been analyzed in terms of delay, power dissipated and

power delay product. Comparison in terms of various parameters has also been performed at 32 nm technology node.

This paper is organized as follow: some related publications are presented in section II. CNFET device description with working principle is described in section III. The comparative analysis between CNFETs and CMOS based digital circuits such as inverter, universal gate (NAND, NOR) along with comparative analysis between reference [12] and this paper work has been carried out in section IV. Results and discussions are covered in section V, and Conclusions are drawn in section VI.

II. Related Work

Chi-shuen Lee *et al.* presented the characteristics of CNFET at sub-10 nm regime giving better results than its counterparts due to its high drive current [4]. S. Lin *et al.* designed ternary logic gates using CNFETs by utilizing binary gates which give high performance, consuming less area and power [7]. S. Shreya *et al.* analyzed that CNFET based digital circuits have high speed, low power and energy efficient [11]. P. Yeole *et al.* designed and compared CMOS and CNFET based logic gates concluding that CNFET based designs have better figure of merit as compared to CMOS based designs [12]. R. Sahoo *et al.* designed CNFET with favorable number of CNTs as a channel and concluded that SW-CNT has better performance over MW-CNTs in a CNFET based logic gates [13]. M. H. B. Jamaa *et al.* presented a method to calculate power consumption in ambipolar CNFETs, which gives 57% power saving then conventional CMOS [14]. M. H. B. Jamaa *et al.* proposed ambipolar library of CNFETs and investigated the performance will be improved by seven times as compared to CMOS [15]. G. Firori *et al.* demonstrated that double gate CNFET structure has good transconductance, driving current and very small Short Channel Effects (SCEs) even for thick gate dielectric [16]. S. Prabhu *et al.* analyzed the effect of supply voltage on power delay product of logic gates designed using CNFETs [17]. R. Gupta *et al*. compared digital inverter based on CNFET and CMOS technology and analyzed that short circuit current in CNFET based inverter is present for shorter duration and of very small value as compared to CMOS, thus resulting in PDP improvement of 1500 times better in CNFET based inverter [18]. G. Navin *et al.* analyzed the performance of CNFET in a memory cell; switching speed of device can be improved by reducing the metal contact size, reducing thickness of oxide as compared to channel length and higher dielectric to improve the performance of device [19]. S. G. Shirazi *et al.* presented the variation in performance of device due to temperature effect on different dielectric materials, higher will be the dielectric value more will be leakage but temperature above 450K has least effect on the device performance for various dielectric materials [20]. A. Singh *et al.* analyzed the performance of CNFET for low power applications, high I_{ON}/I_{OFF} ratio, sharp sub-threshold slope, high transconductance in CNFETs show that it is a promising device to be used at nanoscale [21]. S. K. Sinha *et al.* studied the comparison of leakage power in CNFET and MOSFET, it was observed that threshold voltage (V_{TH}) varies sharply in MOSFET at high temperature (t > 150℃) whereas in CNFET temperature has negligible effect on V_{TH} [22].

III. CNFET Device Structure

CNT was discovered in 1991 by Sumio Iijima [17]. Carbon Nanotube (CNT) forms the backbone of CNFETs. It was first testified in 1998, since then there is a continuous development in CNFETs. In last few years, CNTs have emerged as promising material for nanoscaled technologies. The excellent mechanical and electrical properties of CNTs such as high tensile strength, stiffness, high thermal conductivity, good electrical conductivity, light weight and toughness acted as driving force for their applications in chip interconnects and as channel material between source and drain terminal of transistor [23]. The rolled up graphene sheets in the form of hollow cylinders are basically called CNTs. CNT can operate at elevated temperature (~250℃), very high current carrying capability (~ 10^{10} A/cm^2), larger mean free path (up to $100\mu m$) etc. With the use of CNTs in FET high performance, high impedance, faster switching speed can be achieved [11].

The properties of CNT depends upon the way sheet is wrapped to form nanotubes represented as a chiral vector, commonly expressed as (n, m), if n-m$\neq 3i$ (i is integer) then it is semiconductor otherwise metallic [24]. Semiconductor SWCNTs are always preferred over metallic SWCNTs or MWCNTs because it is able to switched off properly in case of low biasing at source/drain. As CNT works on the principle of ballistic transport [25], metallic CNTs has ability to carry huge amount of current, whereas semiconducting CNTs are used in switching circuits. Switching rate of device can be improved by minimizing its dimensions.

There are different types of CNFETs like Schottky Barrier (SB-CNFET) [26], Tunnel (T-CNFET) [26] and MOSFET like CNFET [27]. In Stanford University Virtual source model for CNFETs (VS-CNFET model), MOSFET like CNFETs are considered with cylindrical gate-all-around structure at room temperature (25℃) for heavily doped source/drain regions [4]. Figure 1.1 represents CNFET device structure.

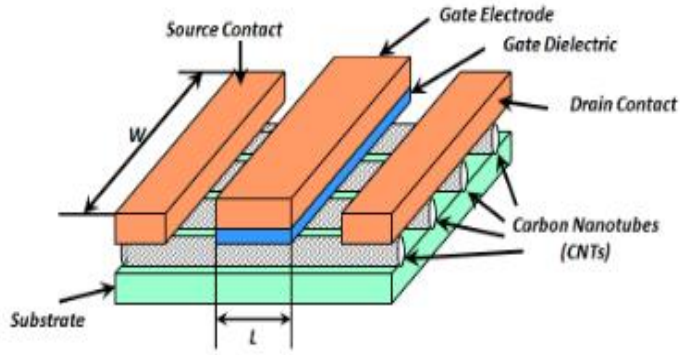

Figure 1 CNFET Device Structure [32]

Figure 1 shows that channel is composed of CNTs with metal contact all around and situated on a gate dielectric. For MOSFET like structure of CNFET both P-type FET and N-type FET shows similar results irrespective of SB-CNFETs which shows ambipolar phenomenon [15]. CNTs have large mean free path; so at nanoscale, there is no scattering of charge carriers even at channel length of 100 nm. The diameter (d) of a tube and the chiral angle (θ) are measured from its chiral vector coordinates as described by equation (1) and (2) respectively as follows:

$$d = \frac{\sqrt{3}a}{\Pi}\sqrt{(n^2 + nm + m^2)} \quad (1)$$

$$\text{Cos}\theta = \frac{(n+m)/2}{\sqrt{nm + m^2 + n^2}} \quad (2)$$

Where, 'a' is carbon-carbon bond distance and is 0.246 nm [28]. Current in CNFETs can be easily changed either by varying the diameter of tube or by making use of more than one tube as a channel. If n=m then carbon nanotubes is metallic, when n-m=3*i* with small gap is semi-metallic, where *i* is an integer, and when n-m≠3*i*, it is semiconductor. Equation (3) states that energy Gap (E_g) of a tube changes with change in its chirality and diameter [29] is given as:

$$E_g = \gamma\left(\frac{2a}{d}\right) \quad (3)$$

Where, γ is hopping matrix element. The threshold voltage depends upon the diameter of CNT which is a function of chiral vector (n, m). Threshold voltage (V_{TH}) of a CNFET is minimum voltage to be maintained at gate to make transistor ON, and is given in equation (4) as:

$$V_{TH} = \frac{b\,(V_\pi)}{\sqrt{3}\,q\,d} \quad (4)$$

Where, q = 1.6×10^{-19} coulombs, b = 2.49Å, a lattice constant and $V_{\prod}$ = 3.033eV is carbon π-to-π bond energy [28]. CNFET uses either a single walled carbon nanotube (SWCNT) or an array of carbon nanotubes called multi walled CNT (MWCNT) as a channel material. In general single walled CNTs are more preferred over multi-walled CNTs. Nano tubes are separated from gate contact by a gate insulator. In silicon technology silicon dioxide can be used as an insulator but in CNFET high-k gate dielectric materials are preferred because with scaling in technology down to nanometers, there is a direct tunneling of electrons from insulator to substrate which may cause increase in power dissipation. Thickness of gate insulator below 1.5nm in MOSFET causes direct tunneling of current through gate. So high-k dielectrics such as aluminium oxide (k=9), hafnium oxide (k=15.6), and zirconium oxide (k=19) are used [22] with oxide thickness below 1.5nm for better performance.

IV. Simulations and Results

Simulations are performed using H-SPICE and results obtained are listed in table 2, 3, 4, 5, 6 and 7. Virtual Source CNFET model from Stanford University has been used for all simulations and PTM models have been used for CMOS transistors. Table 1 lists user defined input parameters for virtual- source CNFET. To compute the performance of the conventional CMOS and virtual-source CNFET, the simulation of basic logic gates like inverter and NAND/NOR has been carried out at 16 nm technology node.

Table 1 Virtual Source CNFET Input Parameters [27]

Parameter	Value	Description
type	-1 or 1	Type of transistor -1: nfet, 1: pfet
Lg	16 nm	Physical gate length

Lc	12.9 nm	Contact length
Lext	3.2 nm	Source/drain extension length
s	10 nm	Spacing between CNTs
Hg	20 nm	Gate height
Geomod	1	Cylindrical gate all around device geometry
SDTmod	1	Source/drain tunneling with inter-band tunneling
BTBTmod	1	Band to band tunneling bond on
Rcmod	1	Diameter-dependent transmission line model
Rs0	0	Series resistance
Vfbn	0.015	Flat band voltage for nfet
Vfbp	-0.015	Flat band voltage for pfet
Dia	1.2 nm	Diameter of CNT
Kox	4-25	Gate oxide dielectric constant
tox	1.2 nm	Thickness of oxide
supply	0.71 v	Gate supply voltage
TEMP	25	temperature

The performance of CMOS and CNFET based inverter and NAND/NOR logic circuits have been analyzed for different gate dielectric materials. Various dielectric materials considered are silicon nitride (Si_3N_4), Aluminum oxide (Al_2O_3), Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) having dielectric constant 7.5, 9, 15.6 and 19 respectively [22]. Table 2 lists the delay, power dissipation and power-delay product for CMOS and CNFET based inverter circuit. It is observed that CNFET based inverter offers PDP improvement of 96.92, 97.20, 111.12 and 123.27 % for Si_3N_4, Al_2O_3, HfO_2, and ZrO_2 dielectric materials respectively. Similarly, delay, power dissipation and power-delay product for CMOS and CNFET based NAND and NOR gates have been computed for different dielectric materials and listed in Table 3 and Table 4 respectively.

Table 2 PDP Calculations for CNFET and CMOS Based Inverter at 16 Nm Technology

Dielectric Material	CMOS			CNFET			PDP Improvement for CNFET Inverter (%)
	Delay (ps)	Power Dissipation (nW)	Power Delay Product (zJ)	Delay (ps)	Power Dissipation (nW)	Power Delay Product (zJ)	
Si_3N_4	4.0878	2.9972	12.251	1.0723	0.1167	0.1251	96.92
Al_2O_3	4.2021	3.2228	13.542	1.0626	0.1297	0.1379	97.20
HfO_2	4.7677	4.2357	20.194	1.0555	0.1707	0.1801	111.12
ZrO_2	5.1496	4.7254	24.333	1.0582	0.1851	0.1958	123.27

Table 3 PDP calculations for CNFET and CMOS based NAND gate at 16 nm technology

Dielectric Material	CMOS			CNFET			PDP Improvement for CNFET NAND gate (%)
	Delay (ps)	Power Dissipation (nW)	Power Delay Product (zJ)	Delay (ps)	Power Dissipation (nW)	Power Delay Product (zJ)	
Si_3N_4	7.5863	3.7311	28.305	1.2741	0.1167	0.1487	189.34
Al_2O_3	8.0148	4.0289	32.290	1.2587	0.1297	0.1633	196.73
HfO_2	9.8739	5.1156	50.510	1.2396	0.1707	0.2116	237.70
ZrO_2	10.7275	5.6389	60.491	1.2362	0.1851	0.2288	263.38

Table 4 PDP Calculations for CNFET and CMOS based NOR gate at 16 nm Technology

Dielectric Material	CMOS			CNFET			PDP Improvement for CNFET NOR gate (%)
	Delay (ps)	Power Dissipation (nW)	Power Delay Product (aJ)	Delay (ps)	Power Dissipation (nW)	Power Delay Product (aJ)	
Si_3N_4	4.3972	11.5593	0.05082	1.4220	0.2335	0.00033	153
Al_2O_3	4.5354	12.3230	0.05588	1.4087	0.2595	0.00036	154.2
HfO_2	5.2328	16.0874	0.08418	1.3946	0.3414	0.00047	178.10
ZrO_2	5.5865	18.0136	0.10063	1.3951	0.3702	0.00051	196.31

In nanoscaled technologies, the thickness of oxide play crucial role in deciding gate leakage currents. Conventional CMOS technology shows significant non-ideal effects as thickness of oxide goes below 1.5 nm. Table 5, 6 and 7 illustrate PDP results of CNFET based inverter, NAND and NOR gates for various dielectric materials as oxide thickness is varied from 1 nm to 4 nm. It is observed that as the dielectric constant increases, PDP at a fixed gate oxide thickness increases. It is also observed that as gate oxide thickness increases from 3 nm, PDP starts increasing and as oxide thickness goes below 2 nm, PDP starts increasing. The optimum results for PDP are obtained at gate oxide thickness of 2nm.

Table 5 PDP results for CNFET Inverter for Oxide Thickness Variations

Power Delay Product (zJ)				
Thickness of Oxide (T_{OX})	**Dielectric Material**			
	Si_3N_4	**Al_2O_3**	**HfO_2**	**ZrO_2**
1 nm	0.1345	0.1478	0.1909	0.2065
2 nm	**0.1063**	**0.1175**	**0.1570**	**0.1725**
3 nm	0.1112	0.1227	0.1652	0.1826
4 nm	0.1603	0.1770	0.2397	0.2660

Table 6 PDP results for CNFET based NAND Gate for Oxide Thickness Variations

Power Delay Product (zJ)				
Thickness of Oxide (T_{OX})	**Dielectric Material**			
	Si_3N_4	**Al_2O_3**	**HfO_2**	**ZrO_2**
1 nm	0.1594	0.1747	0.2233	0.2404
2 nm	**0.1267**	**0.1399**	**0.1853**	**0.2035**
3 nm	0.1322	0.1461	0.1955	0.2153
4 nm	0.1896	0.2096	0.2823	0.3125

Table 7 PDP results for CNFET Based NOR Gate for Oxide Thickness Variations

Power Delay Product (zJ)				
Thickness of Oxide (T_{OX})	**Dielectric Material**			
	Si_3N_4	Al_2O_3	HfO_2	ZrO_2
1 nm	0.3565	0.3914	0.5035	0.5435
2 nm	**0.2825**	**0.3124**	**0.4168**	**0.4573**
3 nm	0.2952	0.3265	0.4396	0.4854
4 nm	0.4253	0.4705	0.6378	0.7074

Table 8 lists device parameters of CNFET which are used for simulation of circuits like inverter and NAND/NOR logic gates.

Table 8 Device parameters of CNFET

Device Parameter	**Value**
Diameter of CNT (nm)	1.018
Power supply (V)	0.71
Gate dielectric Materials	Si_3N_4, Al_2O_3, HfO_2, and ZrO_2
Chirality of tube	(13,0)
T_{ox} (nm)	4
Pitch (nm)	4
The width of metal gate (nm)	6.4

Table 9 compares delay, power dissipation and PDP of virtual-source CNFET based inverter, NAND gate and NOR gate with reference [12]. It is found that virtual source based CNFET model offers better results in terms of delay, power dissipation and PDP for digital circuits.

Table 9: Comparison of PDP Results

Parameters	**INVERETR**		**NAND GATE**		**NOR GATE**	
	Reference [12]	This paper	Reference [12]	This paper	Reference [12]	This paper
Delay (ps)	11.6	**1.40**	28.4	**1.50**	20.9	**2.01**
Power dissipation (pW)	209	**461.50**	586.1	**461.50**	3.38.0	**923.01**
Power Delay Product (zJ)	2.424	**0.646**	16.645	**0.692**	7.064	**1.855**

V. Conclusion

This paper presents effect of dielectric variations on performance of Stanford University virtual-source CNFET model based basic logic gates. Extensive HSPICE simulations have been performed to compute the performance parameters. Virtual Source CNFET model from Stanford University has been used for all simulations and PTM models have been used for CMOS transistors at 16 nm technology node. The performance of CMOS and CNFET based inverter and NAND/NOR logic circuits have been analyzed for different gate dielectric materials. Various dielectric materials considered are silicon nitride (Si_3N_4), Aluminum oxide (Al_2O_3), Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) having dielectric constant 7.5, 9, 15.6 and 19 respectively. It is observed that CNFET based inverter offers PDP improvement of 96.92, 97.20, 111.12 and 123.27 % for Si_3N_4, Al_2O_3, HfO_2, and ZrO_2 dielectric materials respectively. Also the effect of gate oxide thickness has been analyzed on the performance of basic circuits as thickness is varied from 1 to 4nm. It is observed that as the dielectric constant increases, PDP at a fixed gate oxide thickness increases. It is also observed that as gate oxide

thickness increases from 3nm, PDP starts increasing and as oxide thickness goes below 2nm, then also PDP starts increasing. The optimum results for PDP are obtained at gate oxide thickness of 2nm. From results, we conclude that virtual source CNFET based circuits are better alternative than CMOS to meet the low PDP requirements.

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