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Design and Power Optimization of Schmitt triggers using Finfet Technology

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Abstract: *The term very large scale integration reflects the capabilities of the semiconductor industry to fabricate a complex electronic circuit consisting of thousands of components on a single chip. Over the last two decades, low-power design has become a concern in digital VLSI design, especially for portable and high performance systems. A single silicon LSI chip may contain tens of thousands of transistors. Scaling of technology node increases power-density more than expected. CMOS technology beyond 50nm node represents a real challenge. Low cost always continues to drive higher levels of integration, whereas low cost technological breakthroughs to keep power under control are getting very scarce. Innovative device architectures will be necessary to continue the benefits that previously acquired. FINFET technology has been born as a result of increase in the levels of integration. Fabrication in FinFET-DGCMOS is very close to that of conventional CMOS process. Double-gate CMOS (DGCMOS) offers distinct advantages . Basic design of Schmitt trigger is shown. Simulation is done in tanner tool in 45nm technology.*

Keywords: *CMOS, DGMOSFET, FINFET, Ion/Ioff, low power, power dissipation, leakage current, Schmitt trigger*

I. Introduction

Gone are the days when huge computers made of vacuum tubes sat humming in entire dedicated rooms and could do about 360 multiplications of 10 digit numbers in a second[2]. Though they were the fastest computing machines of that time, they surely don't stand a chance when compared to the modern day machines. Modern day computers are getting smaller, faster, and cheaper and more power efficient every progressing second. Since the invention of the first IC (Integrated Circuit)[3] in the form of a Flip Flop by Jack Kilby in 1958, our ability to pack more and more transistors onto a single chip has doubled roughly every 18 months, in accordance with the Moore's Law. Such exponential development had never been seen in any other field and it still continues to be a major area of research work. Very-large-scale integration (VLSI)[8] is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip[2]. During the desktop PC design era VLSI design efforts have focused primarily on optimizing speed to realize computation intensive real-time functions such as video compression, gaming, graphics etc[9]. As a result, we have semiconductor ICs that successfully integrated various complex signal processing modules and graphical processing units to meet our computation and entertainment demands. The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements.

While wireless devices are rapidly making their way to the consumer electronics market, a key design constrain for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries[2][5]. So the most important factor to consider while designing SoC for portable devices is 'low power design[1][7]. Static power and Dynamic power dissipation grows rapidly. Overall power is dramatically increasing. If the semiconductor integration continues to follow Moore's Law, the power density inside the chips will reach far higher than the rocket nozzle[7]. Power dissipation is the main constrain when it comes to Portability.

II. Finfets

A. FinFet Background

Cmos technology has a number of short channel effects, such as the threshold voltage roll-off, the drain induced barrier lowering (DIBL) and the subthreshold swing all of which degrade the MOSFET performance. A number of solutions have been proposed to overcome these problems [1][4]. Employing a double gate field effect transistor (DG MOSFET) structure instead of using bulk-Si transistors is one of these solutions. In

addition to the inherent suppression of SCEs, DG MOSFETs offer high drive current and transconductance [3]. More importantly, the electrical coupling between the two gates results in high Ion/Ioff ratios when the threshold voltage is properly controlled[6].

1) FinFet technology has been born as a result of relentless increase in the levels of integration.
2) To achieve the large levels of integration many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area[5].
3) However other figures such as power dissipation and line voltage have reduced along with increased frequency performance.
4) There are limits to the scalability of individual devices and as process technologies shrink towards 50nm,it became impossible to achieve proper scaling of various device parameters[2].
5) It is therefore necessary to look at other more revolutionary options like change in transistor structure from the traditional planar transistors[1].

These effects make it harder for the voltage on a gate electrode to deplete the channel underneath and stop the flow of carriers through the channel – in other words, to turn the transistor Off.

Comparision:

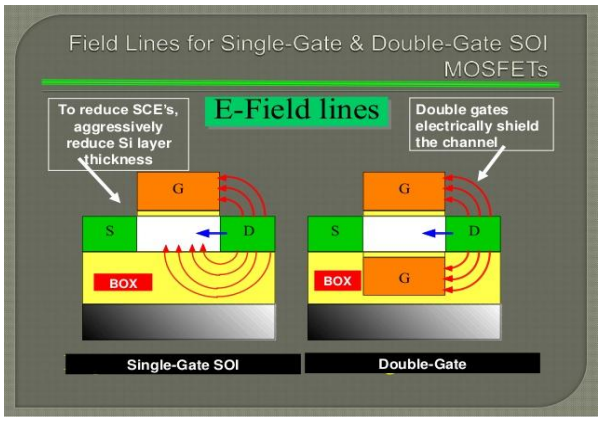

Fig 1 CMOS and DG MOSFET

B. ***Advantages of FinFET technology.***

Power: Much lower power consumption allows high integrational levels. Early adopters reported 150% improvements[6].

Operating voltage: FinFets operate at a lower voltage as a result of their Threshold voltage.

Feature Size: Possible to pass through the 20nm barrier previously thought as an end point[5].

Static leakagecurrent:Typically reduced by upto 85% [6]

Operating speed: Often in excess of 30%faster than the non-FinFet versions

III. Schmitt Trigger

The Schmitt trigger was invented by the American scientist Otto H. Schmitt in 1934 while he was still a graduate student later described in his doctoral as a "thermionic trigger".

It is a comparator circuit with hysteresis implemented by applying positive feedback to the non inverting input of a comparator or differential amplifier[1]. It is an active circuit which converts an analog input signal to a digital output signal. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. In the non-inverting configuration, when the input is higher than a chosen threshold, the output is high[8]. When the input is below a different (lower) chosen threshold the output is low, and when the input is between the two levels the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory. The true Schmitt trigger input has the switching threshold adjusted where the part will switch at a higher point (Vt+) on the rising edge and at a lower point (Vt–) on the falling edge. The difference in these switching points is called Hysteresis (^Vt).

IV. Simulation Results

A. ***Inverter Cmos***

Inverter circuit is designed in tanner tool at 45nm technology.

L=0.045µm W=0.045µm

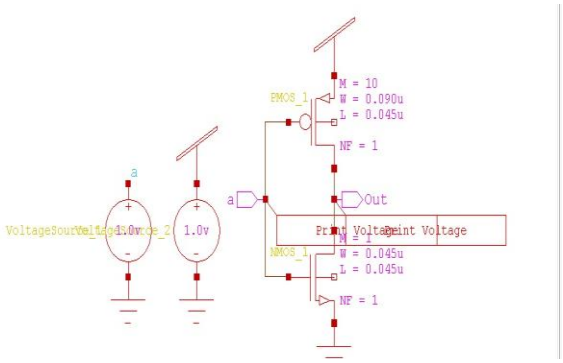

Fig 2 Circuit Inverter CMOS

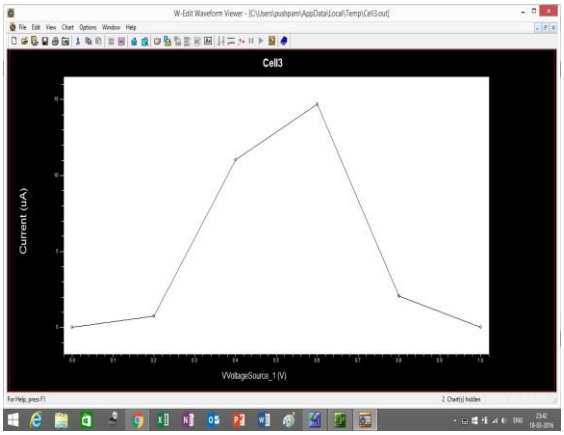

Fig 3 IV Characteristics of CMOS Inverter

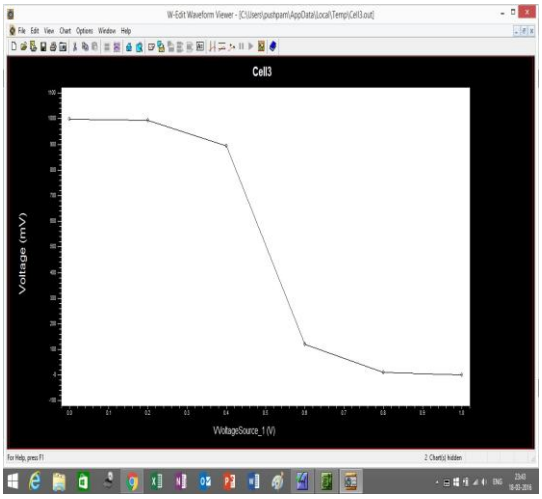

Fig 4 DC Characteristics of CMOS Inverter

Table 1 Vin vs Vout is observed

Vin(volts)	Vout(inv)milli volts
0	999.80
0.1	999
0.2	990.
0.3	960.
0.4	900.
0.5	499.8
0.6	120.
0.7	80
0.8	10
0.9	5
1	0.01

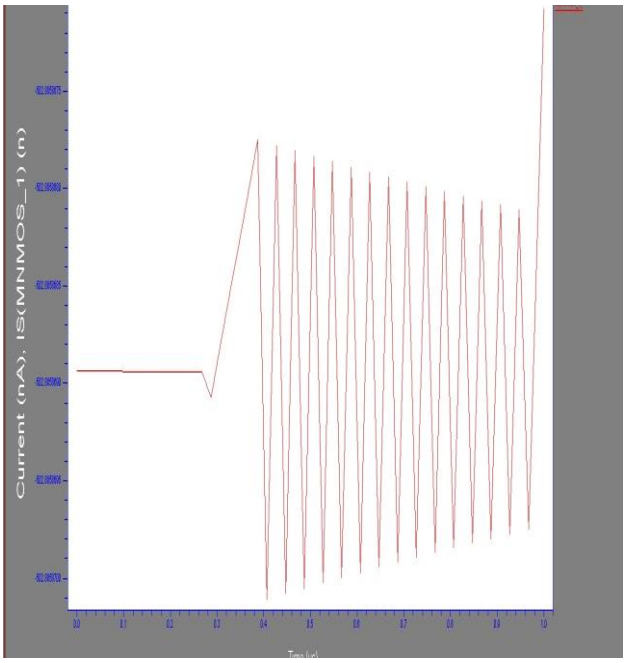

Fig 5 Leakage current waveform CMOS inverter

Table 2 Leakage current wrt time is observed

Time (µ sec)	Leakage current(nano amps)
0	502.88587
0.1	502.88586
0.2	502.88585
0.3	502.88587
0.4	502.88587
0.5	502.88587
0.6	502.88586
0.7	502.88585
0.8	502.88585
0.9	502.88586
1	502.88587

Average leakage current =502.88nano amps.

B. ***Finfet Inverter***

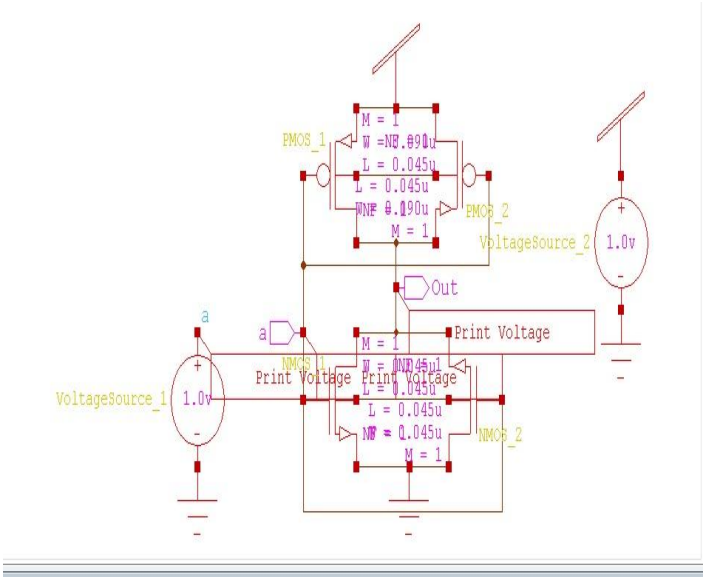

Fig 6 Circuit diagram of FinFet Inverter

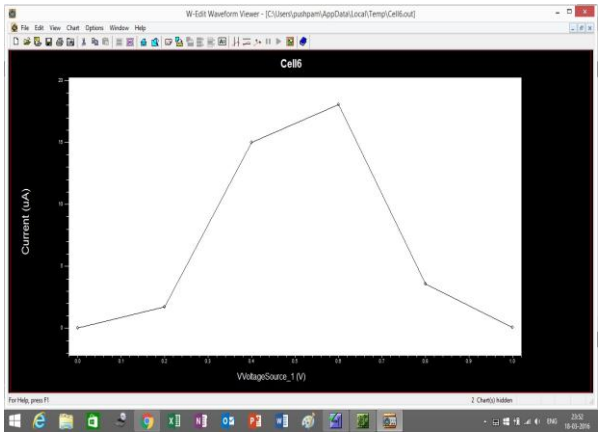

Fig 7 IV characteristics of FinFet Inverter

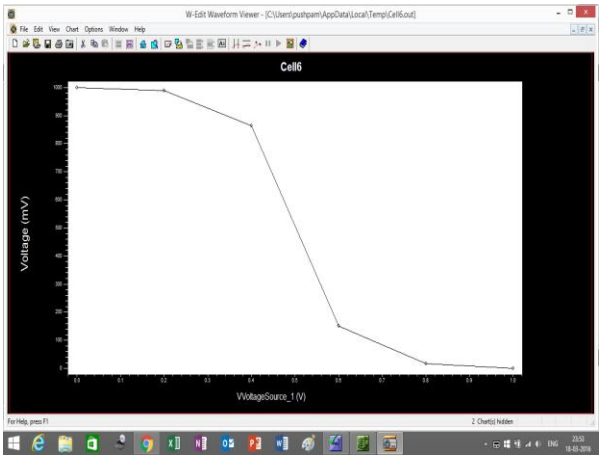

Fig 8 DC Characteristic of Finfet inverter

Table 3 Vin vs Vout is observed

Vin(volts)	Vout(finfet inv)milli volts
0	1000
0.1	990
0.2	980
0.3	940
0.4	860
0.5	500
0.6	150
0.7	90
0.8	20
0.9	10
1	0

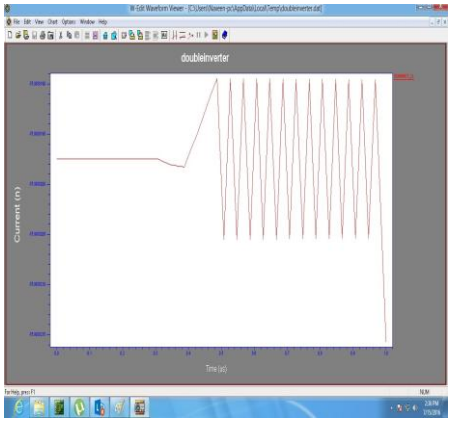

Fig 9 Leakage current waveform FinFet inverter

Table 4 Leakage current wrt time is observed

Time (μ sec)	Leakage current(nano amps)
0	75.9838
0.1	75.9836
0.2	75.9838
0.3	75.9837
0.4	75.9836
0.5	75.9837
0.6	75.9838
0.7	75.9837
0.8	75.9836
0.9	75.9837
1	75.9836

Average leakage current =75.98 nano amps.

C. ***Single Gate Schmitt Trigger***

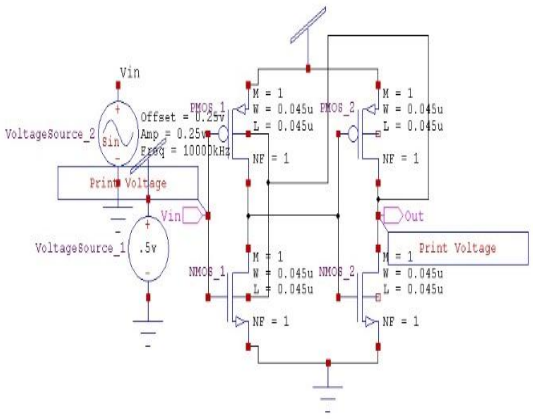

Fig 10 Circuit diagram of single gate Schmitt trigger

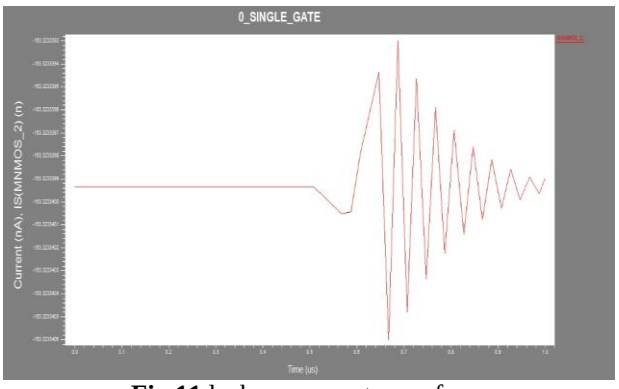

Fig 11 leakage current waveform

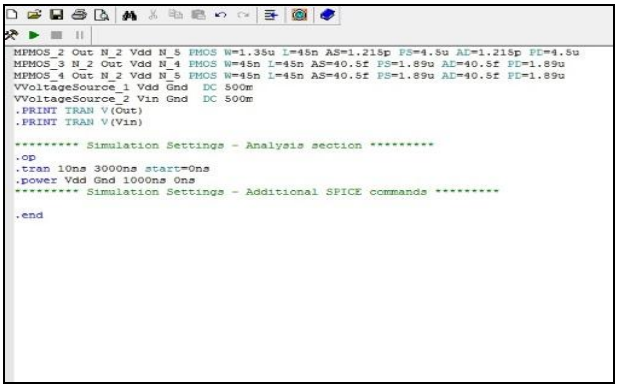

Fig 12 Power command

Table 5 Leakage current wrt time is observed

Time (micro seconds)	Leakage (nano amps)
0	163.3233399
0.1	163.3233399
0.2	163.3233399
0.3	163.3233399
0.4	163.3233399
0.5	163.3233399
0.6	163.3233399
0.7	163.3233340
0.8	163.3233392
0.9	163.3233399
1	163.3233399

Average leakage current =163.323 nano amps.

D. ***Double Gate Schmitt Trigger***

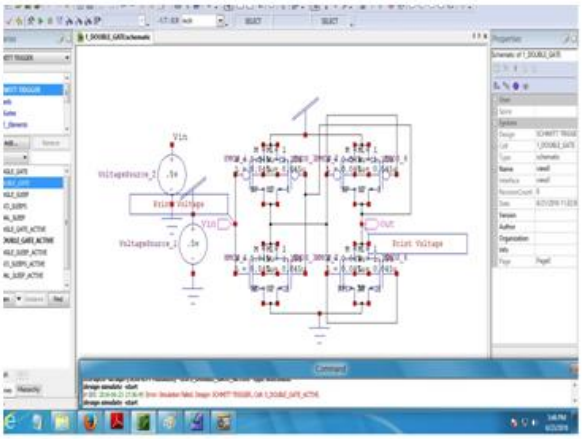

Fig 13 Circuit diagram of Double gate Schmitt trigger

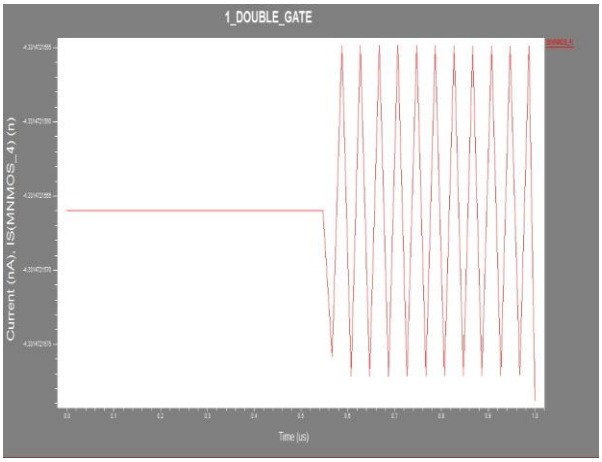

Fig 14 leakage current waveform

Table 6 Leakage current wrt time is observed

Time (micro seconds)	Leakage current(nano amps)
0	4.3314721565
0.1	4.3314721566
0.2	4.3314721565
0.3	4.3314721565
0.4	4.3314721565
0.5	4.3314721566
0.6	4.3314721570
0.7	4.3314721565
0.8	4.3314721570
0.9	4.3314721565
1	4.3314721575

Average leakage current = 4.3314 nano amps.

Table 7 Comparision of Single gate and double gate Schmitt trigger

	Single gate Schmitt trigger	Double gate Schmitt trigger
Average Power (micro watts)	2.390	0.245
Leakage current (nano amps)	163.32334	4.3314722
Rise time delay (nano seconds)	0.779	0.484
Fall time delay (nano seconds)	0.5504	0.266
Upper Threshold voltage(milli volts)	0.25	0.26
Lower threshold voltage(milli volts)	0.235	0.240

Power Consumption:
P=V*I
From the above simulation we observe that the current
is reduced in Finfet compared to MOSFETs. As I is reduced Power is also reduced. Power consumption of FinFet is reduced.
Power consumption of inverter:0.0334µ watts
Power consumption of FinFet inverter:0.01160197µ watts
Power consumption of Single gate based Schmitt trigger: 2.390µwatts
Power consumption of Double gate based Schmitt trigger:0.245µ watts

V. Conclusion

Hence we can say from the above analysis FINFET is better than CMOS technology in terms of power consumption, DC characteristics and leakage currents. Average leakage current in CMOS inverter is 502.8n amps while in FINFET inverter is 75.98 n amps.

Approximately 85% improvement in leakage current is observed between CMOS inverter and FINFET inverter. Single gate based Schmitt trigger circuit and double gate based Schmitt trigger circuit are designed. Double gate is better than Single gate in terms of Average power, leakage current, delay. Percentage improvement in leakage current of double gate compared to single gate Schmitt trigger is 97.34%.

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