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Design, Simulation and FFT for Sense Amplifiers in DRAM using C5 process

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***Abstract**: This paper presents design and detailed FFT analysis for CMOS sense amplifiers for dynamic and static memories. Sense amplifiers in association with semiconductor memories are the key elements in defining the overall performance of CMOS memories. The presented design is implemented using C5 process technology using BSIM-4 Spice models for both open book and closed book architectures. The design includes circuit and operation descriptions, transient signal analysis, FFT analysis, also evaluation of magnitude, phase, and group delay is done at range frequency range from 100 MHz to few GHz. The paper also presents a physical design and interfacing logic for interfacing DRAM Memory arrays to Sense amplifiers and operating point analysis for the same.*

***Keywords**: Sense Amplifiers, DRAM, FFT, CMOS Memories, Sense amplifier interfacing*

I. Introduction

Sensing means the detection and determination of data content of selected memory cell [2]. Sensing shall be non-destructive or destructive and is widely dependent on open or close book architecture in which the CMOS memory is being laid out. The data content of the selected memory cell may be altered or unchanged.SRAMs, ROMs, PROMs etc uses non-destructive sensing and Dynamic RAMs uses destructive sensing.

Sensing circuits generally comprises of sense amplifiers, precharge, reference and load circuits, bitlinedecoupler, an accessed memory cell and other necessary memory control circuits.The control circuits and parasitic elements coupled to horizontal and vertical bit lines generate combined impedance which significantly effects the operation of random access memories. These signals associated with memory control circuits have long propagation and related transients and in turn generate insufficient amplitudes to drive the logic circuits of the memory.

Sense amplifiers are generally applied to improve

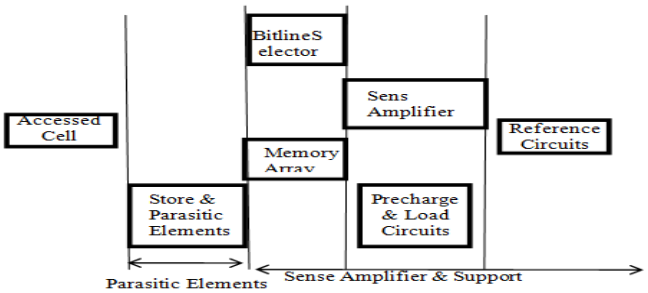

Fig.1 Sense Circuit Topology 1

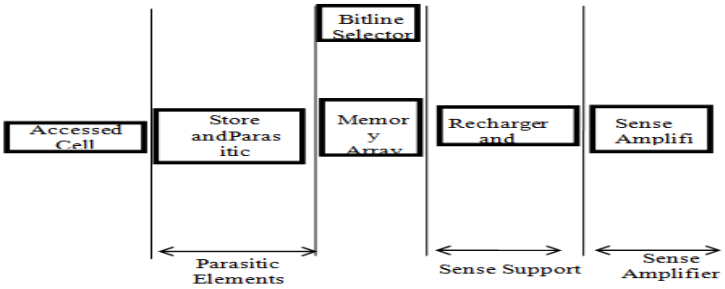

Fig.2 Sense Circuit Topology 2

and provide signals which confirm the requirements of driving peripheral memory circuitry. The presented design for sense amplifier will compare two values and forwarding a greater value and sensing is done by clocking the sense amplifier. [2, 6]

II. Sense Amplifier Design

The summing of the essential conclusions defining the internal operation margins of the sense circuit should be based on worst- case parameters are those which terminate in a maximum degradation in the "0" or "1" operation margin of a sense circuit. For the pronouncement of the worst- case operation margins, the principal voltage terms may be obtained as follows:

A. *Supply Voltage:* In the judgement of operation margins, the initial voltage level V_1 is the minimum supply voltage $V_1 = V_{DD\,(min)} = V_{DD}$. V_1 can be brought out from the supply voltage, eg. $V_{DD} \pm 10\%$, $V_{DD} \pm 5\%$, that is scheduled for the memory.

B. *Threshold Voltage Drop:* The maximum threshold voltage drop V_{TA} through the access transistor of a selected memory cell scales down either the "0" or the "1" operation margin in the sense circuit. On the bitline, the "1" margin lessens when the access transistor is an n-channel device, and the "0" margin fades when transistor is a p-channel device, if a positive supply voltage V_{DD} and a positive logic convention is counterfeited. By the application of a p-channel device as access transistor the minimum achievable bitline voltage V_B rises from $V_B = V_{SS}$ to $V_B = V_O + |V_{TA}|$. Here, V_O is the maximum log.0 output level permeable in the circuit, and operation in the saturation region is presumed for the access transistor.

C. *Leakage Currents:* Leakage currents $I_{L\text{-}S}$ reduce both "0" and "1" operation margins, since they decrease the signal amplitudes on the bitline by $V_{BL} \sim I_L R_B$, and diminish the grade of data stored in memory cells by $V_{CL} \sim I_L R_D$. Here, I_L is the maximum leakage current, R_B consists the maximum resistances of the access transistor and the bitline, R_D is the maximum resistance between the data-storage node and the supply or ground node in the memory cell, and V_{BL} and V_{CL} are the maximum I_L- induced voltages which degenerate the operation margins on the bitline and in the cell, respectively.

D. *Charge Couplings:* Charge couplings $v_c(t)$-s occur mainly through the gate-source or gate-drain and gate-channel capacitances C_{GS}, C_{GD} and C_{GC} of the memory cells access devices and, ultimately, of the bitline decoupling devices, and amend impermanently the signal levels in the memory cells as well as on the bitline and sense-amplifier inputs. The paramount load of charge coupling V_{CC} causes voltage variation in both log.0 and log.1 levels, and modifies both "0" and "1" operation margins unidirectionally.

E. *Imbalances:* Imbalances caused operation margin degradations $V_{IB\text{-}S}$ are particular to those sense circuits which use differential sense amplifiers, and the imbalances reduce both "0" and "1" margins. The phrase imbalance demonstrates the non uniform topological distribution of parameters in the transistor-devices and in the interconnections which comprise of a differential sense circuit.

F. *Precharge Level Variations:*Precharge level variations $\Delta V_{PR\text{-}S}$ due to the effects of semiconductor processing and circumstantial abnormalities may reduce both or either one of the "0" and "1" operation margins. Both margins are ebbed when "midlevel" precharge, and either the "0" or "1" margin may be debased when "low" or "high" level precharge is applied.

III. Design Considerations and Methodology Used

Systematic design methodologies are necessary for implementing various topologies related to sensing circuits. The design of sense amplifiers usually differs by the number of transistors used and sensing circuits implemented with PMOS or NMOS sensing circuits, cell capacitance and memory bit capacitance and corresponding wordline and bitline interfaces. Following block diagram represents the methodology followed for the designing of sensing circuits.

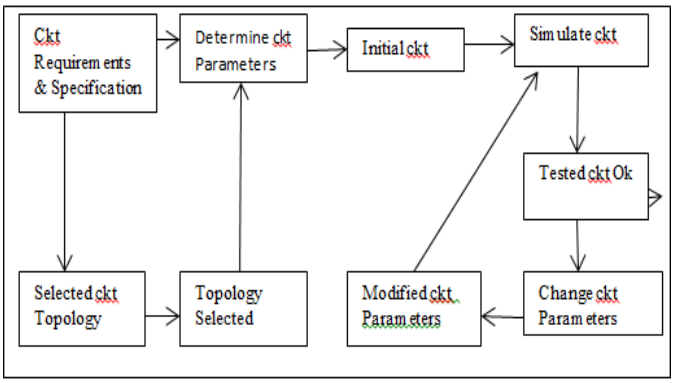

Fig.3 Design procedure and methodology for various Topologies of sensing circuits

Initially circuits are designed using standard topologies, parasitic are decided, the process technology is chosen and circuits are simulated if not found ok are changed and resimulated for numerous topologies selected.

IV. C5 Process Technology

Scalable CMOS (SCMOS) is a set of logical layers together with their design rules, which provide a nearly process- and metric-independent interface to many CMOS fabrication processes available through MOSIS [19]. In the SCMOS rules, circuit geometries are specified in the lambda based methodology. The unit of measurement, lambda, can easily be scaled to different fabrication processes as semiconductor technology advances. Optimized for 5 V mixed-signal applications, the C5 process family from ON Semiconductor offers a medium-density, high-performance mixed-signal technology capable of integrating complex analog functions, digital content.

Features [20]

2 or 3 metal layers
Poly to poly capacitors
High voltage I/O – 12/20 V
High-resistance poly
Low-voltage modules

V. Design and Experimental Data

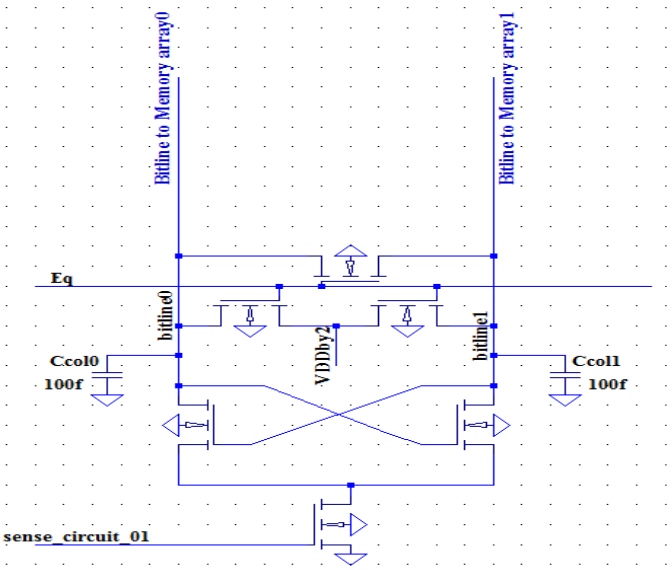

Fig.4 Schematic for sense amplifier design topology 1

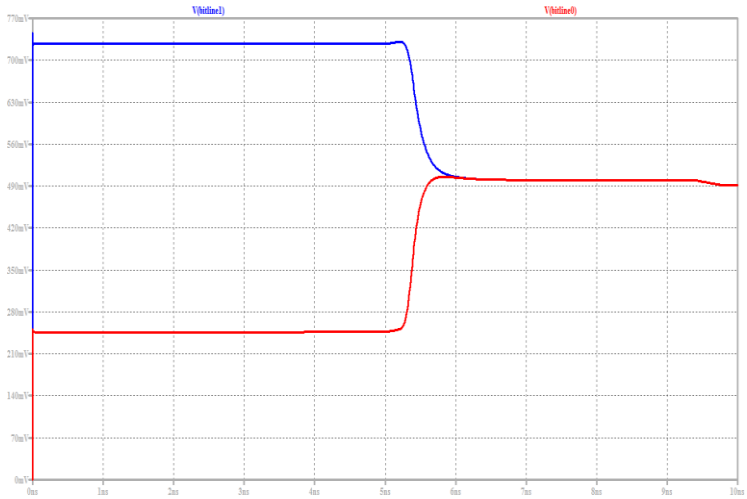

Fig.5 Transient simulation plot for bitline1 and bitline0

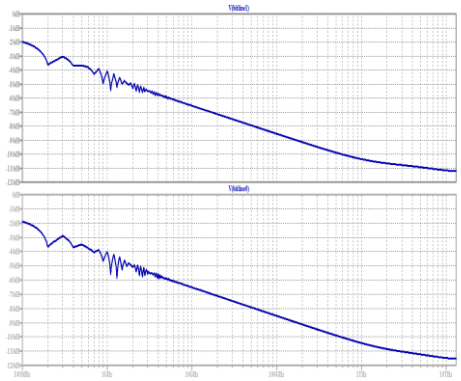

Fig.6 FFT plot for topology1 bitline1 and bitline0 from100 MHz to 10 THz

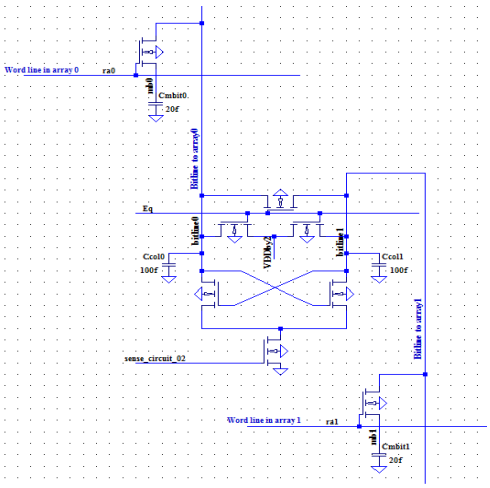

Fig.7 Schematic for sense amplifier design topology 2

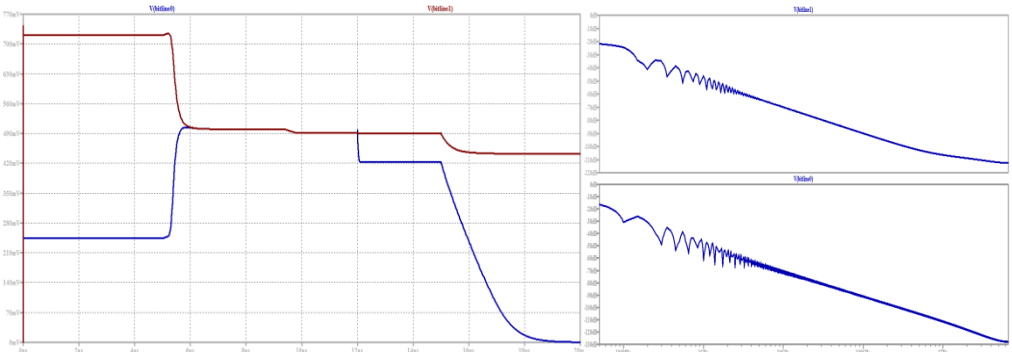

Fig.8 Transient simulation plot for bitline1 and bitline0 **Fig.9** FFT plot for topology1 bitline1 and bitline0 from100 MHz to 10 THz

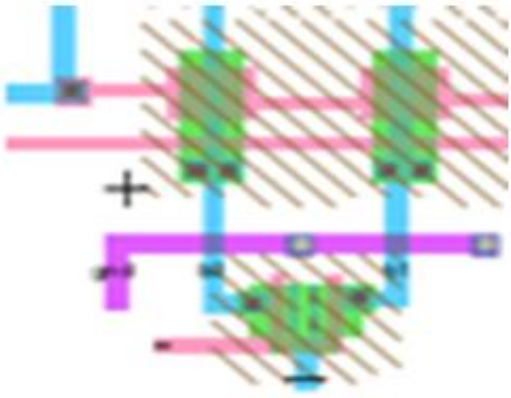

Fig.10 Layout view for sense amplifier interfacing to memory bit

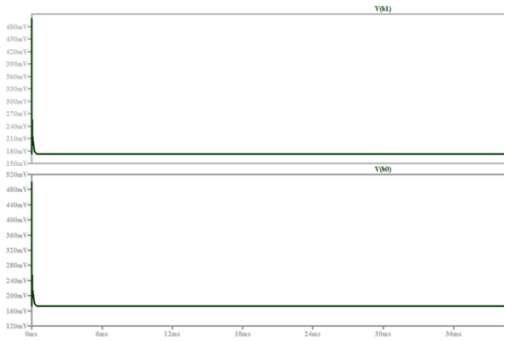

Fig.11 Transient simulation plot for interfacing sense amplifier with DRAM memory array

VI. Results

The results and FFT analysis is done for the above mentioned topologies and is tabulated below Topologies presented above are simulated for VDD value 1 volts and suitable column capacitance with a reference signal is also provided in the form of a suitable pulse and transient analysis is done for 10 nanoseconds. The bit lines are equilibrated first to VDD/2 and any one of them will be pulled to VDD during sense operation

.

Table 1.1 Table enlisting Frequency, Magnitude, Phase and Group Delay for sense circuit topology 1 for bitline1

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	100 MHz	-19.93 dB	-9.3288°	-2.077ns
2.	1 GHz	-41.17 dB	-85.169°	-556.9ns
3.	10 GHz	-65.52 dB	-90.670°	3.32 ps
4.	100 GHz	-85.46 dB	-94.93°	-1.35ps
5.	1THz	-103.5 dB	-132.96°	124.06 fs
6.	10THz	-111.65dB	175.35°	-3.39fs

Table 1.2 Table enlisting Frequency, Magnitude, Phase and Group Delay for sense circuit topology 1 for bitline0

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	100 MHz	-18.92 dB	83.15°	-2.346ns
2.	1 GHz	-40.49 dB	103.26°	23.88 ps
3.	10 GHz	-65.18 dB	90.01°	-9.42 ps
4.	100 GHz	-85.16 dB	92.42°	-4.45ps
5.	1THz	-104.4 dB	113.72°	163.6 fs
6.	10THz	-114.88 B	167.48°	-11.4 fs

Table 2.1 Table enlisting Frequency, Magnitude, Phase and Group Delay for sense circuit topology 2 for bitline1

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	100 MHz	-24.5 dB	-98.87°	1.79ns
2.	1 GHz	-47.60 dB	-100.7°	2.57ns
3.	10 GHz	-70.16 dB	-90.38°	9.37ps
4.	100 GHz	-90.02 dB	-97.99°	-20.ps
5.	1THz	-106.54dB	-151.3°	277 fs
6.	5 THz	-112.18 B	176.28°	1.11ps

Table 2.2 Table enlisting Frequency, Magnitude, Phase and Group Delay for sense circuit topology 2 for bitline0

S.no	Frequency	Magnitude	Phase	Group Delay
1.	100 MHz	-30.69 dB	-119.2°	-2.97ns
2.	1 GHz	-56.38 dB	-116.1°	2.91 ns
3.	10 GHz	-71.52 dB	-88.44°	991.1ps
4.	100 GHz	-91.14dB	-91.68°	-97.8ps
5.	1 THz	-111.66dB	-112.32°	65.61ps
6.	5 THz	-127.15dB	-168.6°	35.81ps

VII. Conclusion

With design technology, it would be possible to implement, verify and test sensing circuits. Using proper CMOS models and design technology above four sensing topologies are implemented. This paper explains various design quality matrices and transients using proper parasitic for bitline and wordline. A detailed FFT is also done for all the topologies and values for magnitude, phase and group delays are calculated for bitline0 and bitline1 for frequency range from 100MHz to 10 THz using proper CAD tools for VLSI.

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