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Implementation of Fault Tolerant Parallel Filters Using ECC Technique

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Abstract: *In this paper, using hamming code technique the parallel FIR filters is designed and implemented. In DSP systems the digital filters are very important and in present days the complex circuits are designed and reliability is an important criteria. Fault tolerant parallel FIR filters are to be implemented for reliability purposes. Using case study the improvements in error correction and circuit cost is determined. By using this hamming code technique, the FIR filter is considered as a bit. By using more filters the area is increased and the delay is reduced to improve performance of the circuit.*
Key Words**:** *Faults, Parallel FIR filters, Hamming codes*

I. Introduction

In present days, the Nano technology is using many applications & their reliability is becoming very difficult to face these challenges like faults the fault tolerant parallel filters are used to add redundancy. The simple technique used is Triple Modular Redundancy(TMR) technique and the block diagram for TMR is shown in figure 1,

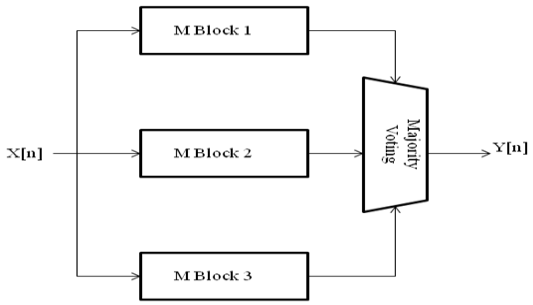

Fig 1: TMR technique

In this technique, the inputs are given to three similar 'M' blocks and by using majority voting the errors are corrected.TMR is simple to design but the demerits of this technique is the area & power is increased and it does not suits for large number of filters. By using Hamming code technique the single errors can be corrected and by increasing parallel filters the FIR filter the performance of the circuit increases. By using one redundant module, the single fault correction is done. In section 2 the FIR filter design & in section 3 parallel filters with same response is discussed and in section 4 the proposed system and case study is implemented and in section 5 the synthesis and simulation results & in section 6 conclusion is discussed.

II. Fir Filters

For high performance applications the FIR filter design is used.These filters are easy to design to match a given response and they have good stability.The block diagram for general FIR filter is shown in fig 2.

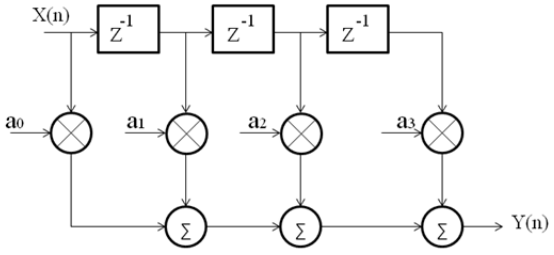

Fig 2: General FIR Filter

The FIR filter equation is given as,

$$y[n] = \sum_{i=0}^{N-1} x[n - i].h[i] \qquad \text{……(1)}$$

Where,

x[n] is input signal, y[n] is output signal and h[i] is impulse response.

III. Parallel Filters With Same Response

Consider a set of 'K'parallel filters with same response and different input signals.The block diagram for parallel filters is shown in figure 3.

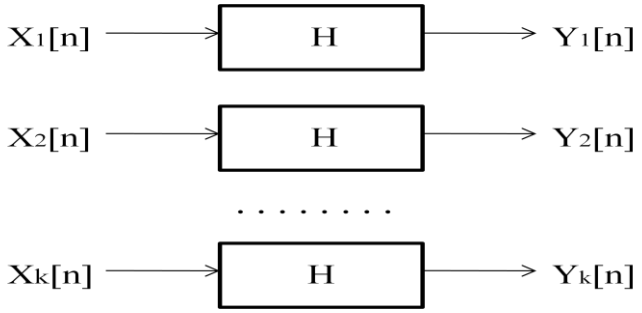

Fig 3: Parallel Filters With Same Response

By using Hamming codes the protection of parallel FIR filters is done and Hamming codes are used to correct single errors and it can detect double bit errors.The Rule for finding parity bits using Hamming codes is given as,

$$2^P \geq x+p+1 \qquad \text{…(2)}$$

Where, X denotes number of data bits & P denotes number of parity bits.

IV. Proposed Method

Consider parallel FIR filter using hamming code with message bits '4' and total bits as '7' to obtain parity bits as '3'.The parity bits are calculated by using the data bits and the parity bit equations are calculated as,

p1=d1 xor d2 xor d3
p2=d1 xor d2 xor d4
p3=d1 xor d3 xor d4

…….(3)

By using the actual input data,the error bits present in any of the bit are stored & replaced with that data.To find the parity bit errors the outputs are compared with the stored results.By using the generating 'G' matrix and parity check 'H' matrix the Hamming Code is represented as,

$$G = \begin{bmatrix} 1&0&0&0&1&1&1 \\ 0&1&0&0&1&1&0 \\ 0&0&1&0&1&0&1 \\ 0&0&0&1&0&1&1 \end{bmatrix} \qquad H = \begin{bmatrix} 1&1&1&0&1&0&0 \\ 1&1&0&1&0&1&0 \\ 1&0&1&1&0&0&1 \end{bmatrix}$$

From above example,

The error in d1 results the errors on p1,p2,p3 check bits and the error in d2 results errors on p1 and p2 and an error in d3 results on p1 and p3 and finally error in d4 results on p2 and p3.

The error bit position is shown in table 1 as,

S_1 S_2 S_3	Error Bit Position	Action
0 0 0	No Error	None
1 1 1	d1	Correct d1
1 1 0	d2	Correct d2
1 0 1	d3	Correct d3
0 1 1	d4	Correct d4
1 0 0	p1	Correct p1
0 1 0	p2	Correct p2
0 0 1	p3	Correct p3

Fig 4: Error Location In Hamming Code

The block diagram for 4 parallel FIR filters & hamming code is given in figure 4,

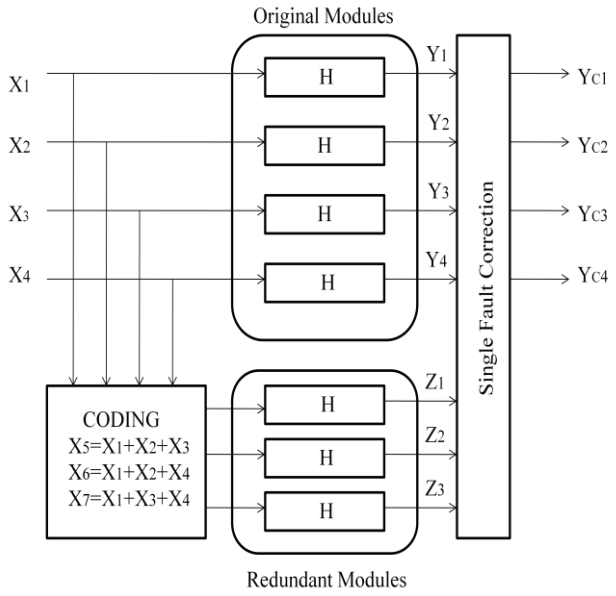

Fig 5: Hamming code technique For 4 Filters

The Encoding is calculated as,

$$y = x \bullet G \qquad \text{……..(4)}$$

For identifying the position of the error bit i.e., syndrome is calculated as,

$$S = y \bullet H^{T} \qquad \text{……..(5)}$$

Where '•' denotes XOR and multiplication operation.After finding the eerror bit,the error bit is inverted to get the final correct output.

The check filters Zj is calculted as,

$$Z_1[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_3[n-l]) \cdot h[l]$$

$$Z_2[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_4[n-l]) \cdot h[l]$$

$$Z_3[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_3[n-l]+X_4[n-l]) \cdot h[l]$$

…….(6)

Checking is done by,

$$Z1[n]=Y1[n]+Y2[n]+Y3[n]$$
$$Z2[n]=Y1[n]+Y2[n]+Y4[n]$$
$$Z3[n]=Y1[n]+Y3[n]+Y4[n]$$

If an error on Y1 is detected then the error is corrected by,

$$Yc1[n] = Z1[n] - Z2[n] - Z3[n] \quad \ldots\ldots(7)$$

The ECC technique can be used for more number of parallel filters to provide effectiveness in error correction and to improve performance.

Consider a block of eleven parallel filters for hamming code with k=11 and n=15 is implemented.Mainly the proposed scheme is based on four factors. Theyare Encoding, syndrome calculation, Error analysis and single fault correction. For eleven parallel filters only four redundant modules are used. The reliability is more for 11 parallel filters than 4 parallel filters .The reductions for eleven parallel filters are large only where the number of filters are increased. By using ECC's as the area increases, the delay decreases.

Consider an example with generating matrix 'G' and Parity 'H' matrix is,

$$G = \begin{bmatrix} 100000000001100 \\ 010000000001010 \\ 001000000000110 \\ 000100000001110 \\ 000010000001001 \\ 000001000000101 \\ 000000100001101 \\ 000000010000011 \\ 000000001001011 \\ 000000000100111 \\ 000000000011111 \end{bmatrix} \quad H = \begin{bmatrix} 110110101011000 \\ 101101100110100 \\ 011100011110010 \\ 000011111110001 \end{bmatrix}$$

The block diagram for eleven parallel filters is shown in figure 5.

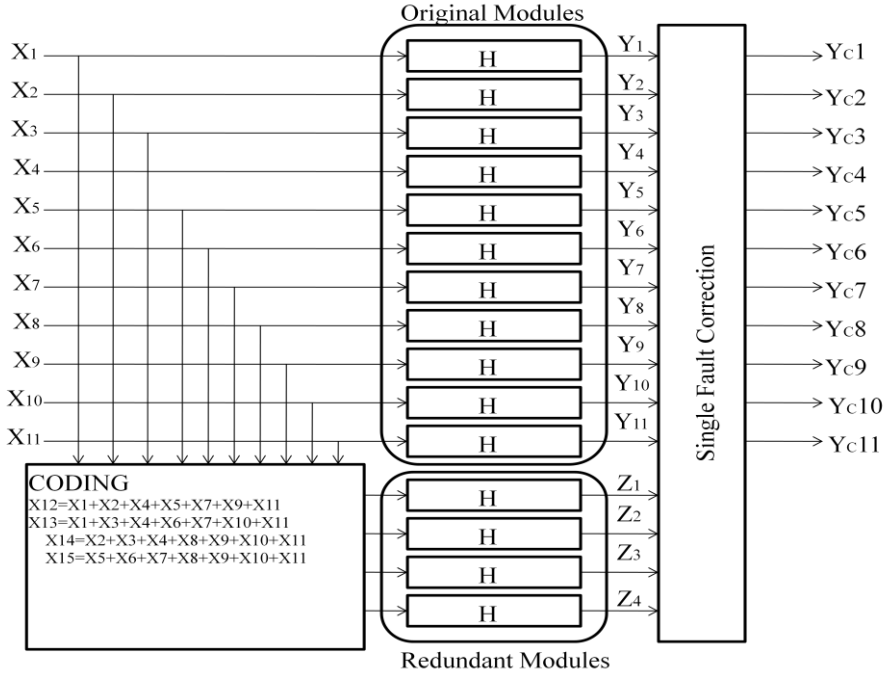

Fig 6: Hamming code technique For 11 Filters

The area is increased by using the eleven parallel filters and the time period is reduced to improve the performance when more number of filters used in design.Finally,the effectiveness in error detection and correction is evaluated by using the case study. Consider a set of parallel FIR filters with the input data and coefficients. Two evaluations are implemented for a block of parallel filters with data bits k=4 & k=11 and total bits n=7 & n=15 bits. These techniques are synthesized and simulated by using a tool Xilinx Spartan 3E. The fault injection experiments and effectiveness in terms of error correction is done by using eleven parallel filters. For input filters and the coefficients the errors are injected randomly and in all these cases the single errors can be injected in various simulations can be detected and corrected. So, by using case study the effectiveness is confirmed to correct the single errors and system cost is determined.

V. Synthesis &Simulation Results

The RTL Synthesis and Simulation results for proposed system are given below.

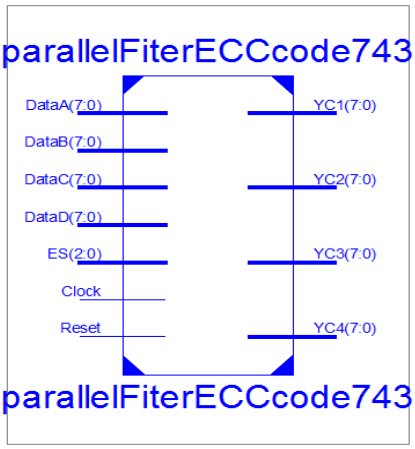

Fig 7: RTL Schematic for 4 Parallel Filters

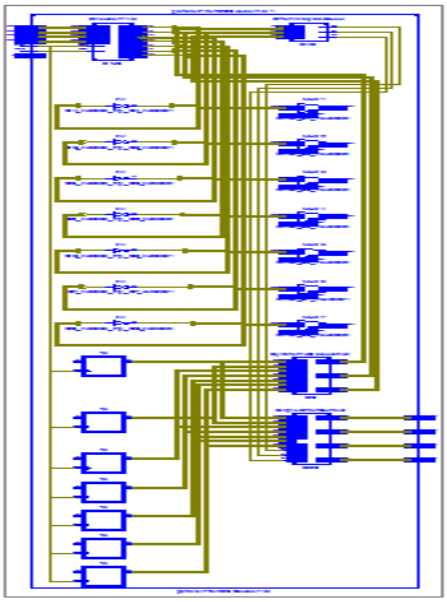

Fig 8: Internal Diagram for 4 Parallel Filters

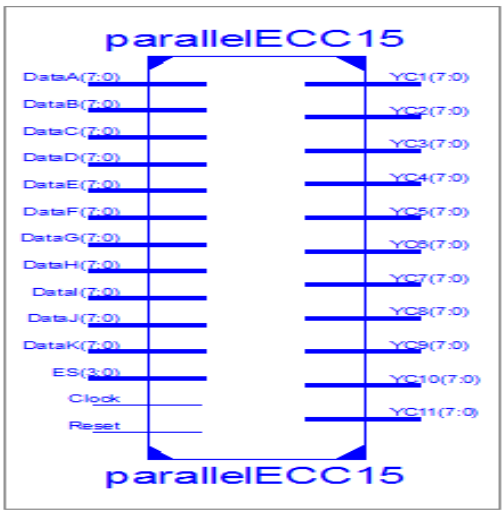

Fig 9: RTL Schematic for Eleven Parallel Filters

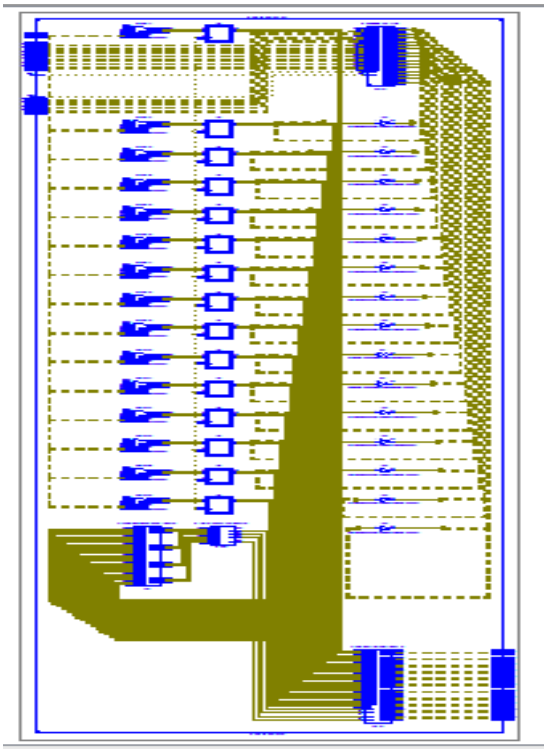

Fig 10: Internal Diagram for 11 Parallel Filters

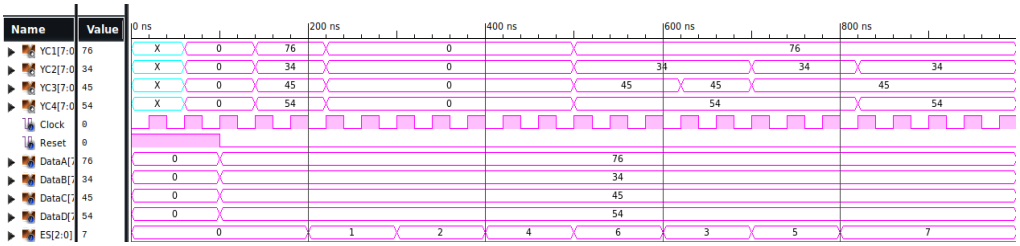

Fig 11: Simulation Result for 4 Parallel Filters

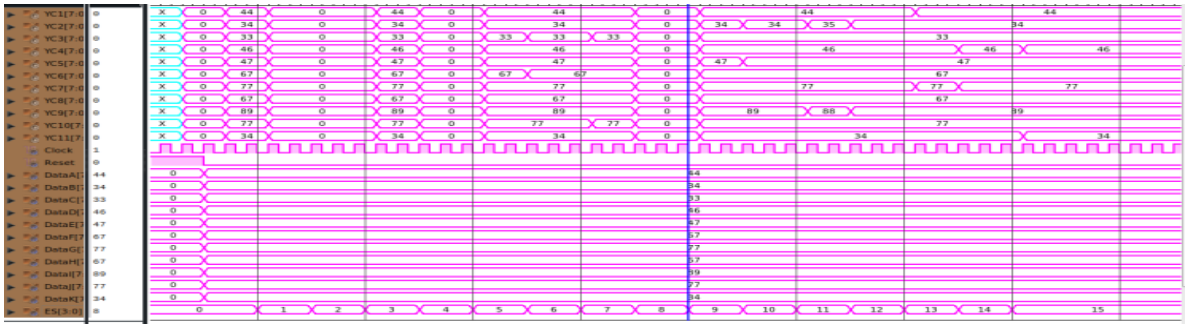

Fig 12: Simulation Result for 11 Parallel Filters

Performance Analysis:

Design	Area (No.of Flipflop's)	Delay	Frequency
Hamming code for 4 filters	112	15.43 nsec	493.390 MHz
Hamming code for 11 filters	240	9.172nsec	485.909MHz

VI. Conclusion

By using the proposed scheme the protection of parallel FIR filter can be done in DSP systems. The error detection and correction is done by applying ECC's to parallel filter outputs.The effectiveness i.e., circuit overheads and single fault correction is discussed by using case study.

The future scope is the scheme is also done for IIR filters instead of FIR filters. Another extension is instead of using hamming codes another error correction codes can be used.

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