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FPGA Implementation of ALU using Vedic Mathematics

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Abstract: *Arithmetic and Logic Unit (ALU) is the most crucial and core component of central processing unit as well as of number of embedded systems and microprocessors. ALU consists of many computational units like adders, multipliers, logical units etc. Vedic Mathematics concepts are proposed here for designing the computational units of an 8-bit ALU. Here, a high-speed 8×8 bit multiplier is proposed which is based on the Vedic multiplier mechanism. A divider based on vedic mathematics is also proposed here. The proposed Vedic mathematics based ALU is designed using high level hardware description language – Verilog, followed by synthesization using EDA tool, Xilinx ISE 14.1. Finally, the synthesized circuit has been implemented on Xilinx Spartan-6 Field Programmable Gate Array (FPGA) device.*

Keywords: *ALU, FPGA, Vedic mathematics, Verilog – HDL, Xilinx ISE 14.1*

I. Introduction

Arithmetic Logic Unit (ALU) is the main part of the Central Processing unit which performs various arithmetic and logical operations. The speed of arithmetic unit is of extreme importance and depends greatly on the speed of multiplier. Therefore, the technologies are always looking for new algorithm and hardware so as to implement this operation in much optimized way in the terms of area and speed. Vedic Mathematics deals with various branches of mathematics like arithmetic, algebra, geometry etc. The use of Vedic Mathematics concepts in the computation algorithm of a processor will reduce the complexity of execution time, area and power consumption etc. The efficiency of Urdhav Triyagbhyam Vedic method for multiplication, strikes a difference of actual process of multiplication, by enabling parallel generation of intermediate product, eliminating unwanted multiplication steps with zeros and scaled to higher bit level. This formula (Sutra) can used to build high speed power efficient multiplier in a processor.Nikhilam division algorithm just involves the addition of numbers which is very much different from the traditional division technique including multiplication of big numbers by the trial digit of the quotient at each step and subtracts that result from dividend at each step. This work aims to design arithmetic and logic unit using the technique of ancient Indian Vedic Mathematics to improve the performance of a processor.

II. Related Work

Many researchers have proposed ALUs and other computational units implemented based on the concepts of ancient Indian Vedic Mathematics concepts for different signal processing applications. These designs have proved to be robust compared to conventional arithmetic computational algorithms.Garima Rawat et al. [1] have proposed an ALU design using Vedic Mathematics approach. A high-speed 8×8 bit multiplier is designed and analyzed which is based on the Vedic multiplier mechanism. This architecture is diverse from the conservative method of employing product of two numbers accomplished by the process of add and shift. The proposed method is efficient and fast, wherein the processing involves the vertical and crossed multiplication of precedent Vedic mathematics.

Rahul Nimje et al. [2] have proposed an ALU design using Vedic Mathematics approach. As the ever increasing demand in enhancing the ability of coprocessor to handle the complex and challenging processor as resulted in integration of number of processor cores into single chip, but still the load on the processor is not less in generic system. This load is reduced by connecting the main processor with co processor, which are designed to work on the specific types of function like numeric computation, signal processing, image processing and arithmetic operation. The efficiency of Urdhav Triyagbhyam Vedic method for multiplication, strikes a difference of actual process of multiplication, by enabling parallel generation of intermediate product, eliminating unwanted multiplication steps with zeros and scaled to higher bit level. This formula (Sutras) is used to build high speed power efficient multiplier in coprocessor.

Abhishek Gupta et al. [3] have proposed an ALU design using Vedic Mathematics approach. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. That's why it highly required designing high speed ALU, which can enhance the efficiency of those modules which lies upon the operations performed by ALU. The proposed ALU is able to perform three different

arithmetic and eight different logical operations at high speed. Suchita Kamble et al. [4] have proposed VHDL implementation of 8-bit arithmetic logic unit (ALU). ALU consist of two input registers to hold the data during operation, one output register to hold the result of operation, 8-bit fast adder with 2's complement circuit to perform subtraction and logic gates to perform logical operation. The maximum propagation delay is 13.588 ns and power dissipation is 38 mW. The ALU was designed for controller used in network interface card.

S.P.Pohokar et al. [5] have proposed VHDL implementation of 8-bit arithmetic logic unit (ALU). Vedic technique eliminates the unwanted multiplication steps thus reducing the propagation delay in processor and hence reducing the hardware complexity in terms of area and memory requirement. Surabhi Jain et al. [6] have proposed that VLSI architecture have higher orders of time and space complexities. Vedic Mathematics on the other hand offers a new holistic approach to mathematics. In this work, optimized binary division architecture has been designed using sutras of Vedic Mathematics which are Nikhilam Sutra and Parvartya Sutra. This work discusses about these two algorithms of division and their application for calculating deconvolution.

Abhyarthana Bisoyil et al. [7] have proposed that Binary multipliers and addresses are used in the design and development of Arithmetic Logic Unit (ALU). The objective of this paper is to implement digital multipliers based on the concept of Vedic mathematics. In order to develop a digital multiplier, Urdhva-tiryakbyham sutra of Vedic mathematics is used to implement vertical and cross wise operations. Since these are digital multipliers, they are implemented on FPGA board.

III. System Design

Fig.1 shows the block diagram of the proposed Vedic Mathematics based ALU design. The latches are used to store the two binary inputs and output result of an arithmetic or logic operation. The multiplexer is used to route the result of a selected operation to the output latches. The ALU performs arithmetic and logical operations. The ALU has two sub-units: an arithmetic unit based on Vedic Mathematics to perform arithmetic operations and a logic unit to perform the logical operations.

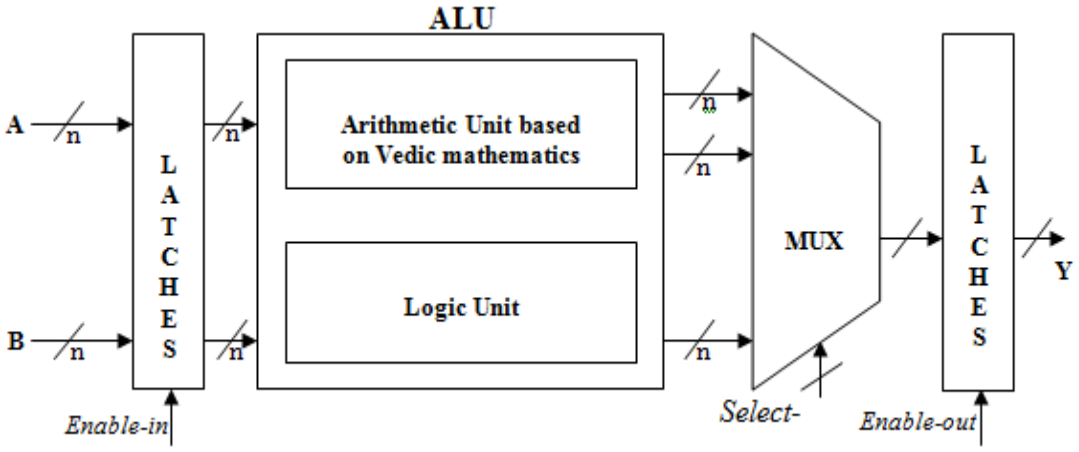

Fig.1 Block diagram of the proposed vedic mathematics based ALU

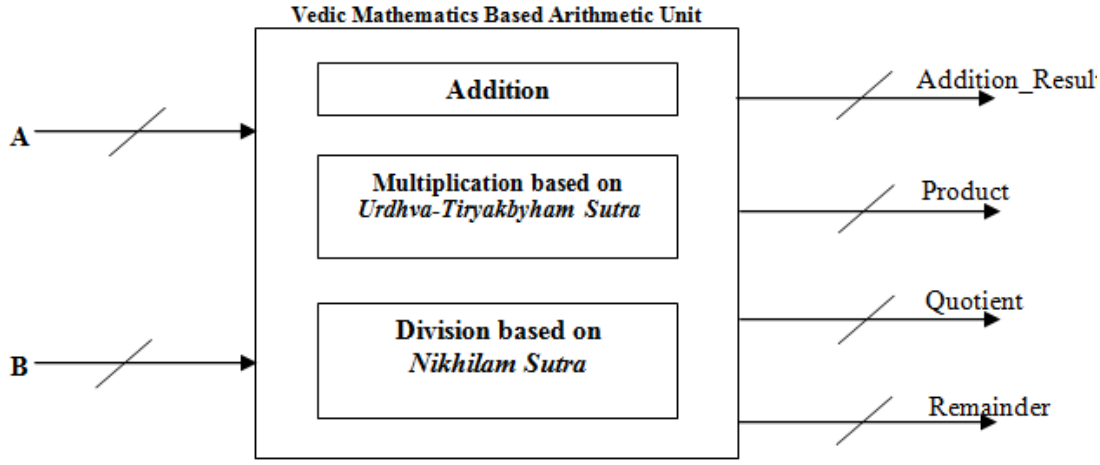

Fig. 2 Block diagram of arithmetic unit of the ALU

Fig.2 shows the block diagram of the Vedic Mathematics based arithmetic unit of the ALU. The addition is carried out using robust adders. The multiplication is carried out using the Urdhva-Tiryakbyham Sutra. The Urdhva-Tiryakbyham Sutra is used to construct 2x2 multiplier blocks. Several such 2x2 multipliers along with ripple carry adders are used to design 4x4 multiplier blocks. This procedure is repeated to obtain the higher order multiplier blocks. The binary division is carried out using Nikhilam Sutra.

The 8-bit vedic mathematics based ALU has the following modules:

1. Adder (8 - bit) – Designed using ripple carry addition scheme
2. Subtractor (8 - bit) – Designed using ripple carry scheme
3. Multiplier (8 - bit) – Designed based on vedic mathematics principles
4. Divider (8 - bit) – Designed based on vedic mathematics principles
5. Logic unit (8 - bit)

Fig.3 depicts 8×8 multiplier based on Vedic methodology. The process of multiplication is accomplished using four bits simultaneously feeding to the 4-bit multiplier unit and its output is added further to obtain the end result of two 8 bit numbers.

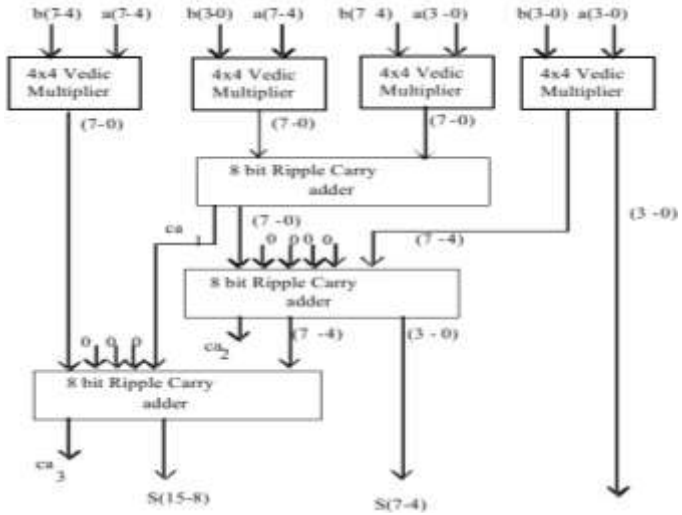

Fig.3 Implementation of 8x8 bit Vedic mathematics based multiplier

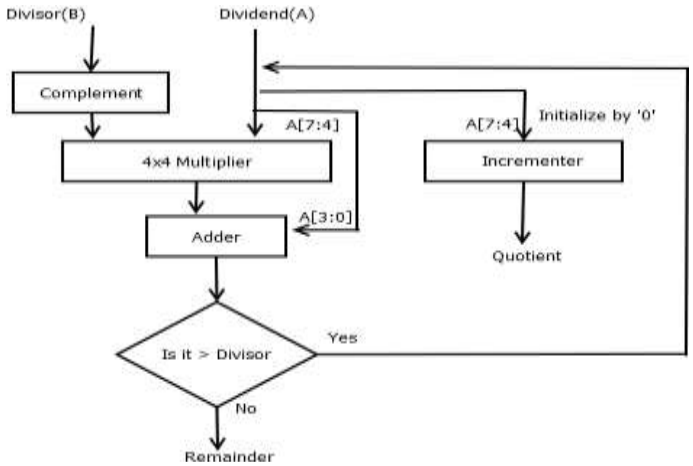

Fig.4 Flowchart of division operation using Nikhilam Sutra

Flow chart diagram of the proposed divider using Nikhilam formula for 8 bit by 4 bit which has been adopted from ancient Vedic Mathematics has been shown in Fig. 4. Assume that, A and B are dividend and divisor respectively. The 'n' bit input from divisor is fed to the complement circuitry. Complement methodology that has been used here, is the two's complement method. The result of complement is fed to the multiplier with 4 MSB of dividend and same 4 MSB of dividend is fed to the incrementer which is initialized by '0'. The result of multiplier is fed to the adder with 4 LSB of dividend. If the result of the adder is greater than divisor then the output from the adder is again fed to the multiplier as a new dividend. The operation is repeated again until the result of the incrementer is n/2 bit or n/2+1 bit. The output from the adder is the actual remainder and the result of the incrementer is the quotient.

IV. Results

The simulation results for various operations of the ALU are shown in Fig.5. Isim simulator of Xilinx EDA tool is used for simulation.

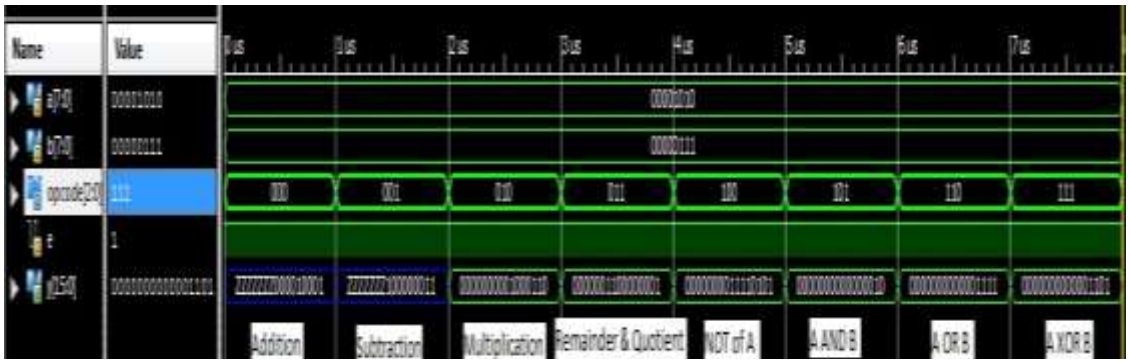

Fig.5 Simulation waveforms of ALU module

Fig.6 and Fig. 7 show the results of multiplication and division obtained from Mimas V2 Spartan 6 Development Board. For example, the inputs A = 6 and B = 3. The product and quotient are shown in Fig.6 and Fig.7 respectively.

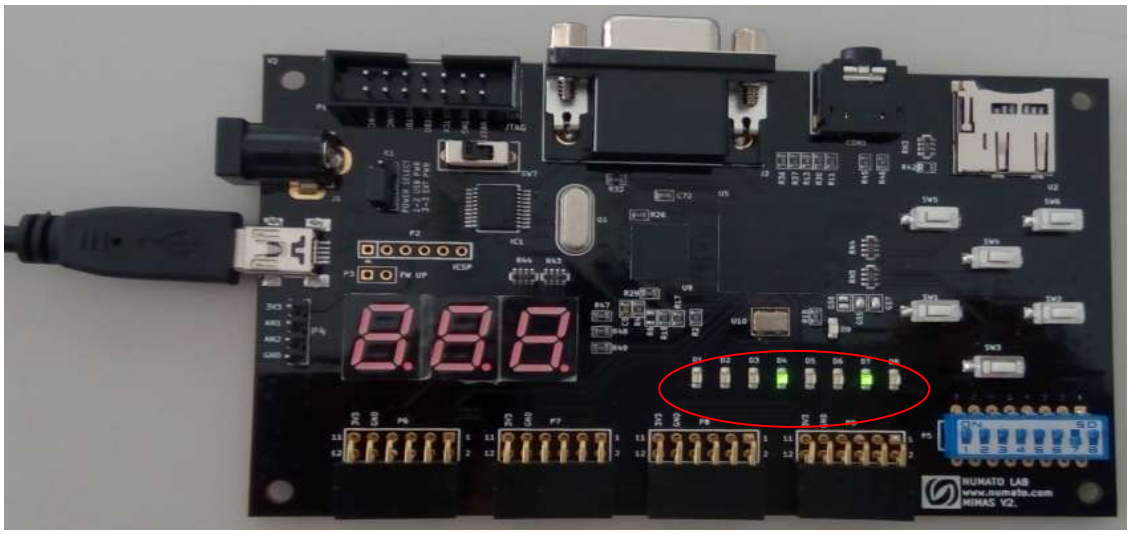

Fig.6 Multiplication result

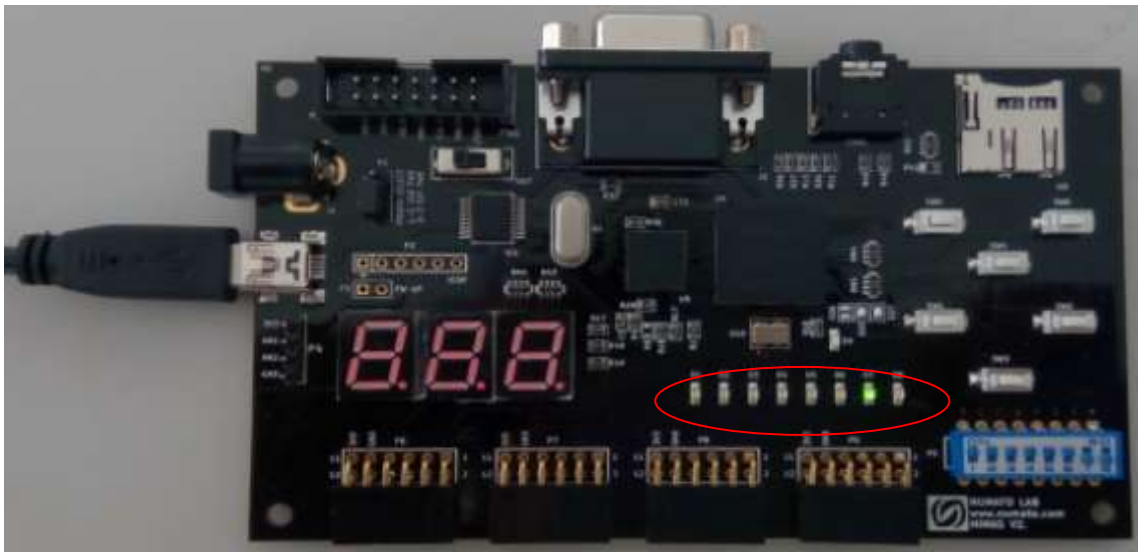

Fig.7 Division result

V. Conclusion

Vedic Mathematics concepts for various mathematical computations are proved to be efficient as compared to conventional methods. Many researchers have proposed computational units based on Vedic Mathematics for various signal processing applications and these designs are proved to be efficient ones. The proposed Vedic Mathematics based ALU uses Urdhva-Tiryakbyham Sutra and Nikhilam Sutra for the implementation of multiplication and division respectively. The proposed ALU architecture would find application in various signal processing areas.

FPGA is advantageous in terms of cost, development time, cost, maintainability and practicability. Stability and minimizing the tendency of mistakes in designs can be solved with all designs in FPGA. FPGA is used to upgrade obsolete integrated circuits reduces hardware circuit board changes, increases productivity, and ensures that the operational constraints are met.

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