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Fault Detection and Diagnosis

[1]S Vinayaka Babu, [2]K V Ramana Reddy& [3] Siva S Yellampalli
[1]*Author of Fault Detection and Diagnosis, VLSI Design and Embedded Systems, VTU Extension Centre, UTL Technologies, Bangalore,*
[2]*Assistant Professor, VTU Extension Centre, UTL Technologies, Bangalore*
[3]*Professor, VTU Extension Centre, UTL Technologies, Bangalore,*

Abstract: *This paper describes about the ability of a system to detect the fault and diagnose of the test board by using generic logic array (GAL). It has been very popular in defense sectors like military systems, aerospace and medical instruments as well as in security and safety applications. The methodology used in this is "repair on the go" which detects the fault IC on the board that is under the test, then that fault IC is controlled by one of the columns of GAL. The fault pin of that IC can be visualized using a seven segment display and audio representation with the help of a buzzer. This method increases the life line of the system and this methodology can also be implemented using FPGA's.*

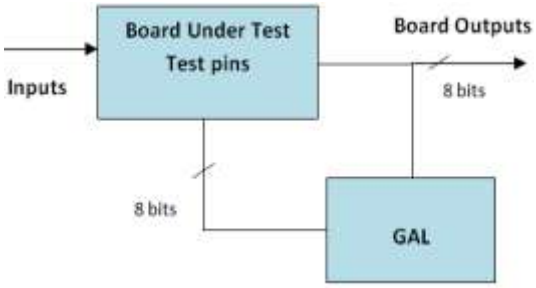

Figure 1: Block Diagram

I. Introduction

Since the evolution of the VLSI applications, there has been a tremendous amount of applications built with difficult complexity. As the complexity kept on increasing the testing of the application becomes even more complex. The demand of ASIC (Application-Specific Integrated Circuit) applications gave rise to more sophisticated computer aided design (CAD) tool, which has played an important role in testing. To overcome the utilization of expensive tools we have come up with a low-cost and easy solution "Programmable Logic Devices (PLD)".

PLD's are one of the best evolutions in the history of electronics, it is an electronic component used to build reconfigurable digital circuits and which led from PLA's to PAL, GAL, CPLD and FPGA. These devices do not have a defined function once manufactured, unlike the logic gates which has to be programmed first and then use it. PLD's plays a major role in the modern systems, due to its reprogrammable ability. These devices are used to obtain the required logic output, but by reprogramming feature of semiconductors they have replaced flip flops, multiplexers, logic gates and many more custom applications. It uses various technologies like fusible links and E^2CMOS (Electrically Erasable Complementary Metal Oxide Semiconductor). Therefore, as the complexity of system increases the chips geometry decreases which in turn increases the fault in the components.

The PLD used to overcome the faults of the IC on test board is generic array logic (GAL). GAL has E^2PROM feature that is programmable AND array with E^2CMOS cells.

II. Design Scenario

Initially, the testing happened only on the printed circuit boards (PCB) which was then applied on IC's. There is not much difference between IC testing and PCB testing as their aims is same like test and discards the faulty IC or board respectively, rather than detecting the defect and replacing that part.

The assumptions were made that the board is working perfectly. The system is designed to get into the network of blocks to realize the separate integrated circuits. Each block is considered as repairable GAL. As GAL consists of mesh that is array of AND gates and OR gates arranged in column and rows respectively. The columns are connected to the board's test pins.

As the board consists of IC's, taking the concept of boundary scan the outputs of the IC's are connected to the test pins. In turn, those test pins are connected to the inputs of the GAL. As the board is put under test, board is given the test vectors and expected for outputs. But if there is a defect in an IC's output pins then that output pin is replaced by the GAL. In this case, GAL is also used to indicate the fault IC's pin number by displaying using seven segment and simultaneously an alarm to indicate there is some fault. This mechanism is termed as "Repair on the Go" and by this mechanism the test boards can be diagnosed. Therefore, defects on the test boards can be detected with audio and video indication.

III. Implementation

Consider the two board's one is testing board and other one is GAL board. In the testing board all the output pins are connected to the test points. Similarly, the inputs pins of the GAL are connected to the test points of the test board that is the output pins of test board and input pins of GAL are connected to same test points of the test board. When the testing program runs on the testing board and if there is an issue in getting the output, then that test pin is connected to the GAL IC and the output is obtained on temporary bases. The test pin which is fault on the test board, that test pin number is displayed on the seven segment display and also an alarm is raised on the identification.

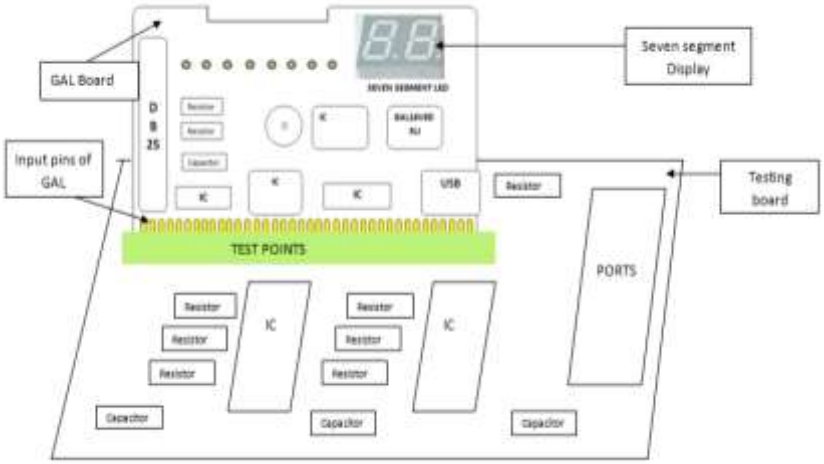

Figure 2: Board Connection

IV. Results

The outputs of the testing programs are simulated using WinCUPL software which is provided by Atmel. A simple logic is implemented on the board by giving its input and the output is expected in waveforms as shown in the figure 3. In these waveforms, the outputs obtained have some untested waveform.

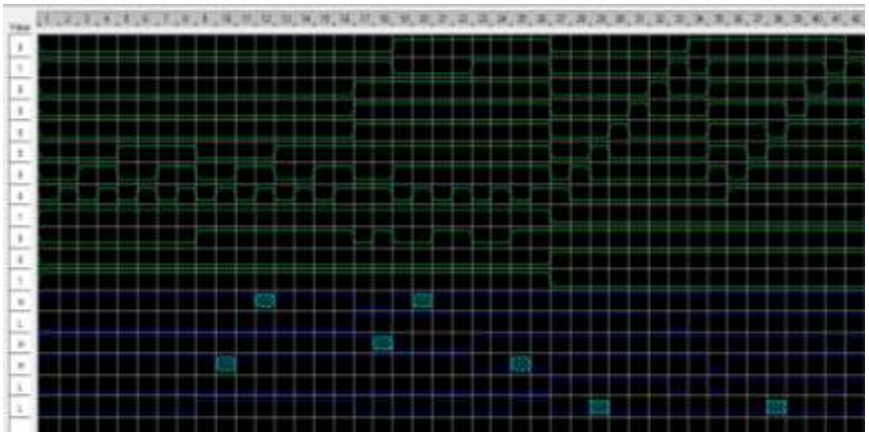

Figure 3: Wave form indicating the untested part of the inputs

In the figure 3, the green lines indicate the inputs and the blue lines indicate the output. The light blue mesh structures in the output lines indicate that there is some problem with the output. The problem in the output represents that an IC is not working or some pin of IC is not working. After finding this error, the test board output lines are connected to the input lines of GAL board and then outputs are obtained.

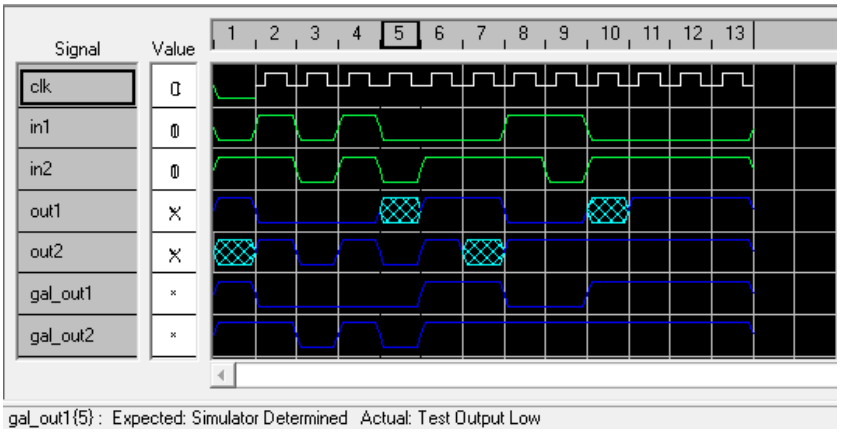

Figure 4: Wave form corrected by GAL and its output

In figure 4, the untested output (mesh) occurred in figure 3 has been corrected by using GAL board. For example, at the 5th vector column that is for "out1", the expected output is low. This was corrected by GAL IC then it is simulated and the corrected output waveform is represented for gal_out1.

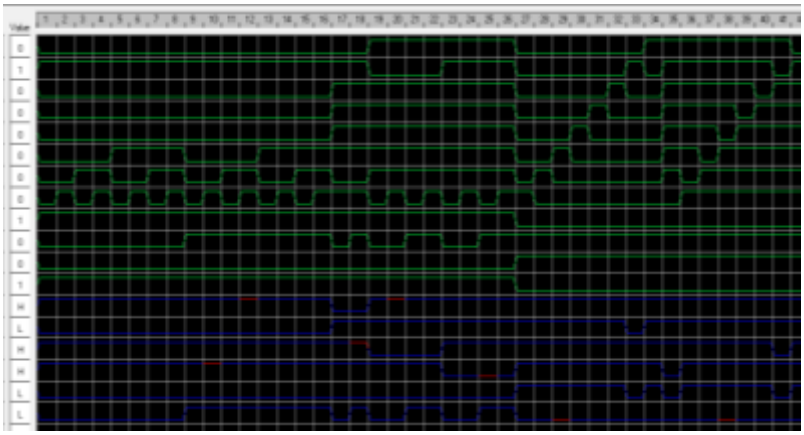

Figure 5: Wave form corrected by GAL

In the figure 5, the waveform shows that the outputs in red colored are corrected by the GAL that is the "repair on the go" concept. This indicates that the Board is functioning correctly but that IC is at fault.

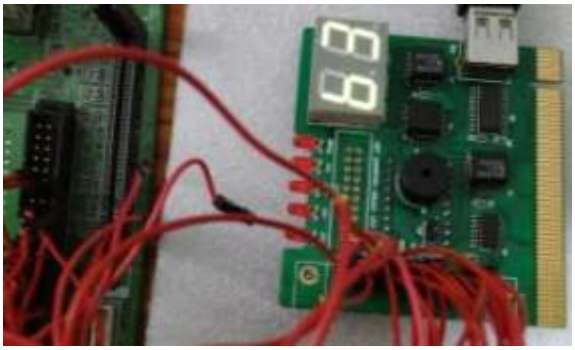

Figure 6: board displaying the number of the IC

In the figure 6, the seven segments displays the fault pin of test board IC. Also the buzzer indicates that an IC is at fault.

V. Conclusion

This paper is only an attempt to introduce the concept of "repair on the go". This concept has been presented with the help of GAL, whereas this implementation can also be applied to FPGAs. This concept was adapted to find the faulty IC and diagnose it, instead of assuming that the board is at the fault and replace it completely. The test pins of the board under test is connected to the GAL's input which act as temporary link between the output of the board under test and the GAL board. For the future enhancement this concepts can be implemented using hardware design languages for higher end boards like FPGAs.

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Mr. S VINAYAKA BABU
BE, MTech (VLSI)