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Optimized Design of Column Level ADC for CMOS Imager using 180 nm Technology

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Abstract: *An integrating type ADC is the most commonly used column level ADC for its simple architecture and small surface area. 12-bit Dual slope ADC is developed which has less complexity in design. This architecture has basic advantage that it eliminates the dependence of the conversion on the linearity and accuracy of the slope. The main block of this circuit is opamp. Two stage opamp is developed which has gain of 78dB. Dual slope integrator is designed which has one resistance in feed forward path and one feedback capacitance with opamp circuit. This dual slope column level ADC minimizes the conversion time. CMOS process is used because it provides high integration capabilities. This column level dual slope ADC is implemented using 180nm technology.*

Keywords - *ADC, CIS, CMOS, OPAMP, Pixel*

I. Introduction

The demand of CMOS imager is increasing day by day. This is due to growth in mobile imaging, video imaging camera, industrial machine vision and optical sensors. This situation is expected to continue with increasing demands from emerging applications in biomedical imaging, remote sensing, digital surveillance, sensor networks and robotics etc [1]. Popularity of these devices depends on small surface area, speed and reliability [2]. Scaling improves the transistor density on chip. It improves the frequency of operation and performance [3]. Today portable devices have main concern in VLSI. It is due to limited power supply through battery. So circuit should consume less power [4].In current scenario smart portable electronics with high resolution CMOS image sensors become very popular. To achieve high resolution, low cost CMOS image sensor in a thin and compact smart electronic devices pixel dimension of the CIS are getting smaller [5].

The architecture of CMOS imager has two important parts one is array of pixels and other is column level analog to digital converter for each column of pixel's array. To achieve a high resolution CIS number of pixels should increase but surface area remain same. It means that there is decrease in pixel width. So, column level ADC should be small in size. In CIS a scene is focused by a lens through an array of pixels on to image sensor which converts light into electrical signal [6]. Each pixel consists of one photodiode to sense the light and some transistor. These transistors can act as reset, shutter and source follower [7]. Pixel converts light into electrical signal. This electrical output goes to analog to digital converter then a significant amount of digital processing image enhancement and compression occurs [8].

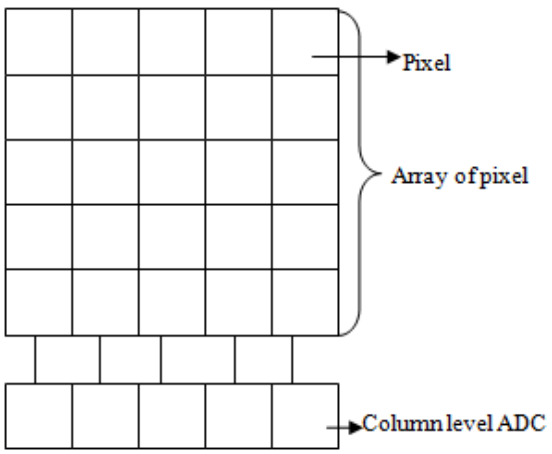

Fig.1- Pixel array with column level ADC

The architecture of pixel may change according to application. Depending upon the application of device the circuit will change [9].The connection of column level ADC with pixel array is depicted in fig.1.As shown in figure that for every column of array one ADC is required. So, this type of ADC is called as column level ADC. Hence the size of ADC should be minimized to match the column width of pixel array. Small surface area also helpful in reduce power consumption. It means to design CMOS image sensor surface area of column level ADC is very important.

Cost of chip is also a one important factor. CMOS implementation offer high integration capability with low cost [10]. CMOS is a type of integrated circuit chip manufacturing process. It is used in scientific, industrial and many applications [11]. Designing the ADC using small devices takes scaling merits. Small area in turn contributes to reduce the power consumption [12]. The demand of such type of ADC has increased. This is because they employ a large number of parallel ADC channels, which provide the high speed readout of large pixel array [13].

II. Proposed Dual slope ADC

Dual slope ADC is an integrating type ADC. Column level integrating type ADC is widely used for the commercial high resolution CMOS image sensor product [14]. It has less hardware complexity and suitable for design high resolution ADC. It is more accurate. Dual slope ADC consists of integrator, comparator, counter and control logic. Schematic of dual slope ADC is shown in fig. 2.

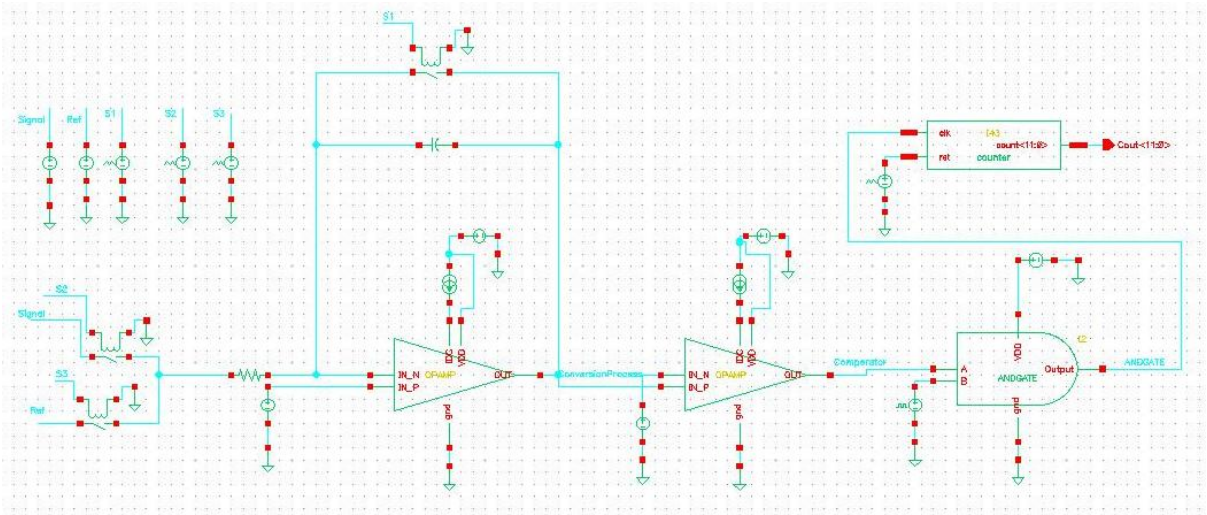

Fig. 2- Schematic of Dual Slope ADC

The conversion process of dual slope ADC is shown in fig.3. It is observed that the slope of the V_{int} is proportional to the amplitude of V_{in}^{*}.

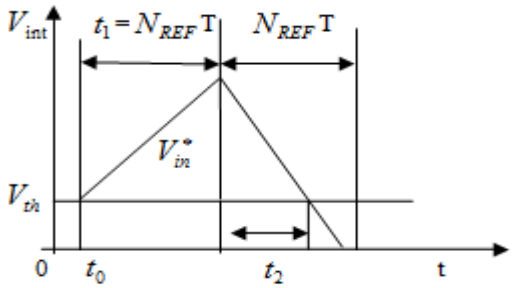

Fig. 3- Waveform for Dual slope ADC

Initially when switch1 is in operation the output of the integrator will stable at it's reference voltage. At time t_0 switch2 integrator connects to signal voltage V_{in}^{*}. This time capacitor starts charging and counter's counts up to particular time t_1. The voltage $V_{in}(t_1)$ at t = t_1.

$$V_{\text{int}}(t_1) = \text{K}\int_0^{N_{REF}T} V_{in}^* dt + V_{\text{int}}(0) = \text{K}\,N_{REF}\,\text{T}\,V_{in}^* + V_{th} \quad (1)$$

Where $t_1 = N_{REF}\,\text{T}$ and T = clock pulse.

At time t_1 Switch3 is connected to reference voltage. Capacitor starts discharging. Count of counter starts. When the output of the integrator reaches to the threshold voltage V_{th} of comparator counter will be stopped and binary count can be converted in to digital word N_{out}. t_2 is the time where the output of the integrator reaches to the V_{th} of comparator. The integrator voltage at $t_1 + t_2$ is given as

$$V_{\text{int}}(t_1 + t_2) = V_{\text{int}}(t_1) + \text{K}\int_{t_1}^{N_{out}T+t_1} (-V_{REF})dt = V_{th} \quad (2)$$

Where $t_2 = \text{T} + \text{t}_1$

Substituting Eq. 1 in Eq. 2

$$\text{K}\,N_{REF}\,\text{T}\,V_{in}^* + V_{th} - \text{K}\,V_{REF}\,N_{out}\,\text{T} = V_{th} \quad (3)$$

solving Eq. 3 for N_{out}

$$N_{out} = N_{REF} - \frac{V_{in}^*}{V_{REF}} \quad (4)$$

It has observed that N_{out} will be some fraction of N_{REF}, where fraction corresponds to the ratio of V_{in}^* to V_{REF} [15].

III. Two- Stage Operational Amplifier

Differential amplifier can be considered as the operational amplifier. Load resistance of the differential amplifier replace with current mirror. This is a single stage opamp. The two stage opamp is the combination of differential amplifier and common source amplifier. The geometry of the transistors in the opamp is very important to achieve a high gain. Saturation current equation is very significant to calculate the width and length of transistors. In two stage opamp first stage provides high gain and second stage provides large swings [16].

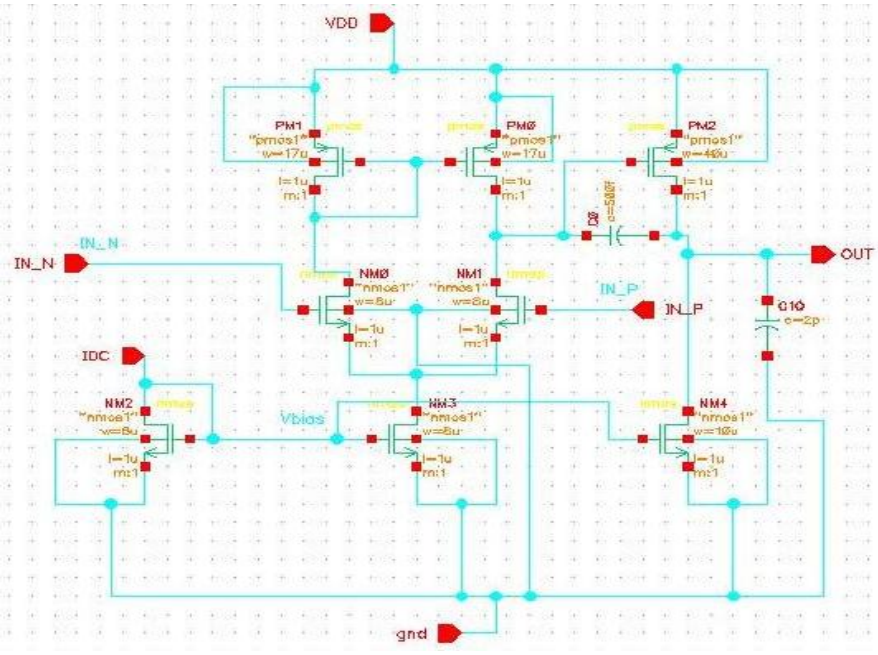

Fig. 4- Schematic of Two stage Opamp

The schematic of two stage opamp is depicted in fig. 4. The supply voltage of two stage opamp is 3.3volt.

IV. Result and discussions

Opamp is one crucial block for integrating type ADC. In proposed dual slope ADC two stage opamp is design. Gain of two stage ADC is observed from the simulation which is 78 dB. It can see in fig. 5. It shows the AC analysis of two stage opamp.

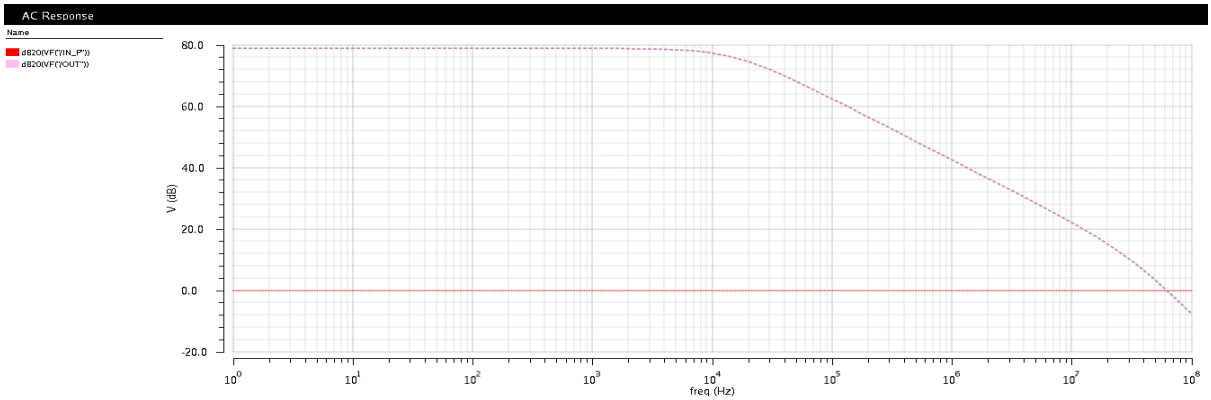

Fig.5- AC analysis gain of two stage Opamp

DC analysis of two stage opamp is depicted in the fig. 6. DC voltage varies from 0volt to 3.3volt. Same opamp has been used as comparator.

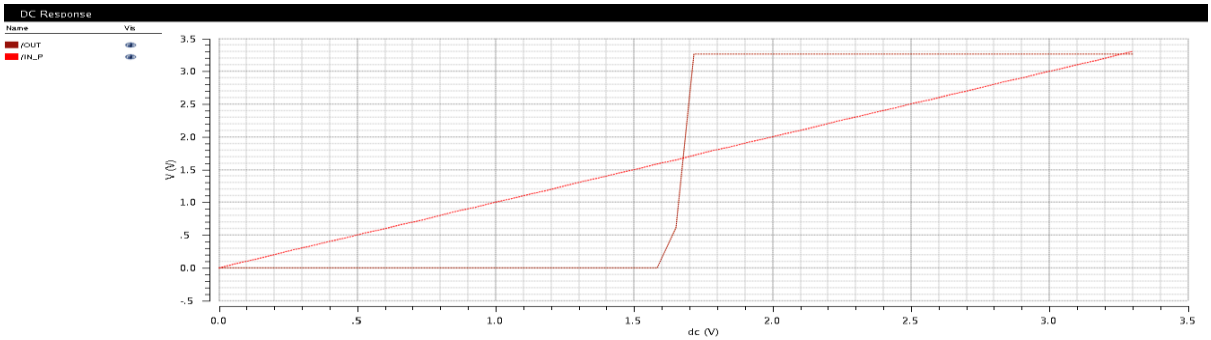

Fig.6- DC analysis of two stage Opamp

It provides the value of input voltage where gain of opamp is high. Simulation for conversion time is depicted in fig. 7. This figure shows the conversion time of dual slope ADC and comparator output.

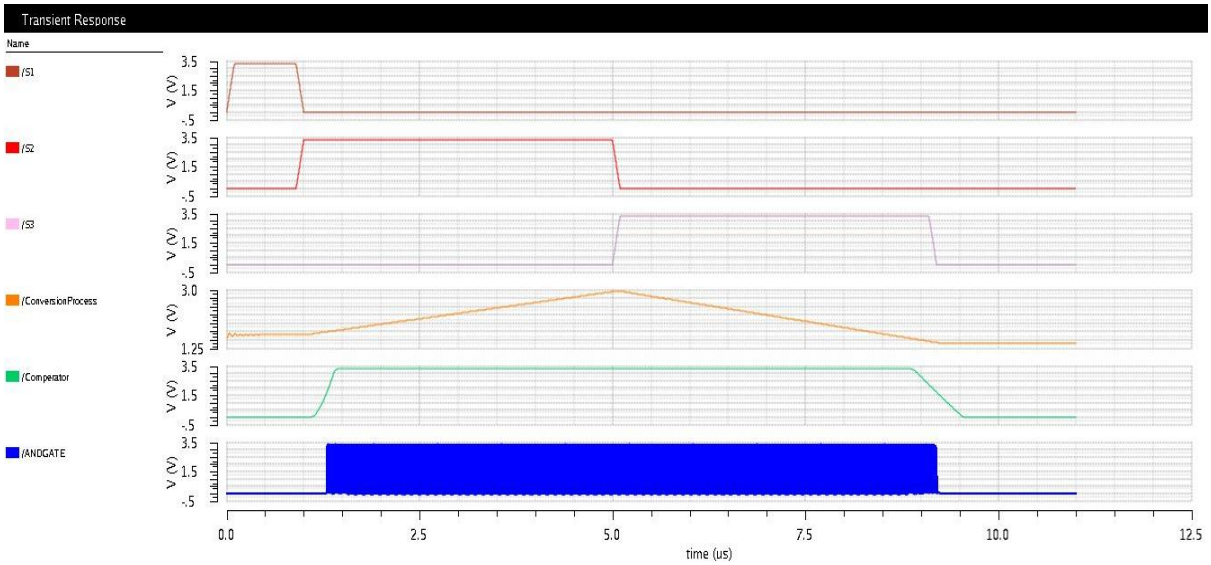

Fig.7- Simulation for conversion time.

Simulation of dual slope ADC shows the conversion time is 9.2µs. Three switches timings are also shown in this fig. 7. These results obtained for the 12-bit dual slope ADC. Design summary of dual slope ADC is presented in Table 1.

Table 1. Design summary of Dual slope ADC

Parameters	Proposed Work
Technology	0.18 µm
Type of ADC	Dual slope
Resolution	12 bit
Conversion time	9.2 µs
Opamp used	Two Stage
Gain of Opamp	78 dB

The comparison of proposed dual slope ADC with other ADC is shown in table 2.

Table2. Comparison of parameters with other ADC

Parameters	Proposed Work	[14]
Technology	0.18 µm	0.18µm
Type of ADC	Dual slope	SS/SAR
Resolution	12 bit	11 bit
Conversion time	9.2 µs	12 µs

It shows reduction of 23.33% in conversion time as comparison with [14]. Resolution of dual slope ADC is also increased. Graphical representation of comparison is shown in fig.8. First two bars shows the comparison between resolution and next two shows the comparison in conversion time.

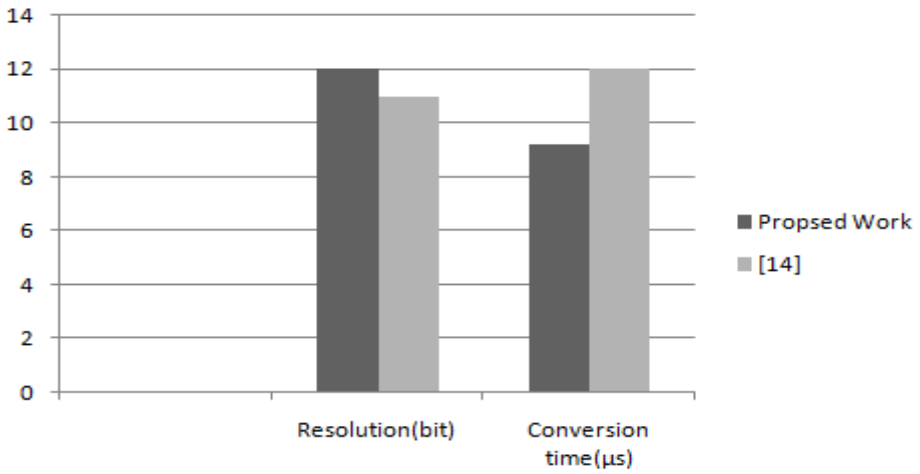

Fig.8 Graphical comparison of other ADC

V. Conclusion

In this paper a 12- bit dual slope ADC is designed for CMOS imager which is an integrating type ADC. This is well suited for column level ADC because it is more linear and accurate than any other ADC. Opamp plays a main role in this type of ADC. Two stage opamp is design which provides gain of 78 dB. The conversion time of this dual slope ADC is 9.2 µs. It can be observed from simulated results that proposed dual slope ADC results in 23.33% reduction in conversion time when there is increase of 1 bit resolution over the work previously carried out as depicted in table2. Simulation of this column level ADC is obtained using 180nm technology.

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