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An Energy-Efficient sense amplifier using 180nm for SRAM

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Abstract : *Static Random Access memories are scaled down in order to improve overall density of the chip and hence to lower the power consumption of the system. So increased density but less power consumption optimises the overall system. For SRAM sense amplifiers which are important peripheral circuitry also need to be designed to optimize overall system. Scaling and process variations may change the sense amplifier characteristics which further results to the wrong decision. It has been observed that the threshold variation gives rise to the power and delay variations. A proposed model has been derived for simplified latch to model the effect of threshold variations. The output is observed under the various conditions of V_{DD} and temperature to obtain the optimum value of sense delay, power consumption using 180nm technology mode. In this paper the power of the sense amplifier circuit is reduced upto 30µw with reduced delay.*

Keywords: *offset cancellation, static random access memory (SRAM), threshold voltage mismatch, Voltage sense amplifier.*

I. Introduction

SRAM's (Static Random Access Memories) consume most of the space in the system on chips (SOCs). It takes at least one third of the total area of the chip and thus has large impact on chip yield. SRAM read access yield (Y_{read}) is defined as the probability of correct read sensing operation [1, 2]. With increase in random variations (due to random dopand fluctuations, line edge roughness and other sources) SRAMs become very sensitive to dynamic operating conditions like temperature, aging, changing application load and process variations especially when the supply voltage is reduced. Random variations causes yield loss due to several mechanisms such as read stability, write ability, retention and read sense margin, however read sense margin is the mechanism that typically limits SRAM speed [2, 3]. The process variations may also results in the threshold mismatch which affects the offset voltage of the circuit. So offset compensation techniques are required to produce the accurate output [4]. Factors that determine the suitability of a SA includes sensing delay, power/energy consumption, die area, and resolution [1]. With scaling down of CMOS technology leakage is another important issue. To reduce leakage power many techniques like dual-Vth, multi-Vth, transistor stacking and body biasing are used [5].

Sense amplifiers are the important peripheral circuits of the SRAM which are used for reading the memory at a fast rate. Various types of sense amplifiers are used according to the requirements. Voltage sense amplifiers are used because of the property of low power dissipation and faster speed. The use of current sense amplifiers [6] has a number of benefits over voltage sensing amplifiers. Sense amplifier which uses PMOS transistor for its operation causes the power to be reduced to a large extent and it works in different V_{DD} conditions [7]. Sense amplifiers are also classified in local sense and global sensing for the fast operation and low power consumption. Global stage is activated only if the local stage has completed its sensing and amplification [8]. The slower transition of SAEN signal is proposed to result in high speed as well as low power consumption in SRAM application. In this paper a model of sense amplifier is proposed whose operation is examined under the various conditions of temperature and substrate potential.

The sections in this paper demonstrate the following. In the section II methodology used for low power operation is introduced. Section III looks into the design of the proposed circuit. In sectionIV the simulation results are introduced and finally V concludes the paper.

II. Sense Amplifiers

Current sense amplifier and voltage sense amplifiers are used in the SRAM for the read operation. Latch type voltage sense amplifiers find a wide use because of various advantages like low power consumption and less delay. Simulations are performed using 180nm technology with V_{DD} taken at 1.8V. During simulation V_{bl} was assumed to be greater than V_{blb} by ∇V_{bl}. For the high resolution of sense amplifier circuits the input offset voltage of the sense amplifier is reduced. Below this voltage the sense amplifier does not sense the input and does not produce any output so this region is also called deadzone. The input offset voltage may vary due to

the threshold mismatches of the input and sensing transistors [9]. According to Pelgrom's research [10], the standard deviation of Vth variation (σ_{VT}) is expressed as

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}} \quad (1)$$

Where

$$A_{VT} = \frac{\sqrt[4]{4q^3\epsilon_{si}\phi N}}{2}.T_{OX}/\epsilon_{OX} \quad (2)$$

where A_{VT} is a constant that depends on the process technology used [9],Φ is the Fermi potential, T_{OX} is the thickness of the gate oxide, N is the doping concentration of the substrate, and$\epsilon_{Si}$and ϵ_{OX} are the permittivity of silicon and the gate oxide, respectively. In this paper low power and low delay is achieved by applying the substrate bias voltage from a control circuitry. The voltage applied at the substrate terminal may change the behavior of transistor. Fast operation may be achieved using the multi-threshold devices in the circuit. The threshold condition of the MOSFET depends on the following factors

$$Vth = Vtho + \gamma\left(\sqrt{|2\theta_F + V_{sb}|} - \sqrt{2\theta_F}\right) \quad (3)$$

Where

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}} \quad (4)$$

III. Proposed Low Power Sense Amplifier

A Latch sense amplifier is used in most of the memories for sensing and amplification of the data. It provides fast operation of read and consumes low power so used in most of the memory designs. Here the modified latch type sense amplifier is shown in Fig. 1.

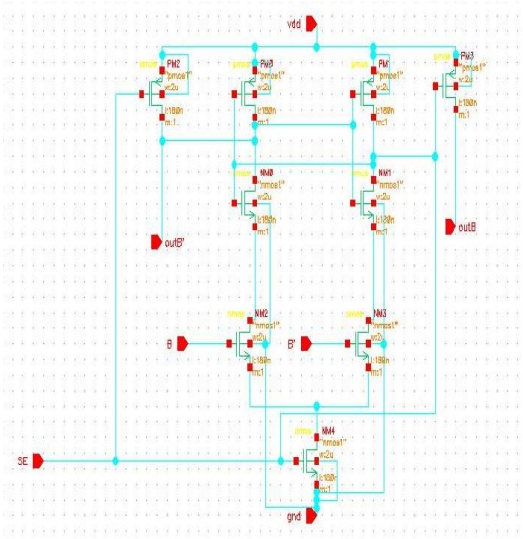

fig1:- Modified latch type sense amplifier

This sense amplifier circuit consists of 5 NMOS and 4 PMOS transistors. This circuit is in sensing mode when input to SEN is high. The circuit performance is tested for the precharge mode and read mode. The circuit is precharged by giving low voltage at NM4 and a high voltage at b and b'. Due to this, MP2, MP3 transistors performs in linear region and all the remaining transistors are in cutoff region. So the output will follow the input voltage (1.8V). Now for the read mode SEN and b' is kept at high potential and b is kept at low. Under this condition, transistors MN1, MP0, 1 and 4 are in cutoff region and MN0, 2, 3, 4 and MP2, 3 are in linear region. Hence the out will follow the input whereas the out' is low.

In proposed sense amplifier circuit a range of input voltage is applied to the substrate of the pmos and nmos transistors. With the change in the substrate voltage results in changed level of threshold value of the mos transistors and hence the delay and power consumption of the circuit changes. The schematic of proposed amplifier is shown in Fig. 2.

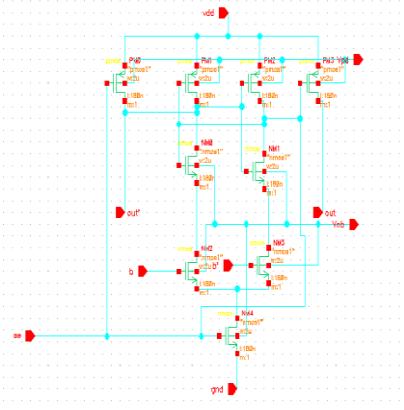

fig 2:-Proposed latch type sense amplifier

IV. Simulations Result

The circuit is simulated under the different values of substrate voltage in order to reduce the threshold voltage of the transistors. For the low power consumption variable threshold cmos are used, but increase in lower threshold voltage leads to increased leakage hence more standby consumption. So appropriate value of threshold voltage is determined. The transistors with the low threshold values switch faster than the high value threshold transistors. Here Vdd 1.8v is applied to the circuit. On simulating the circuit at the temperature of 27^0 changes in power consumed are being checked. The circuit is simulated using the 100Mhz frequency. Fig. 3 shows the input conditions of the circuit.

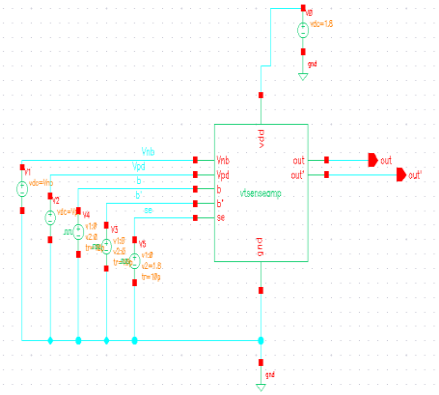

fig 3:-Biasing of proposed sense amplifier

Fig. 4 shows the simulation results of the proposed circuit. It is observer that when sense enable signal is activated the circuit senses the input and amplifies it. But when it is not activated it passes the previous stored value to the output. The biasing voltages to the circuit components and w/l ratio determine the sensing speed and consumed power of the circuit.

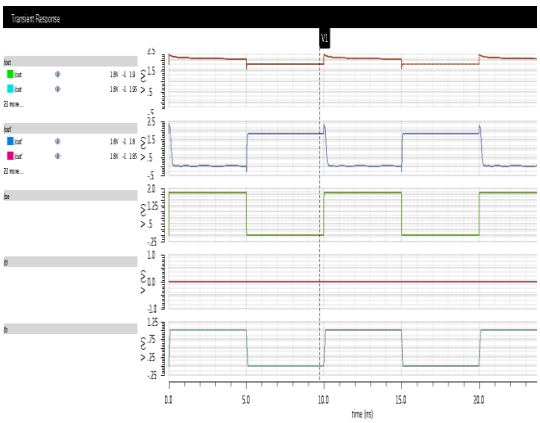

fig 4:- Input and output wave shapes of the proposed sense amplifier

A performance comparison of proposed sense amplifier is shown in Table 1 and it is observed that the power consumed and hence the delay produced is very low as compared the previous designs. Graph showing the power consumed at various bit voltage difference is also shown in Fig. 5

Table1:- Performance comparision of the prosposed sense amplifier

Design	Area	Design Node	Power	Delay
Proposed	9T	0.18µm	30.637µw	.108ns
[4]	13T	0.18µm	21.2µw	.70ns
[10]	14T	0.18µm	84µw	1.10ns

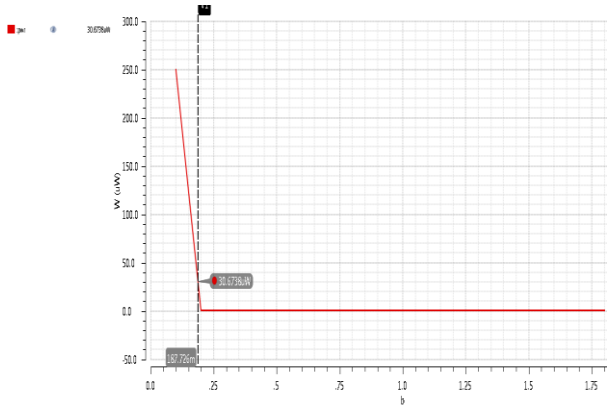

fig 5:- Measured power w.r.t various bitline voltages

V. Conclusion

A SRAM latch type sense amplifier has been proposed with variable threshold CMOS. It may be conclude that on increasing value the w of cmos transistor the offset voltage may be improved but it may results in increased area. Simulations at 180nm CMOS technology at 100MHz frequency are done and it has been observed that the proposed sense amplifier gives the correct read decision at very low voltage difference and hence produces the less delay of .108ns, which leads to the fast operation and low power consumption of about 30µw, and improved yield.

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