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Design of Voltage Controlled Oscillator for Clock Synchronization in Phased Locked Loop

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Abstract: *A voltage-controlled oscillator is an oscillator designed using cascaded inverters of order of odd number to generate signal of certain frequency. This depends on the control voltage applied as input to the VCO. VCO can be designed as part of Phased Locked Loop where a Phase detector detects the difference between phase and frequency of reference frequency with a required frequency. This difference is applied as control voltage to VCO. The output frequency is divided by certain frequency to generate a low frequency to match with that of Reference frequency. Oscillators are used in Phased Locked Loop receivers. Phase noise is the most important parameter to be controlled. For high performance and Low power design, different types of inverters are analyzed and the corresponding VCO is designed.*

Keywords: *VCO, PLL, Ring Oscillator, clock synchronization etc.,*

I. Introduction

The drastic development in VLSI Technology and scaling of technology parameters have led to integration of millions of transistors in the chip. The devices built of these minute components operate at very high frequencies thus need stable clock frequencies with good transitions. But the delay in transferring the signals create Clock skew and Jitter. The clock is to be routed to various subsystems with synchronization to reference. Also having dedicated quartz crystals for high frequencies is also not possible. But Stable frequencies are generated by these crystals. This A VCO can be used to generate a signal of required frequency and it is frequency or phase locked to reference clock with the help of Phase Locked Loop.

A Phased Locked Loop is a feed back system whose output frequency or phase is compared to an input signal. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison since the output is "fed back" toward the input forming a loop. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency

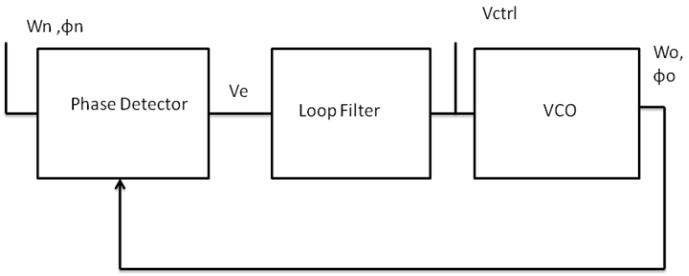

Fig.1 Phase Locked Loop

The quality of a clock signal is determined by its phase noise and jitter. Maintaining the phase noise and jitter in as low as possible for these high performance applications is a necessity. phase-locked loop (PLL) is used to produce low jitter clocks.

II. Ring Oscillator (VCO)

A ring oscillator is a device composed of an odd number of Inverter output Varies between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.

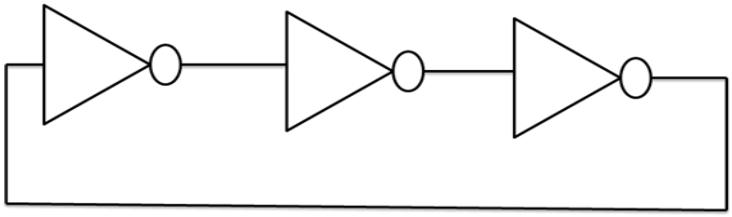

Fig.2 Ring Oscillator

If 't' represents the time-delay for a single Inverter and 'n' represents the number of Inverters in the Inverter chain, then the frequency of oscillation is given by

$$f=1/2*t*n$$

Here n

1. n-stage ring oscillator will have a period
2. n should be odd
3. The delay of each inverter stage depends on V_{CTRL}

$$Tperiod = 2*N* t\ inv$$

2.1current Starved Inverter Stage

1. The delay of each inverter stage depends on V_{CTRL}
2. Very wide tuning range
3. Terrible supply sensitivity

$$t_{inv} = V_{DD} /(V_{CTRL}-|V_T|)$$

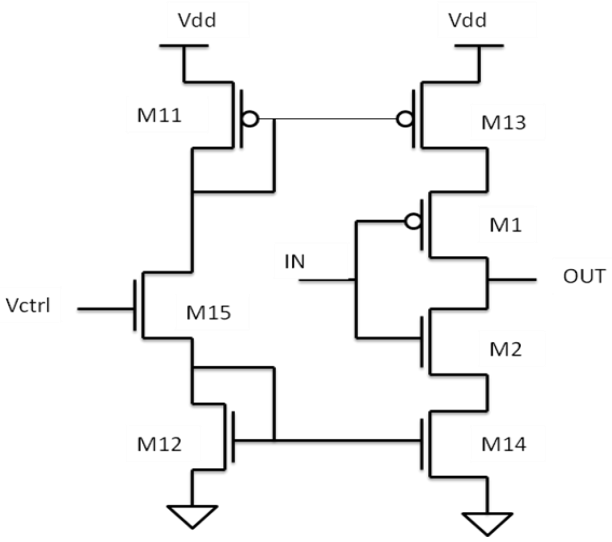

Fig.3 Current Starved Inverter

In the Current Starved Inverter the control voltage applied is Vctrl whereas input voltage is applied to an inverter.

2.2 Differential Inverter Stage

1. Diode connected PMOS offers a resistive load ,1/gm,p
2. The resistance changes with the bias current
3. Very sensitive to supply noise

$$t_{inv} = C_L/gm,p$$

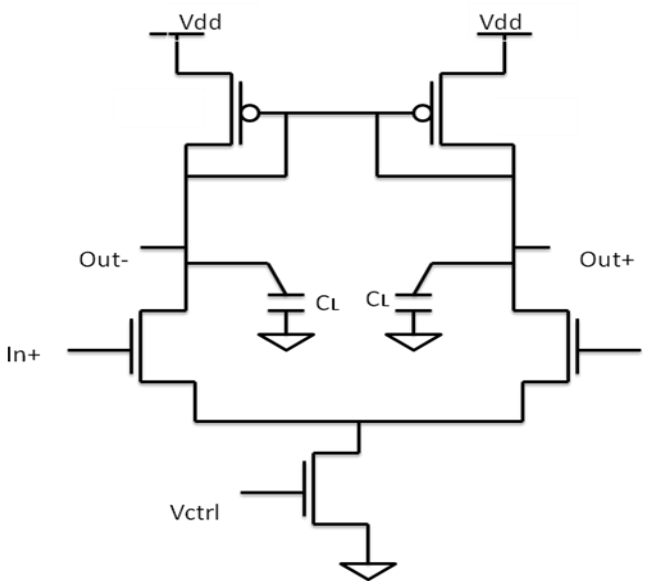

Fig.4 Differential Inverter Stage with V_{Ctrl}

2.3 Differential Inverter Stage With Vb

1. Triode pmos devices act as variable resistances -wide tuning range
2. Differential nature reduces supply noise only slightly
3. Bias current has to be adjusted to maintain swing- A Swing control loop may be used.

$$t_{inv} = C_L/(V_{DD}-V_{CTRL}-|V_T|)$$

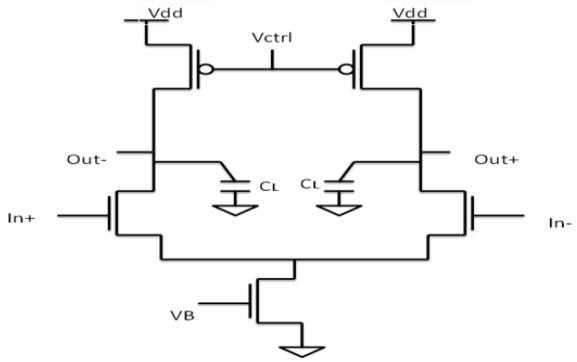

Fig.5 Differential Inverter with Vb

2.4 Full Swing Differential Inverter Stage

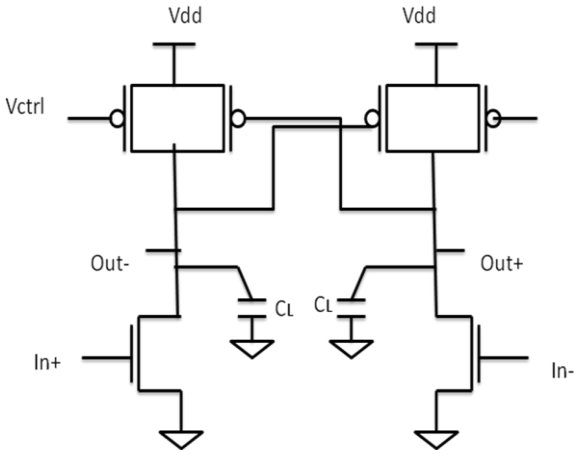

Fig.6 Full Swing Differential Inverter Stage

2.5 Full Differential Inverter Stage With Vb

1. CMOS Transmission gate act as variable resistances -wide tuning range
2. Differential nature reduces supply noise only slightly .Bias current has to be adjusted to maintain swing- A Swing control loop may be used.

$$t_{inv} = C_L/(V_{DD}-V_{CTRL}-|V_T|)$$

A Ring Oscillator is implemented with Current starved Inverter Stage, Differential Inverter Stage ,Differential Inverter with bias, Full Swing Inverter Stage, Full Swing Inverter Stage with V_B .

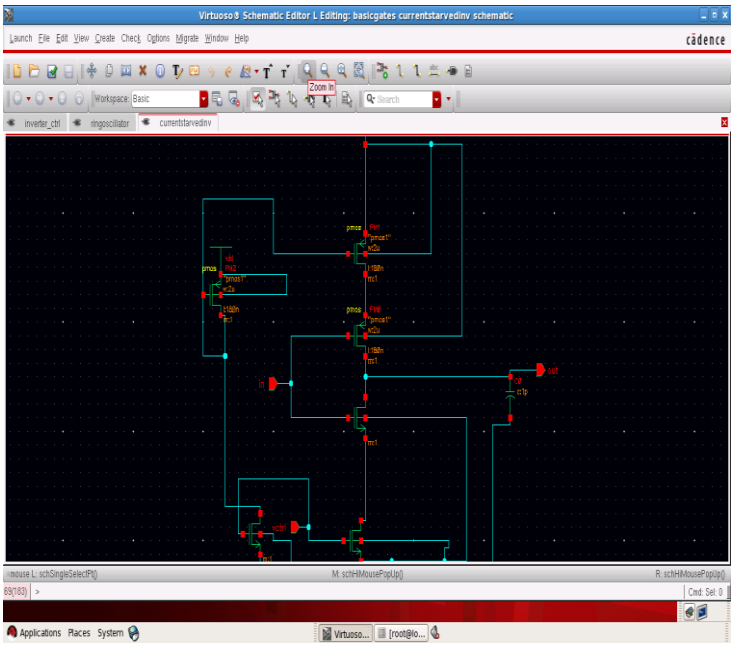

Fig.7 Schematic of Inverter with ctrl & Ring Oscillator

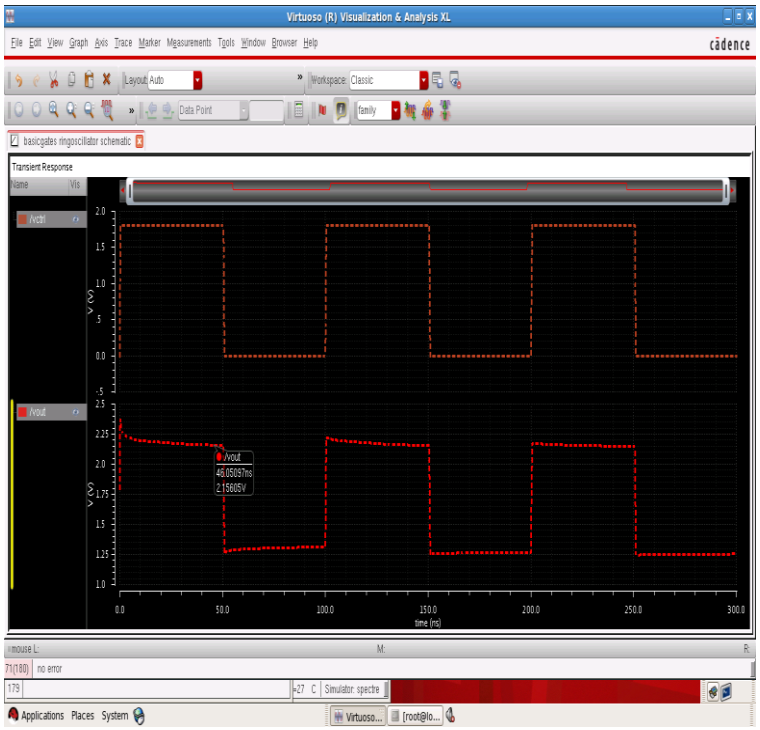

Fig.8 Simulation Results of Ring Oscillator using Inverter with ctrl

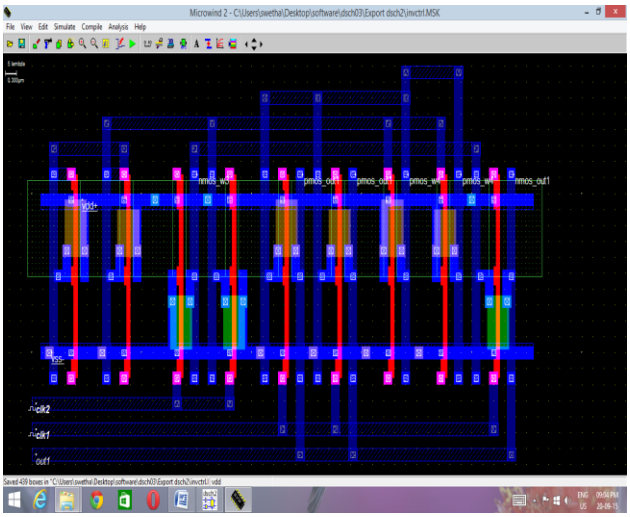

Fig.9 Layout of Inverter with Ctrl

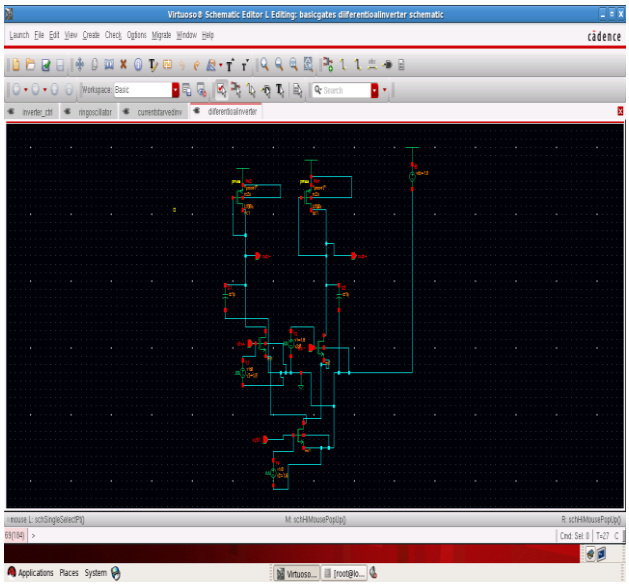

Fig.10.Schematic of Differential Inverter with V_{ctrl} & Ring Oscillator

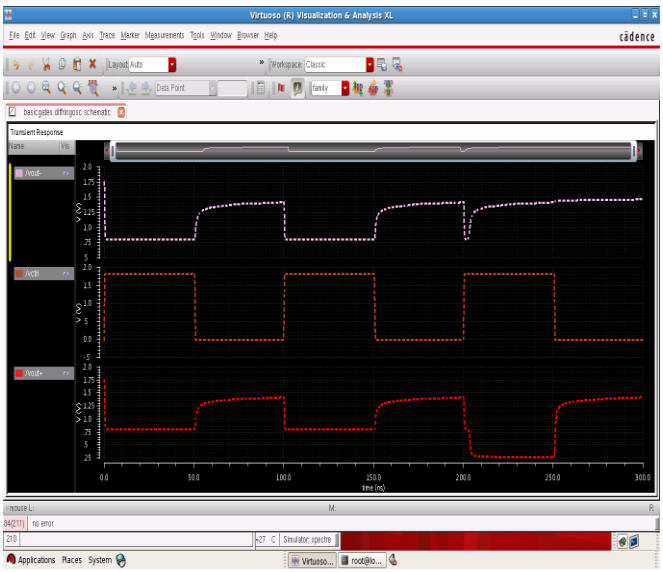

Fig.11 Simulation Results of Ring Oscillator using Differential Inverter with Ctrl

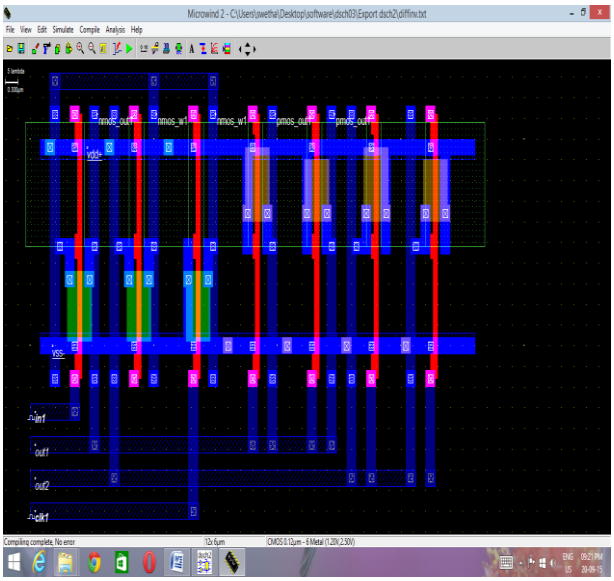

Fig.12 Layout of Differential inverter with Ctrl

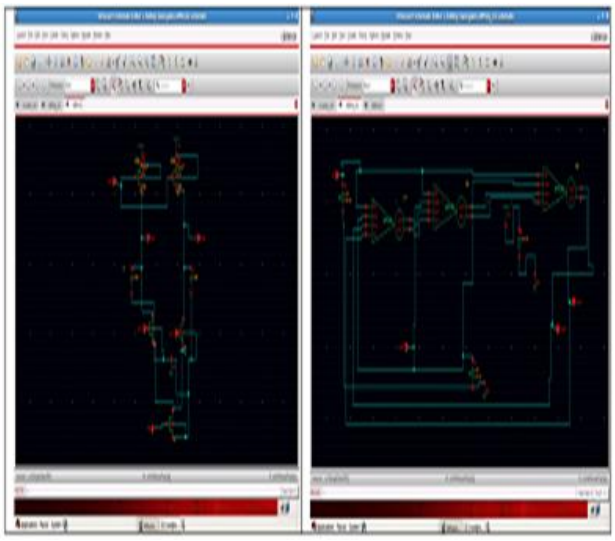

Fig.13 Schematic of Differential Inverter with Ctrl & V_B & Ring Oscillator

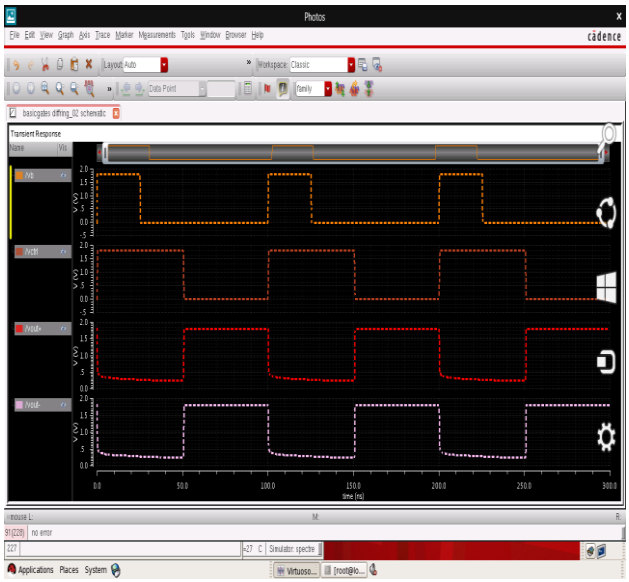

Fig.14 Simulation Results of Ring Oscillator using Differential Inverter with Ctrl & V_B

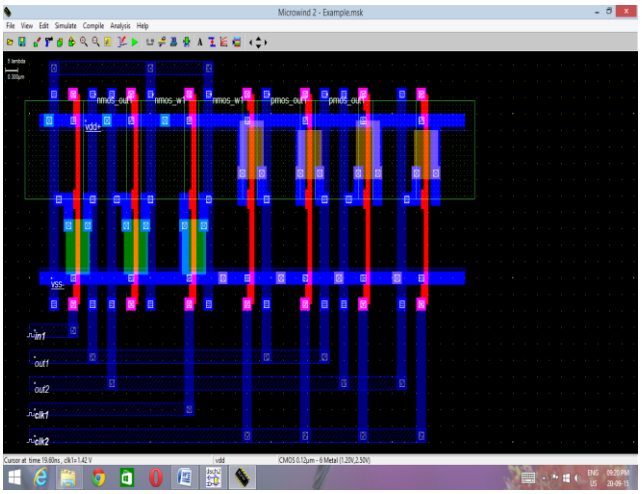

Fig.15 Layout of Differential Inverter stage with Ctrl & V_B

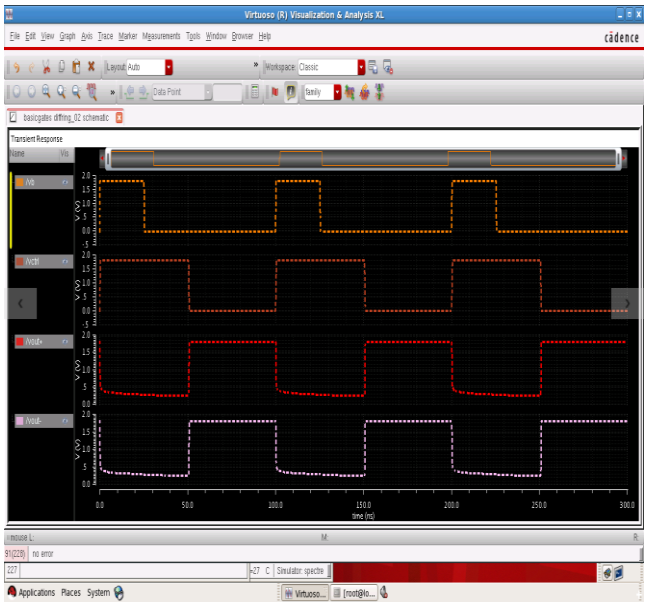

Fig.16 Simulation Results of Full Swing Differential Inverter Stage

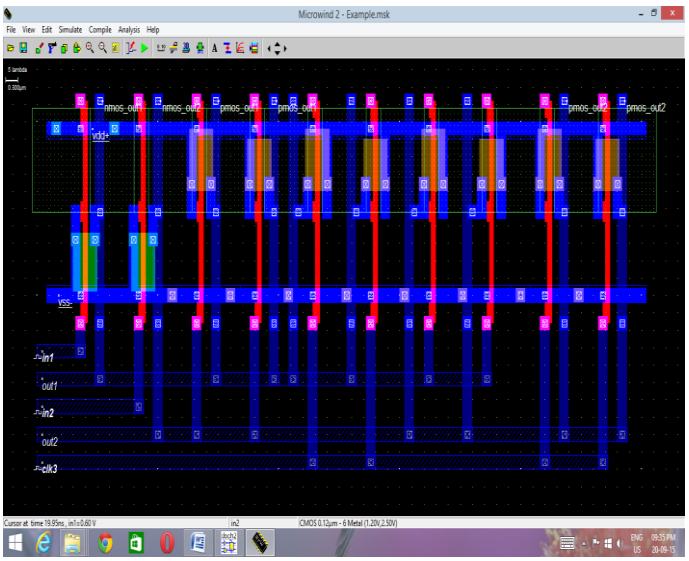

Fig.17 Layout of Full Swing Differential Inverter stage

III. Conclusion

In this paper, Voltage Controlled Oscillator is designed as a Ring Oscillator in which variant types of Inverters are analyzed. the main aim is to adopt a Low power Clock generation using differential stages or a reduced swing clock signal . Therefore, the power dissipation of the VCO, clock network can only be reduced by

a) reducing the total load capacitance.
b) reducing Vdd
c) reducing Vs without reducing Vdd, which corresponds to a linear reduction in the power dissipation.

To reduce Power dissipation of Voltage Controlled Oscillator , design of inverter with multiple voltages and multi Vth is used.

S.No.	Different types of Inverter	Power Dissipation
1	Inverter with Ctrl	0.413 mw
2	Differential Inverter with Ctrl	0.371 mw
3	Differential Inverter with Ctrl and Vb	0.269 mw
4	Full Swing Differential Inverter stage	0.983mw
5	Differential inverter with multiple voltages/Reduced Swing Logic	0.213mw
6	Differential inverter with multi Vth	0.202mw

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