IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 3, Ver. II (May. -Jun. 2016), PP 107-110
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design & Implementation of Low Power 4-Bit Full Adder Using XNOR Logic by Gate Diffusion Input (GDI) Technique with Header and Footer Sleep Transistors

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Abstract: *The basis of numerous operations such as counting, multiplication, filtering are done with the full adder. Adders are heart of computational circuits and many compound arithmetic circuits on the basis of addition. The vast uses of this operation in arithmetic functions attract a lot of researcher's attention for mobile applications. Nowadays, various adder implementations are available in order to realize the speed or density requirements in which adder's optimization is paramount factor. This paper describes GDI based XNOR logic 4-bit full adder. It uses added logic in the design which results area overhead but since our concern is power so we have to compromise upon the area. This 4-Bit Full adder will be analysed with incursion of both header and footer switches. The proposed technique uses extra transistor logic (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other. The proposed circuit offers less average power and time delay. Simulations have been carried out by Tanner EDA tool.*

Keywords: *Full Adder, GDI (Gate Diffusion Input), Sleep Transistor*

I. Introduction

As the technology increasing, battery backup is a big problem. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. For portable electronic devices this equates to maximizing battery life. This low leakage adder is designed for mobile phones. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. The Boolean equations are repositioned by typical level optimization to attain smaller circuit. On the other hand transistor size and circuit topology is manipulated by Circuit Optimization to optimize the speed. These studies approaches different types of application oriented CMOS design [1].

Gate Diffusion Technique uses less number of transistors as compare to any conventional technique of implementing logic circuits. This technique designed circuits with low complexity and reducing power consumption, propagation delay and area of digital circuits [2].

In this paper we design the 4-bit full adder having less average power consumption and reduced the ground bounce noise by using the power gating technique. For reduction of noise sleep transistors are used. This is stated based on the fact that a state is less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path. The power gating uses both Header as well as Footer as per the circuit use [3].

The paper is organized as follows. GDI based XNOR design describes in section II. Section III shows the proposed circuit. Section IV describes the result of GDI based 4 bit full adder. Section V describes conclusion and future scope.

II. Gdi Based Xnor Design

In present scenario, portable devices have important role in our life style. These devices demanded compact size, high speed and low power dissipation. ALU uses the full adder as a component that i.e. the most important part of processer. In low power design digital circuits the popular design is Pass Transistor Logic (PTL). PTL has some advantages over standard CMOS design that are high speed, less number of transistors, low power dissipation and having less are i.e. low interconnection effect [2].

Gate Diffusion Input (GDI) approach allows execution of an extensive range of complex logic function using only two transistors. GDI technique implementation is suitable for logic implementation at low power level, less number of transistors and faster than existing previous techniques [4].

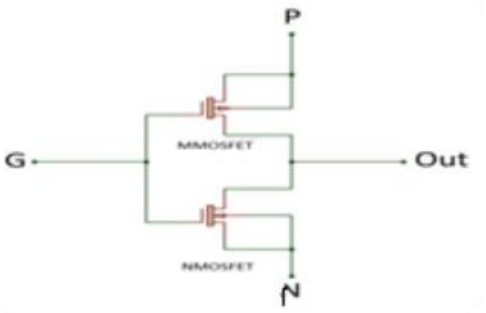

Fig. 1 GDI Basic Cell [2]

The GDI based logic implementation depends on its single cell. GDI cell made up of two transistors (N-MOS and P-MOS) or one of the standard CMOS inverter, but there are some differences.

Table No. 1 Various Logic Functions of GDI Cell for Different Input Configurations [2]

N	P	G	Out	Function
'0'	B	A	$\bar{A}$B	F1
B	'1'	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

The GDI cell contains three inputs: G (common gate input of N-MOS and P-MOS), P (input to the source/drain of P-MOS), and N (input to the source/drain of N-MOS). Bulks of both N-MOS and P-MOS are connected to N or P, so it can be biased at contrast with a CMOS inverter.

Basic component in the design of the communication circuits are arithmetic circuits such as adder and multiplier. Now days an irresistible curiosity has been seen in the designing of digital processing system and communication systems with low power at no performance tolerance. Conventional full adder combines transistor PMOS pull-up and transistor NMOS pull-down network to produce output. This complementary static CMOS design requires 28 transistors. Carry is generated by first 12 transistors and Sum by remaining transistors. Due to large consumption of area, this circuit is slow. In this circuit signal propagates through two inverting stages in the carry generation circuit. For designing a high speed adder, minimizing the carry-path delay is the major goal. Performance of the full adder cell can be increase by optimizing the adder equations. For designing of full adder XOR and XNOR are the key variables [5][6].

$$\text{Sum} = A \oplus B \oplus Cin \quad (1)$$

$$\text{Carry} = A.B + Cin(A \oplus B) \quad (2)$$

Equation 1shows the sum output of full adder and 2 shows the carry output of the adder.

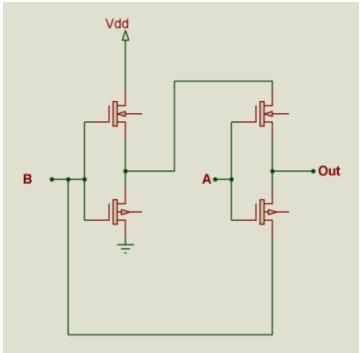

Fig. 2 GDI based XNOR gate

Fig.2 shows that implementation of the XNOR gate using GDI technique. In our proposed design we use gate diffusion input (GDI) based XNOR gate which uses only 4-transistors [7]. This GDI based design provides improvements in several areas such that static power dissipation, design intricacy, logic level swing and transistor count that make it more useful for designing in VLSI area [8].

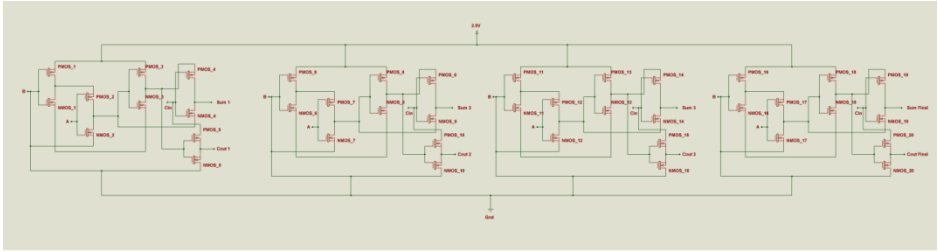

Fig. 3 4-Bit Full Adder using XNOR logic by GDI Technique

Fig. 3 shows 4 bit full adder using XNOR logic by GDI technique in which A, B and Cin are the inputs and Sum and Cout are the outputs.

III. Proposed Design

In our design, the transistor ratio of pMOS to nMOS has been kept 2:1. It is simulated in 250nm process. Proper sizing is very important for adder modification using power gating technique. Fig.4 shows leakage power reduction technique by insertion of a sleep transistor between actual ground rail and virtual ground and actual power supply and virtual power supply. The average power dissipation is measured by making both the sleep transistors ON and then giving input to the circuit.

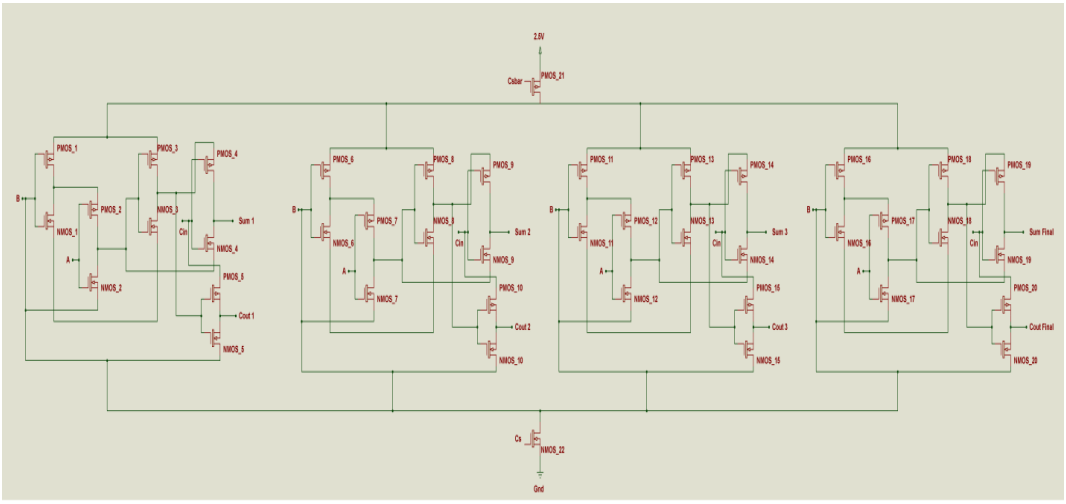

Fig. 4 4 bit XNOR based Full Adder using GDI technique with Header and Footer transistor (Proposed Design)

The ground bounce depends on the gated circuits, pole/zero points and inherent distinctiveness i.e. the dump coefficients with the charge/discharge current rate. When the circuits are connected with header and footer transistors then ground bounce noise is being estimated.

IV. Result Analysis Of Proposed Work

Fig.5 shows the output waveform of the proposed work. Simulation is carried out on the Tanner EDA tool v13.0. Transient analysis of these full adders is done for a time period of 500nsec without giving delay in the output at standard mode from DC operating point.

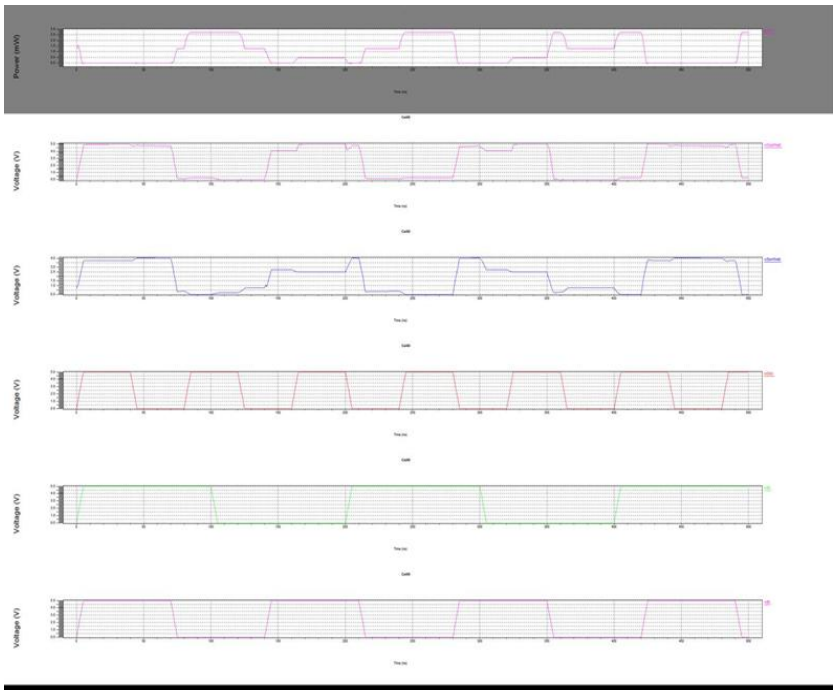

Fig. 5 Output Waveform of 4 bit XNOR based Full Adder using GDI technique with Header and Footer transistor (Proposed Design)

Table No.2 Measure Analysis of Proposed 4 bit Full Adder

Designs	Without Header and Footer Sleep Transistor	With Header Sleep Transistor	With Footer sleep Transistor	With Header and Footer Sleep Transistors
Average Power(mW)	1.927558	1.30426	4.404279	0.9651941
Transient Time Delay(nSec)	51.203	0.16299	51.796	0.23429

V. Conclusion

In this paper, average power consumption and delay of proposed GDI based 4 bit full adder have been analyzed on simulation tool "Tanner EDA". Output waveforms of 4 bit XNOR based Full Adder using GDI technique with Header and Footer transistors are drawn. Noise immunity has been carefully considered since significant threshold current of the low threshold voltage transition becomes more susceptible to noise. For low power application some designing level power management technique should be used.

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