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High Frequency Stability 1GHz Temperature Compensated Crystal Oscillator (TCXO)

Ranjini Rao N[1] , Roopashree[2]
[1,2]*Electronics and Communication Engineering Sahyadri College of Engineering and Management Mangalore, India*

Abstract: *Modern communication applications operating in Ultra High Frequency (UHF) band requires low phase noise, tight initial frequency calibration, good frequency stability over wide temperature range and low power consumption. All these parameters are achieved by the best sample of Temperature Compensated Crystal Oscillator (TCXO) only in 10-50MHz frequency band. It will be challenging in order to get these tighter specifications at VHF/UHF band. The small size TCXO can provide good combination of all these parameters when it is locked by the very high frequency reference signal. This allows to keep the good temperature stability and to achieve phase noise level of -112dBc/Hz @ 10kHz carrier frequency. TCXO can provide frequency stability of ±0.5ppm with good temperature compensation in -40^o C to 85^o C range.*
Keywords: *Phase noise, PLL, TCXO, VCXO, Microcontroller, UHF band*

I. Introduction

High accuracy synchronization and timing throughout a network are necessary to support fast bit rates, to preserve data and to maximize the use of available bandwidth so that networks can operate at their full capacity. The temperature compensated crystal oscillator is used to generate higher levels of temperature stability which are not possible with normal crystal oscillators. To reduce the frequency variations in output signal the correction voltage is generated using temperature sensor via a compensation network. Low phase noise, good frequency stability and low power consumption are essential for modern communication systems, radar application and digital signal processing (DSP). For example, in code division multiple access (CDMA) technique uses digital codes to represent the different phase states of frequency and time interval used by the mobile station or base station. If phase noise in system is excessive then it results in the possible loss of data and high bit error rate.

Synchronization of signal frequency in network must be extremely accurate in communication applications. Perfect frequency stability ±0.5ppm at all points is required for absolute synchronization. To diminish frequency discrepancies all timing devices inside the system is locked with a reference source. For example in global positioning system which uses CDMA technology with two timing devices are able to synchronize suitably to reference clock over complete lifetime and able to clutch frequency stable over a period. Poor synchronization results into loss of information.

Radios and other communication devices use quartz crystal resonators as frequency reference. When extraordinary precision was required by communication system then crystal is kept inside oven which held the crystal at persistent temperature. Therefore it is called as oven controlled crystal oscillator (OCXO) with appreciable accuracy. There are several limitations of OCXO are oven demands power to heat with internal temperature range 75°C to 95°C, relatively large warm-up time and long time to gain precise frequency and large package size. TCXO was developed to overcome the limitations of OCXO with good temperature and frequency stability.

TCXO when it is used with the high frequency reference allows to keep the good temperature stability and to achieve phase noise level of -112dBc/Hz @ 10 kHz carrier frequency and frequency stability of ±0.5ppm with good temperature compensation in -40^{o}C to 85^{o}C range. Achieving all these parameters at high frequency is complicated because of larger frequency dependency on crystal stability and circuit components. Proposed system employs a standard, low cost Phase Locked Loop (PLL) [1]-[5] technique, low frequency good compensated TCXO, low phase noise UHF frequency 250MHz VCXO, PLL with Low Pass Filter(LPF) and low cost, high performance Microcontroller.

II. Objective

1. Development of Microcontroller programming for loading data to the Phase Locked Loop (PLL).
2. Locking of 10MHz reference frequency with 250MHz RF using Phase Locked Loop.
3. Simulation in ADS software.

III. Existing System

CDMA mobile communication system timing and frequency synchronization are maintained to operate properly. 13MHz Temperature Compensated Crystal Oscillator (TCXO) with 1PPS phase locked with spreading code waveform with Pseudo Noise (PN) that modulates CDMA stationary base station carrier transmissions. Voltage Controlled Oscillator (VCO) to produce Local Oscillations (LO) used with PLL for GSM base station. GSM channel spacing 200 kHz to achieve this reference input is divided by 65 using reference divider of PLL. Input of loop filter is connected to output of Charge pump of PLL. The phase margin of loop filter is 45 degrees and reference input frequency is 200 kHz. Loop filter drives VCO input which is fed back to PLL synthesizer RF input.

IV. Proposed Methodology

Low noise 10MHz TCXO is locked with the low phase noise 250MHz VCXO by Phase Locked Loop. The PLL is controlled by the Microcontroller. The PLL register values are loaded by the microcontroller via simple three wire interface. PLL consist a precision charge pump, low noise Phase Frequency Detector (PFD), Programmable A and B counters, Programmable reference counter(R counter) and dual modulus prescalar P/P+1. At the PFD input the 14-bit R counter gives REFIN frequency. N divider is implemented using A (6-bit) counter, B (13-bit) counter and the dual-modulus prescaler (P/P + 1) that is N=BP+A. An external loop filter and voltage controlled crystal oscillator (VCXO) are used to implement the complete low noise PLL circuit.

The PFD produces an output that is proportional to the frequency and phase difference between the input signals which are taken by N counter and R counter. The loop filter is driven by the output of the charge pump. The loop filter is designed so that overall phase margin of the system must be 45 degrees. The output of the loop filter drives the input of the VCXO and output of VCXO is fed back to the PLL RF input. There are two main sources of noise in PLL [6] are Reference noise usually small since it frequently use a crystal oscillator and VCXO noise [7] is often high. The PLL is used to suppress most of the noise.

The N counter value has the largest impact on phase noise. The N counter value multiplies the phase noise hence N counter value must be small for better phase noise. Spur is noise energy focused at carrier discrete offset frequencies. Amount of the time PLL takes to change frequencies when N counter is changed is called as lock time.

The value of the comparison frequency is determined as maximum of common multiple of required output frequency *fout* and reference frequency of a phase detector. Calculation of the phase deviation can be evaluated using common formula [8] at a time interval τ:

$$\sigma^2_{\Delta\varphi}(\tau)=8\int_{f_\tau}^{2f_{out}} \frac{\beta_3}{f^3}[\sin(nf\tau)]^4\, df \qquad (1)$$

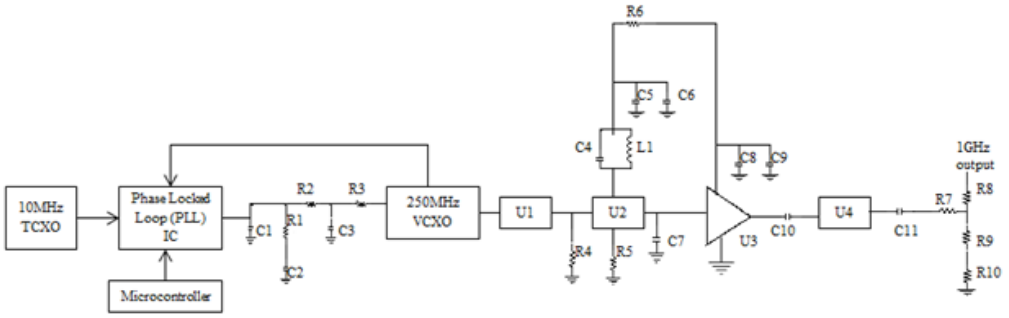

Fig. 1. 1GHz TCXO schematic. Where: U1- Band Pass Filter, U2- Narrow Band Pass Filter, U3- High Power Amplifier, U4- Band Pass Filter

In actual crystal element the cut of the crystal can help to minimize the temperature effects. Temperature drift can be minimized with AT cut crystal type around ambient temperature. Many of temperature effects can be minimized using temperature compensated crystal oscillator (TCXO).

Reference counter, N counter and Function counter values are loaded by programming the microcontroller using MPLAB ICD software. Function latch is used to program and select the prescalar value. The MPLAB ICD 3 In-Circuit Debugger that is controlled through a PC running MPLAB X IDE software. It has a USB cable to provide power to the debugger and to provide communications between debugger and a PC. Modular Cable is used to connect the MPLAB ICD 3 to a target board or header module. Three latches are 21 bit wide and it is divided into three sections like 5 higher bits, 8 middle bits and 8 lower bits are sent during normal operation of the PLL. Once 21 bits are sent to the PLL the load enable (LE) signal is high as shown in the Fig 2.

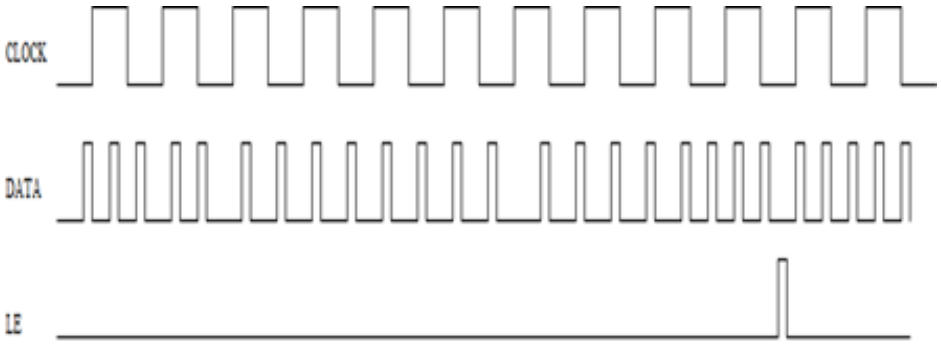

Fig. 2. Timing Diagram

V. Circuit Description

The phase frequency detector (PFD) is used to achieve wide pull-in-range in the PLL. The PFD takes inputs from R counter and N counter and the produces output that is proportional to the frequency and phase difference between input signals.

A 3rd order loop filter is used in PLL to convert the charge pump current to the control voltage for VCXO. Also it is used for filtering out noise which is coming to the control voltage from the input clock, otherwise which results in the unacceptable high spurious are present in PLL output spectrum. 3rd order filter is used to suppress the ripples in the control voltage. The transfer function for 3rd order filter loop filter is

$$\frac{V_{cntrl}}{I_{cp}} = \frac{1+s(R1C1)}{s(C1+C2)(1+sR1(C1//C2))(1+sR3C3)} \quad (2)$$

The second stage of the oscillator is a narrow band amplifier, which is also tuned on the required output frequency. To obtain a good spectral purity of VCXO output signal, it is necessary to pay attention to isolating of the frequency multiplication stage from the filtering and the output buffer stages to avoid an excessive amplification in device circuit as shown in Fig 1.

VI. Results

The programming is done the MPLAB X ICD v3.05 to load the data from the microcontroller to the PLL using modular cable. Microcontroller is connected to PC using high speed USB cable.

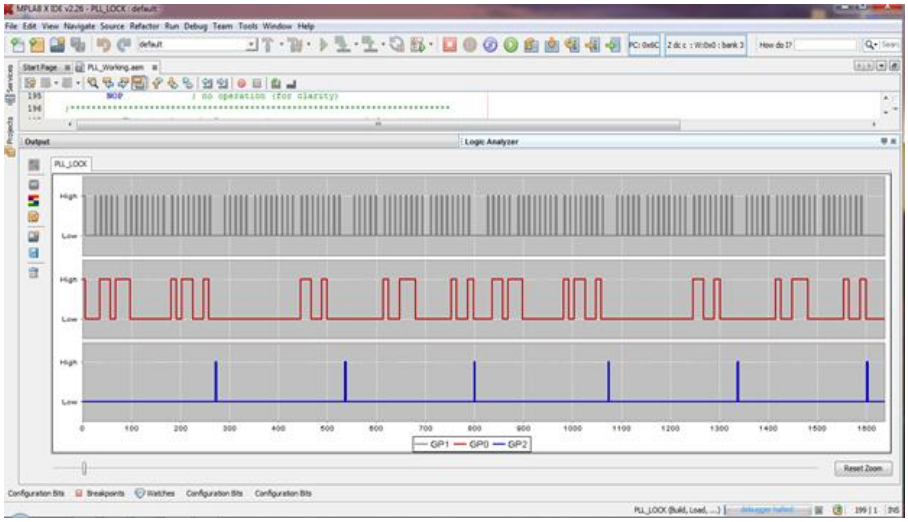

Fig. 3. Timing diagram for loading data from the microcontroller

The curve describes the phase noise of 1GHz TCXO signal. The lock time is important in communication synchronization as moving from on base station to other base station. The Fig. 4 describes the 250MHz VCXO frequency is locked with 10MHz TCXO frequency and it does not exceed 2.5V. The plots of the phase noise spectral density versus frequency offset are presented on Fig. 7.

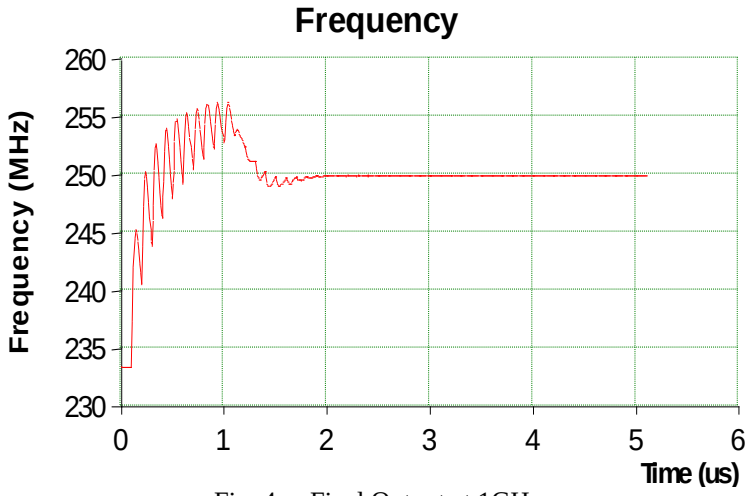

Fig. 4. Final Output at 1GHz

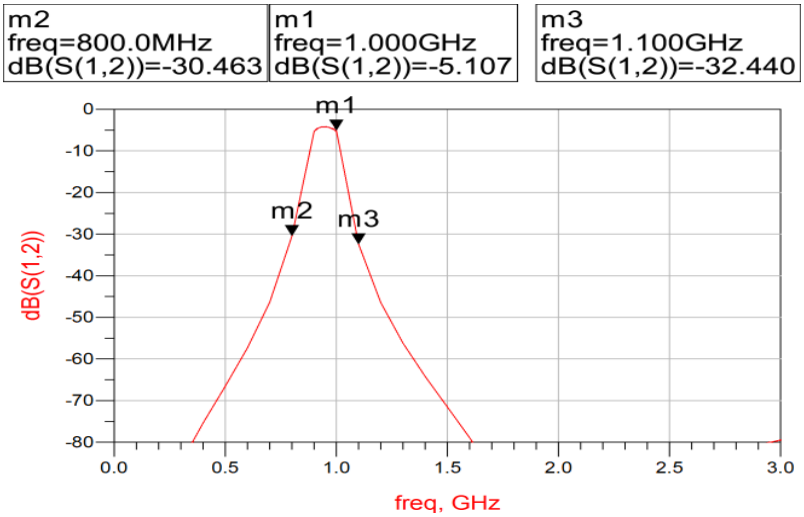

Fig. 5. 1GHz output

Temperature stability is a measure of how much the oscillators frequency varies over temperature.

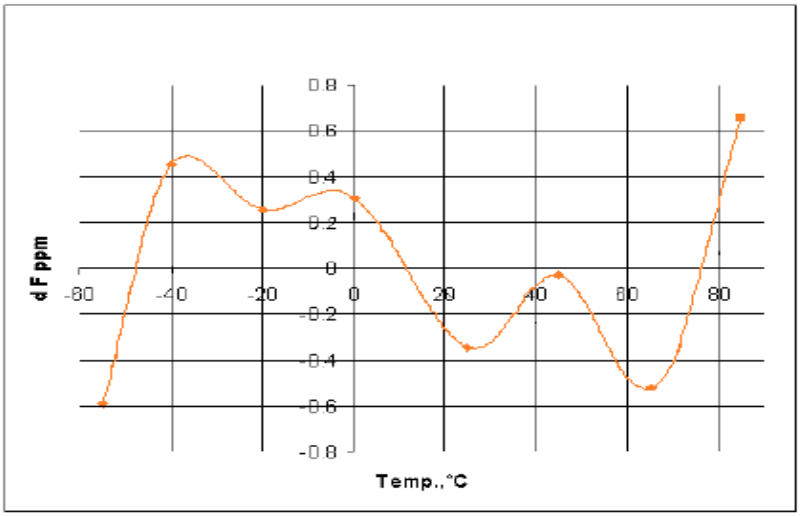

Fig. 6. Temperature stability curve

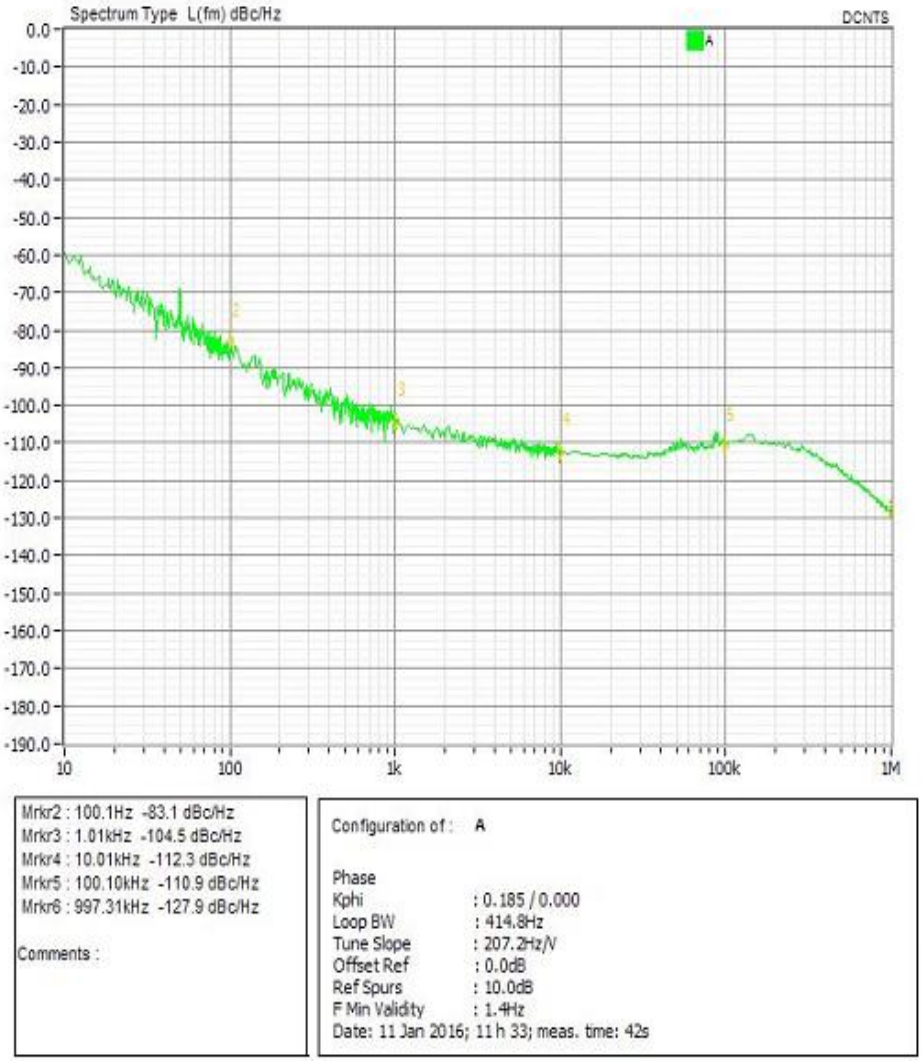

Fig. 7. Phase Noise plot of 1GHz TCXO

VII. Conclusion

Accurate synchronization can be achieved in digital communication using this technique. Low phase noise, high frequency stability TCXO can operate in UHF band in a small SMD package device. The lock time of PLL is less than 10microseconds. Also AT-cut crystal produces accurate frequency stability over temperature. The frequency stability does not exceed ± 0.5 ppm over temperature -40^{o}C to 85^{o} C range with good aging and tight initial calibration, provided by the low frequency reference.

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