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Low Power Implementation of RISC-V Processor

Shashi Kumar V[1], Gurusiddayya Hiremath[2]
[1](Electronics and Communication Engineering, Sahyadri College of Engineering and Management, India)
[2](Electronics and Communication Engineering, Sahyadri College of Engineering and Management, India)

Abstract:*This paper presents the implementation of RISC-V processor with low power optimization techniques. To minimize the power of the processor techniques as clock tree optimization and clock gating to reduce dynamic power along with Multi-Vth, Power Shut Off (PSO) and Multi Supply Voltage (MSV) to reduce leakage power are proposed. Synthesis is done using Encounter RTL Compiler to generate netlist at the gate level and the back end flow of VLSI design is carried out on Cadence Encounter Digital Implementation System using the power intent captured by the Common Power Format (CPF) which aid in the low power implementation the processor.*

Keywords: *RISC-V, Low Power, Clock Gating, Multi-Vth, Multi Supply Voltage, Power Shut Off, Common Power Format*

I. Introduction

Today in the design of System on Chip (SoC) the most crucial issue is the alarming increase in the rate of power (watts per sq. millimeter) consumption. Thus it is mandatory from a chip engineering perspective to emphasize power management in almost every field of chip design to incorporate low power techniques starting at the architecture stage for effective energy management in each stage of the design that is from RTL to GDSII.

This rather alarming trend was first noted by Fred Pollack of Intel in his key note at MICRO-32 in 1999. He observed that the power density is increasing at an alarming rate and rocketing to the point of being the hottest man made object on this planet. The trend of power density versus power design requirements for today's SoC gap is widening and has become a challenge to designers of wireless, portable, consumer and other electronic products. Thus design efforts in power management are scaling upwards due the necessity for low power as well as for performance and costs.

Presently management of power is mandatory for all designs of 90nm and below because with the shrinkage of device geometries the leakage current increases rapidly. The management of this leakage current has high influence on the design as well as the implementation choices, as for few libraries and designs, leakage current surpass dynamic switching currents, hence becoming the source in squandering of power in CMOS.

Until now the primary concern was to improve performance in the designs and reducing silicon requirement thus lowering manufacturing expenses but this trend is losing to power management as the key concern in SoC designing. All SoC designs are affected these power challenges with upward thrust in growth of personal, wireless and mobile communications along with home electronics calls for high speed computation and complex functionality for challenging market growth. Today's innovative products are expected to be not only small, lightweight, and cool, but also prolonged battery life, less heat and lower power requirement.

RISC-V is newly introduced instruction set architecture (ISA) which is free that in the beginning was designed to hold up education and research of computer architecture and at present lay to be a standard open architecture for industry implementation being under the control of RISC-V establishment. This architecture initially been elaborated at the University of California, Berkeley in EECS Department under the computer science branch.

II. Existing Systems

As seen most of the instruction set architectures (ISAs) may be proprietary and we do have companies with triumphant ISAs like Intel, IBM and ARM have got patents on idiosyncrasy of their ISAs, which avert others from using them without a permit from the respective company to use or modify the ISA with the needs. Negotiations take months and it tends to peak up the cost, which make it difficult for community apprehensive with the stalk of education and research, and small organizations. We also see that license from companies like ARM forbid to design an ARM core; but just use their designs, same goes with IBM in perspective of OpenPOWER ISA. All these restrictions do not allow the designers to design and share their ISA reconcilable cores. It may also be seen that most accepted ISAs aren't the most desirable ISAs as we can't change it as with our requirements for example ARM and 8086 aren't considered best ISA epitome. Considering Proprietary ISAs, they are not assured to last because if a company shuts down so does its ISAs with it; an instance of this

situation is the decease of DEC's also brought an end to the VAX and Alpha ISAs. To overcome these issues, we should have an open ISA to attain sizeable innovation, and with shared open core designs and higher quantity of devices possess an advantage of shorter mean time to market and cheaper price, hence affordable.

III. Project Overview

The main idea behind the project is to have an efficient low power RISC-V processor with DFT. The following power management techniques for switching and leakage power reduction are being applied to the design,

i. Multi-Vth
ii. Clock Gating and Clock Tree Optimization
iii. Multi-supply voltage
iv. Power Shut Off (PSO)

3.1. Multi-V_{th}

Gates with different thresholds are utilized in Multi-V_{th} optimization for optimizing the major constraints of VLSI design namely power, timing and area. Generally, libraries are made available for use by vendors constituting cells with dissimilar switching thresholds so that the tool used to synthesize design for low power application which makes it possible to pervade all the multi threshold cells available in the libraryensuingan effect onarea and area constraints with a possibility of power dissipation at its lowest level.

A design with the specialpurposeHigh-V_{th} cells where possible in the netlist is the common trend used in leakage reduction technique. While the Low-V_{th} gates respond faster to signals from input end and leakage power consumption is more, whereas the gates with High-V_{th} switches at a slower rate, but leakage power consumption is less. So the tool used for synthesis should be able to control the extent of highest leakage power by executing multi-V_{th} leakage optimization on the design. The High-V_{th} cells are chosen by the compiler in order to replace it with the cells with Low-V_{th} in places where critical timing path is not affected thus Low-V_{th} cells can replace in areas where timing is not so critical factor.

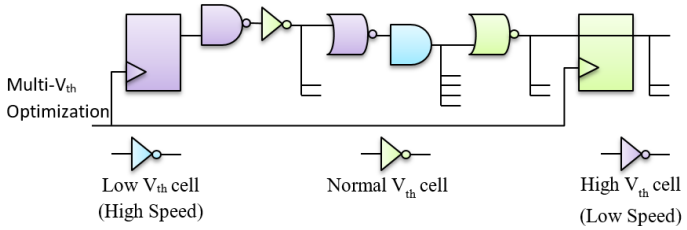

Fig. 1. Multi-V_{th} Optimization

3.2. Clock Gating and Clock Tree Optimization

In the typical working mode, the clock continuously toggles at every clock cycle immaterial of any function or operation is associated by its switching operation. Thelarge source of dynamic power is clock trees due to the high rate of switching activity and usually have a very large capacitive loads. In case data being loaded into registers are irregular instants of time; a notable quantity of power is wasted. So by clock gating which can automatically shut off the blocks which are not required to be active by ensuring that when the blocks are in idle condition the power is not wasted. This clock gating can occur at either at the register or at higher up in the clock tree. The entire clock tree for the block shall be disabled by applying clock gating atblock level, ensuring clock network switching reduction thus reducing dynamic power, which is of great value.

In many a designs the registers, data is not loaded in a stream though the clock signal keeps toggling at every clock cycle. Usually the clock signal drives a very large capacitive load resulting in extreme dynamic power dissipation.

Power dissipation is reduced by clock gating for reasons mentioned below:

a. In idle period power is not dissipated if the gating function shuts off the register.
b. In the gated-clock circuitry itself the power is saved.
c. The enable circuitry logic is removed from the original design.

Clock-Enabled Register Example:

If you look into a multiplexer (MUX) of a register's data input, the enable signal controls the MUX. If in a flip-flop, the data input is brought down to a MUX between output pin and data pin of the flip-flop, it is possible to be modelled by synthesis tool by connecting the data input to the data pin of the flip-flop without any interfering logic blocks and also the MUX enable is used to gate the clock signal of the flip-flop through an additional installed element for gating the clock.

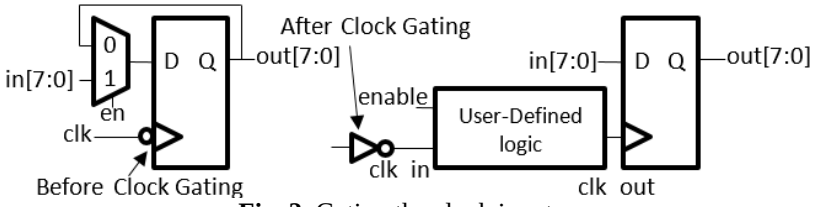

Fig. 2. Gating the clock input

De-Cloning of Local Clock Gating:

In many registers in the design uses a common enable clock-gate logic signal, compiler of a RTL can merge all these instances of clock-gating for allpreviously mentioned similar registers which are gated. This series of steps takencan be summoned as local clock gate de-cloning.

3.3. Multi-Supply Voltage (MSV)

On the basis of requirements of performance operating different blocks at different voltages is the function of Multi-Supply voltage technique. MSV technique approach is the key to reduce power but level shifters are required on signals where the voltage level vary. So if the level shifters are not used, the signals cannot be sampled accurately that cross voltage levels. Thus MSV can reduce SoC's power consumption which do not require all those blocks to operate at stipulated peak speeds always. So designers of the chip incorporate MSV on different blocks based on their performance requirement.

MSV synthesis include the following features:

Domains with multiple voltage, assign libraries and blocks to domains, up-down analysis and optimization, insertion of level shifters. A concept known as power domain which gives a detailed account ofa group of design blocks or signals which share the identical supply voltage are used in synthesis in describing blocks that are switchable having non-identical voltages incorporated with level shifters that ensure the correct operation when integrated with SoC. Level shifters should assure the genuine voltage level and signals with error free timing as passes from a level of voltage to another either way.

3.4. Power Shut-off (PSO)

Power Shut Off is among the preponderance efficacious techniques or so called power gating, when the blocks of the chip that are not in being utilized switches the power off to those parts of blocks and can save almost completely any leakage current. PSO is made use in when the block goes to standby mode by shutting off power. A particular power down concatenation is needed along with seclusion on signals from the domain that is going to be shutdown. Untimed power up/down are the important source of fallacy that can lead a chip to re-spin. Thus there is need for it to be faultlessly and comprehensively verified along with working RTL ensuring that the chip operates as it is intended to with blocks turned off while the system can recuperate after the units been powered up. The use of power shut-off needs isolation logic and if available state retentive power gating(SRPG) for MSV along with level shifters. Here the power domain concept is used the major role of the synthesis is adding isolation cells automatically basing on CPF. PSO do not affect much the synthesis unless it needs to insert state retention cells and/or always on cells. Connecting the power switch to the power control module is operational during physical implementation flow only when physical information is known.

State Retention Power Gating (SRPG):In unequivocal circumstances there is need forretaining the state of control flops of crucial importance power in the course of power off state in certain blocks of a design and re-establish to prior state after power-up sequences. So as to implement PSO, state retention cells are considered essential to store existing state of the blocks before it is shutdown. Thus retaining by the use of flip-flops of the systems state throughout the time of power down while at sleep mode all the combinational logic will be turned off.

Isolation: Preventing from floating, unpowered signals at the output of a power down block is where the isolation logic is used.

IV. SoC Block Diagram

The Rocket SoC Generator generates n tiles with Host Target InterFace (HTIF) and Uncore. The tile consists of the core, Floating Point Unit (FPU), Rocket core (ROCC) Accelerator, Instruction and Data cache. The Uncore consists of (Coherence agent, Tile interface and Host interface).

FPU - Designed to carry out operations on floating point numbers.

(ROCC) Accelerator – It changes the priority of a process by allocating more CPU power to the current active process.

Coherence agent – Used to overcome the issue of Memory coherence that influence the design of computer systems in which multiple processors or cores been allotted a common area of memory.

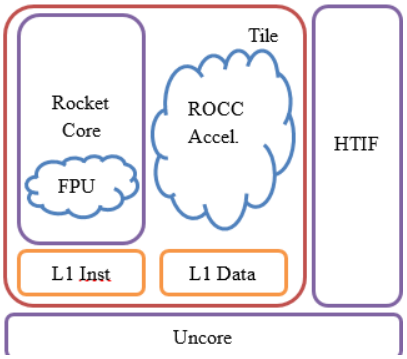

Fig. 3. Rocket Core SoC

V. Results

The complete placement and routing flow is done on Cadence Encounter Digital Implementation System tool. The following screenshots show the placement of Isolation/level shifter combinational cell (Fig-4), State Retention cells (Fig-5), Power switches (Fig-6) andRouting (Fig-7).

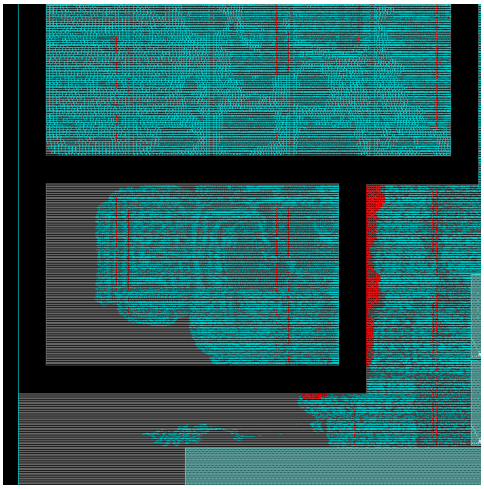

Fig. 4. Isolation/level shifter combinational cell

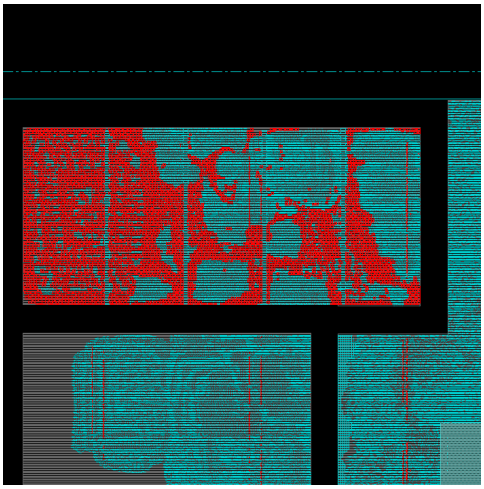

Fig. 5. State Retention cells

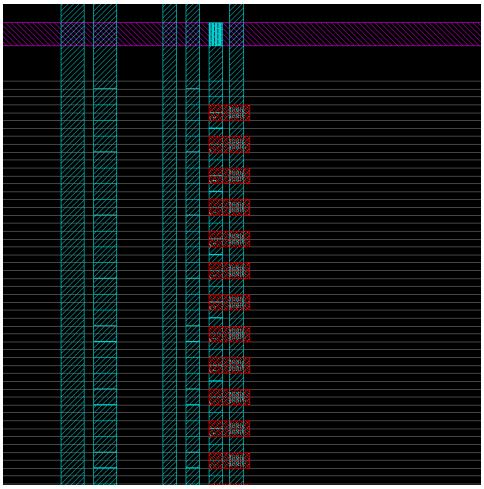

Fig. 6. Power switches

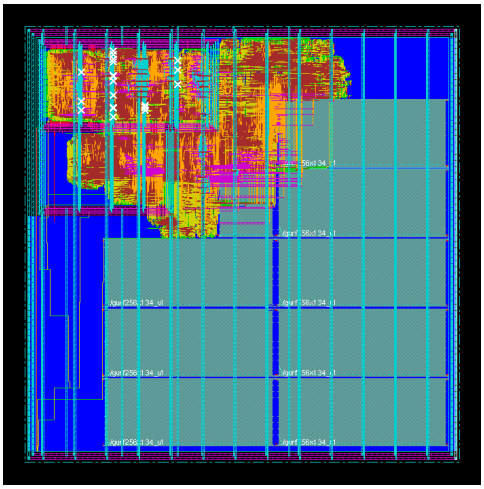

Fig. 7. Routing

Table 1. Comparison of Obtained Results

Technique	Internal Power (W)	Switching Power (W)	Leakage Power (W)	Total Power (W)	Area (μm^2)
Without Low Power Approach	6.287	2.387	0.01439	8.688	2333692.0
With Clock Gating Approach Alone	2.215	0.9514	0.01461	3.181	2308018.3
With Combination of Rest Mentioned Low Power Approaches	1.615	0.789	0.01175	2.415	2374572.1

VI. Conclusion

At the employment stage for the low power techniques are accompanied by entanglement and issues of its own, but it is possible to resolve these issues with the right methodology, awareness about low power, tools and standards.

- An undeviating aim to encapsulate the objectives of power by utilizing a format for power being a standard like Common Power Format from Silicon Integration Initiative.
- Manual manipulating the formulations of low power like the power switches, level shifters, retention and isolation cells, etc. are to done by the EDA tools for implementation using CPF.

To follow the above aspect there is a need for the designer to possess a knowledge of all the components and formulations of low power techniques conceptually. As low power come to the fore and increase in the automation on the ground of CPF, change around of area, performance and power is possible to be observed as the improvement of the design and employment. Power trade-offs will become the added center line in the design. The conventionally area and timing were only the trade-off constraints but now power also have become another challenging constraint in the design.

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