IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 3, Ver. I(May. -Jun. 2016), PP 82-88
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design of an Operation Amplifier for Switched Capacitor Filter Application with 50 Mhz Unity Gain Bandwidth And 42.5dB Gain

Nirav Desai, Ramesh Harjani,
University of Minnesota, Twin Cities

I. Introduction

The goal of the project is to design a high gain bandwidth op-amp to be used in a switched capacitor filter for baseband sampling in a DECT receiver [1]. DECT requires a 700KHz baseband bandwidth, which sets the anti-aliasing sampling frequency to 1.4MHz. Adding another 5X oversampling to adequately suppress higher frequency aliases, takes the sampling rate to 7MHz. Sampling at 10X the highest desired frequency should also be enough for the continuous time approximation necessary for switched capacitor filtering.

Using the approximation that a unity gain bandwidth of 10 times the clock frequency would give adequate performance in an op-amp, a unity gain bandwidth of 70MHz would be desirable. A 50 MHz unity gain bandwidth was picked as the target as a compromise between a stable high frequency performance and adequately high sampling rate. A power specification of 1 mW was picked as achievable for this design. A fully differential design was picked because of its advantage in common mode noise rejection. CMRR of 70dB and PSRR+/- of 70dB was picked for rejecting common mode noise and allowing integration with noisy ADC supply voltage. A high gain would help minimize charge injection non-idealities in a switched capacitor filter and 100dB gain was picked for this design. 45dB gain would give a 10% charge injection error and so this would be a good gain target. A high dynamic range would give better SNR and improve the ADCs ENOB. Dynamic range of 100dB was picked for this design.

Since the slew rate determines the settling time for switched capacitor applications, a slew rate becomes an important design constraint. For a 2MHz clock, the clock period would be 500ns and for settling time less than 1/10 of the clock cycle, the slew rate will become 1V/5ns = 200V/usec.

Summary of Design Specifications:

Design Specification	Target
Supply Voltage	3.3V
Gain	45dB
Bandwidth	100MHz
Phase Margin	50 degrees
Power Consumption	0.5mW
Dynamic Range	100dB
Slew Rate	200V/usec
CMRR	70dB
PSRR+	70dB
PSRR-	70dB
Settling Time	<30nsec
On-Chip load	5pF

II. Design

Considering the gain – bandwidth requirements, a number of options were considered ranging from 2 Stage Miller Compensation to Multistage Nested Miller Compensation.

Since a gain of 45dB would be sufficient for 10% error, Multi Stage Nested Miller Compensation was not used. A 2 stage Miller Compensation would give sufficient gain with extra area and power and was an attractive design option. The final design uses a single stage fully differential telescopic cascode op-amp as shown in figure below.

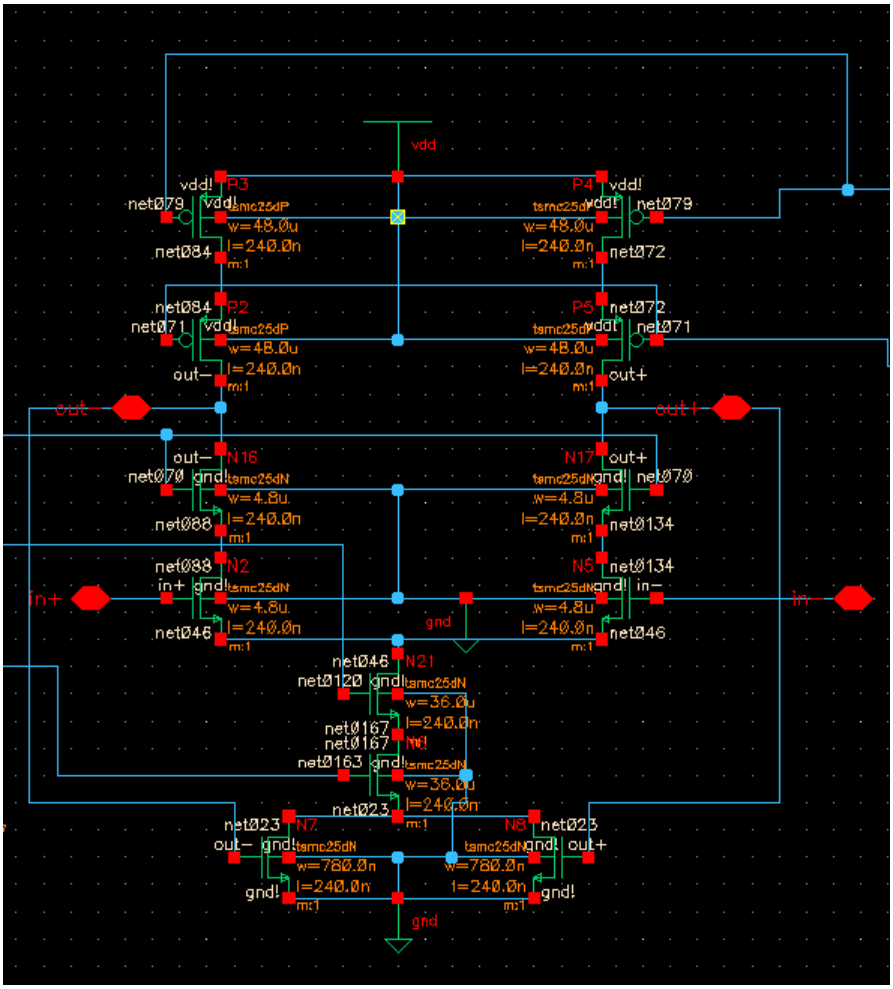

Figure 1: Single Stage Fully Differential Telescopic Cascode Op-Amp (NMOS W/L Changed to 48/0.24um)

Each arm current was set to a current of 110uA giving a slew rate of 20V/usec. This would increase the settling time requirement to 50ns or could give lower settling time with lower voltage swing. The design implemented was tested using a 1V sine wave giving a slew rate requirement of 60V/usec for 5nsec settling. Cascoding was used in the current source, NMOS transistors and PMOS transistors to improve the CMRR and PSRR respectively. The final design is shown in Figure 1.

The design procedure is as follows: The output impedance on a minimum length NMOS and PMOS were measured. (Minimum lengths were taken for best high frequency response). The widths were chosen as 48um arbitrarily. The NMOS and PMOS output impedances were measured as 22Khoms and 16Khoms respectively. For a W/L of 48/0.24, the trans-conductance of NMOS was found to be 2.6mS giving a gain of about 58.85dB. A low voltage cascode biasing was designed and power saving was achieved by reducing the current in the biasing arms and scaling down the W/L ratios.

The following Figures 3 and 4 show the biasing used.

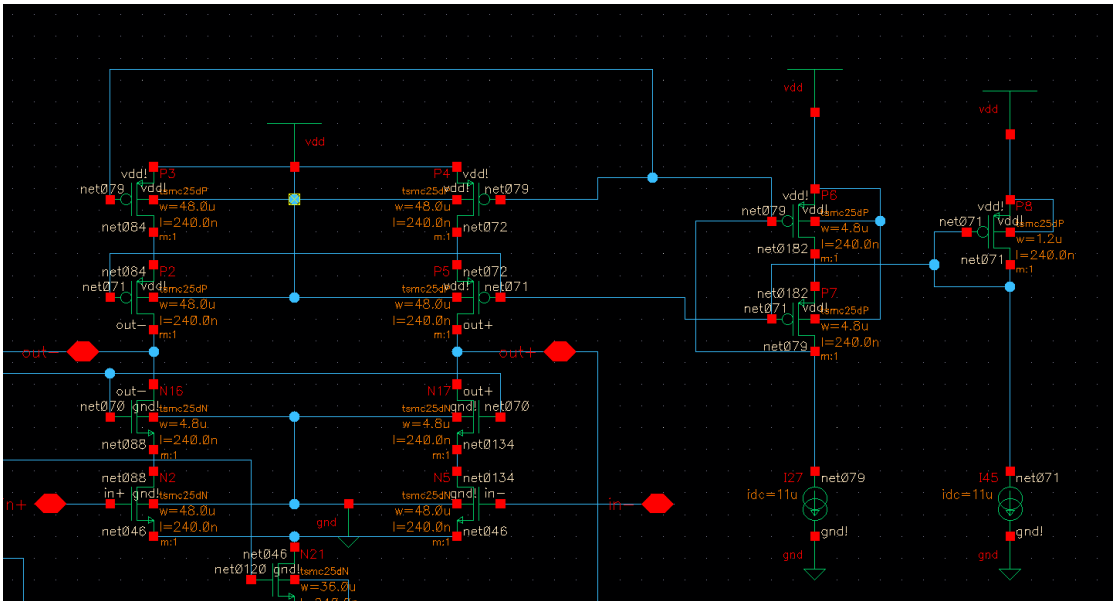

Figure 2: PMOS Low Voltage Cascode Biasing with cascode transistor biased using a PMOS having W/L ¼ of the W/L of the PMOS transistor biasing the main transistor.

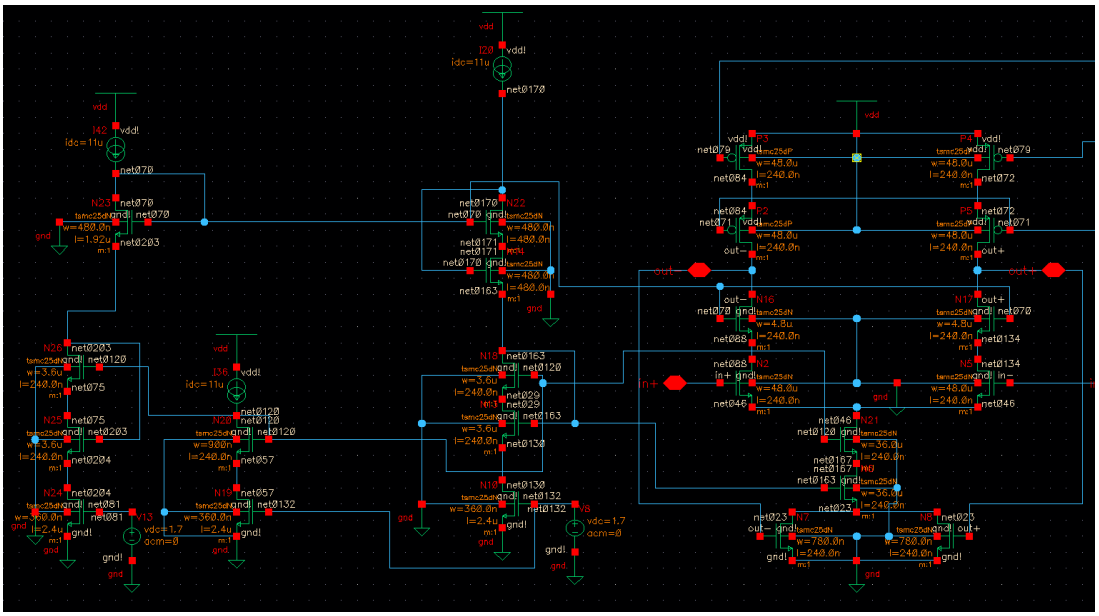

Figure 3: Biasing for NMOS Cascode, NMOS Current Source Cascode and Common Mode Feedback using triode transistors.

Since the fully differential telescopic cascode will have only one dominant pole, compensation will not be a problem.

III. Simulation Results

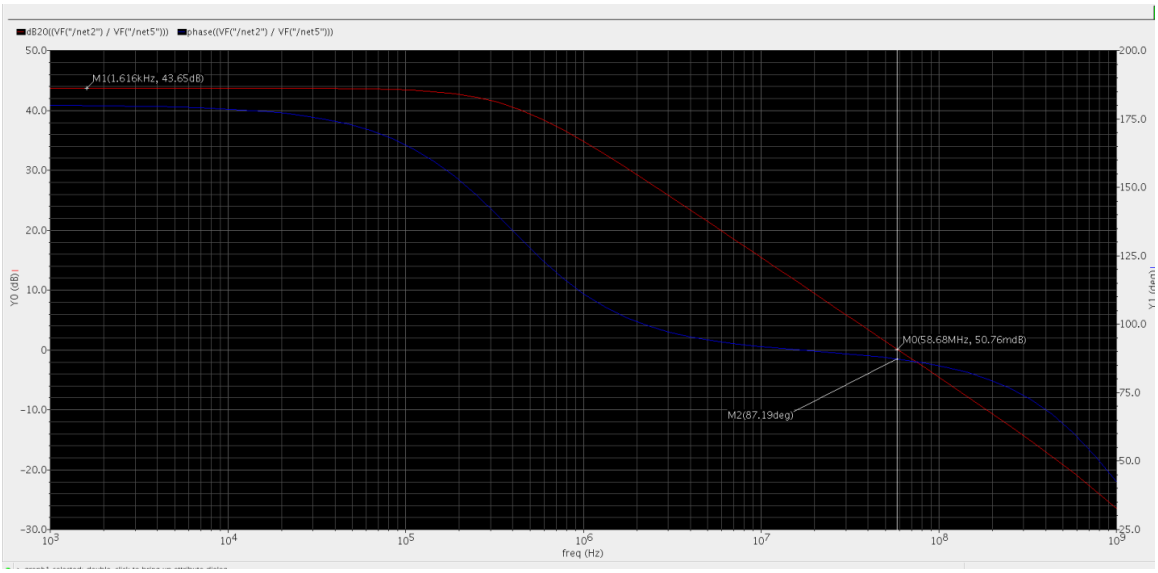

Figure 4: Simulate gain and phase response for single stage telescopiccascode op-amp. DC gain is 43.65dB and UGF is 58.68MHz with a phase margin of 92.81degrees.

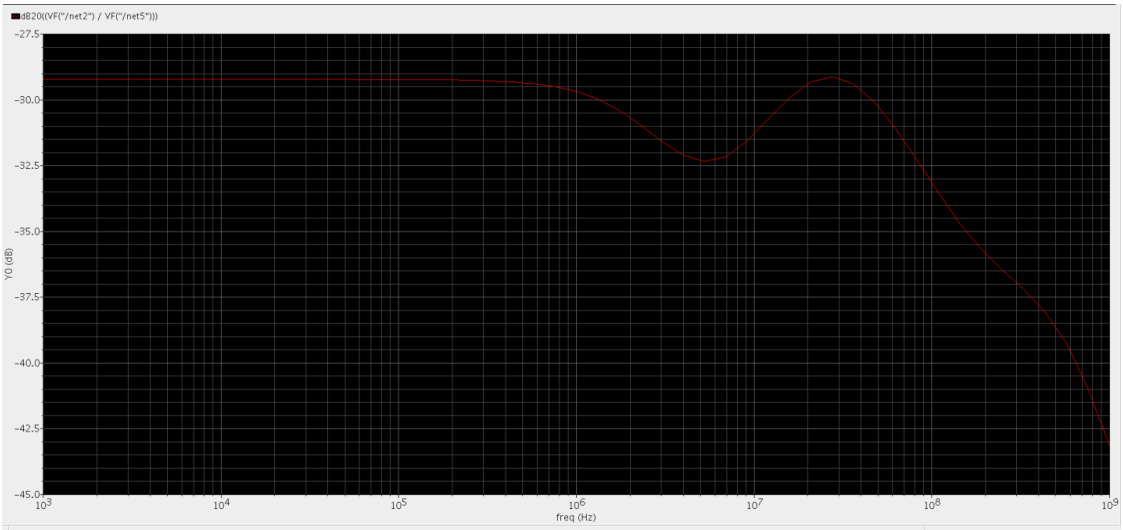

Figure 5: Simulated CMRR is -29dB with a 3dB bandwidth of 2 MHz.

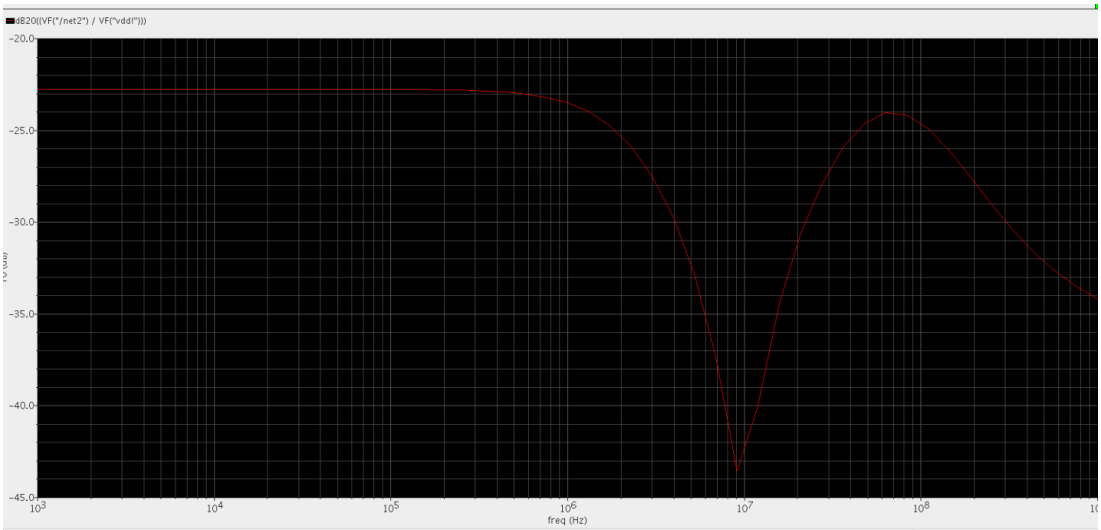

Figure 6: Simulated PSRR is -23 dB with a 3 dB bandwidth of 2 MHz.

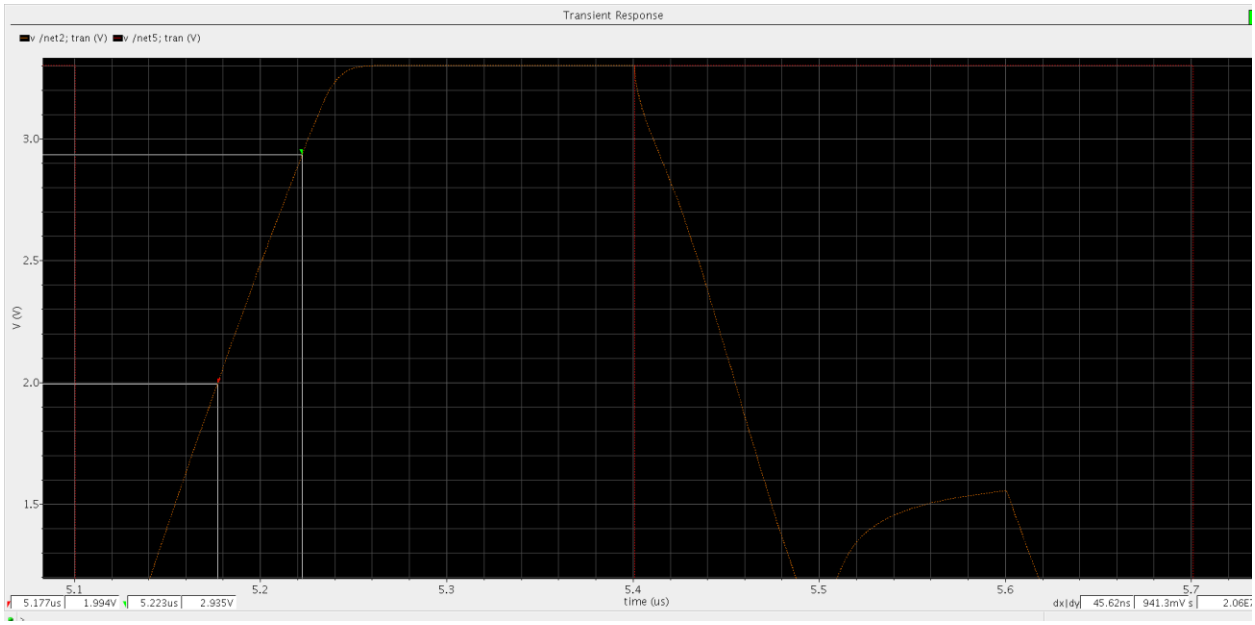

Figure 7: Slew Rate of Op-Amp ~20V/usec

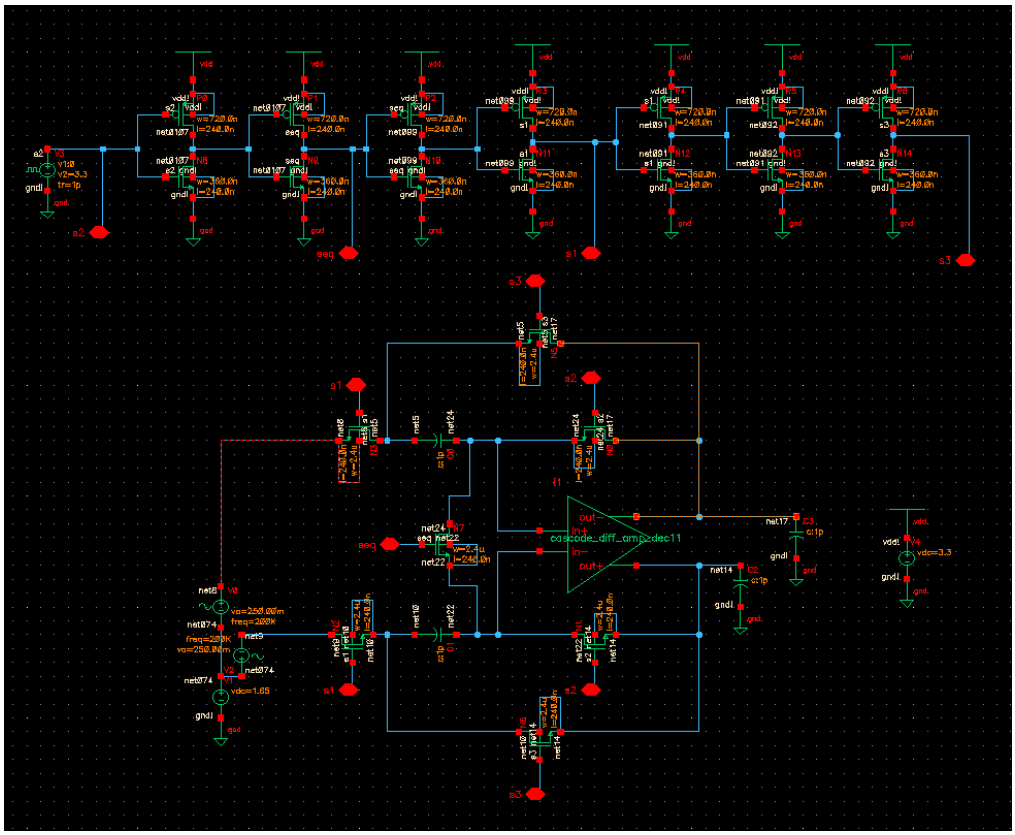

Figure 8: Op-amp configured for test as unity gain follower

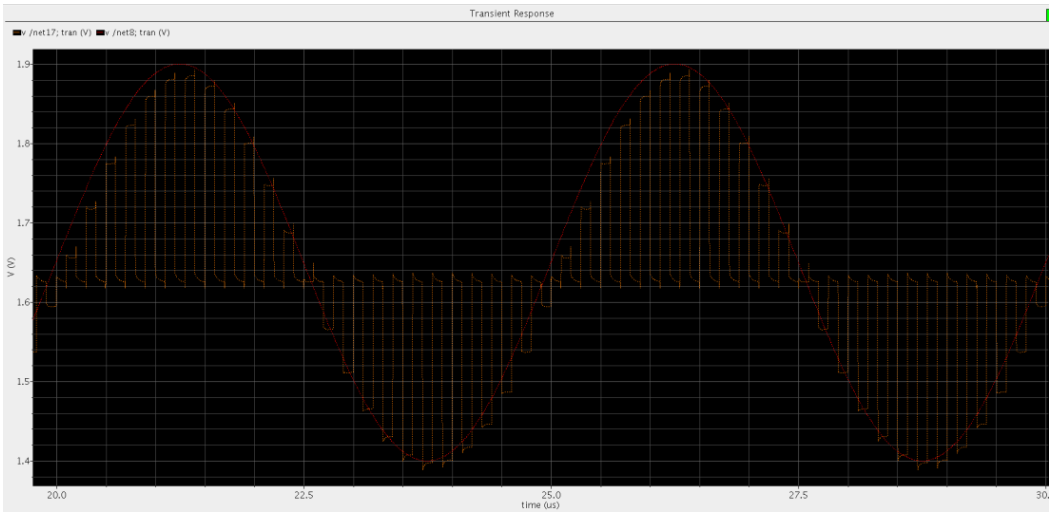

Figure 9: Op-Amp response in the unity gain follower configuration. The 98degree phase margin gives a slow settling response and slewing remains a smaller fraction of the total swing at output. Settling Time ~ 187nsec

Summary of Simulation Results

Supply Voltage	3.3V
Gain	42dB
Bandwidth	50MHz
Phase Margin	92.81 degrees
Power Consumption	0.923mW
Dynamic Range	Not measured
On-Chip load	1pF
Slew Rate	20V/usec
CMRR	-29.25dB
PSRR+	-23dB
PSRR-	Not measured
Settling Time	187nsec

Circuit Layout

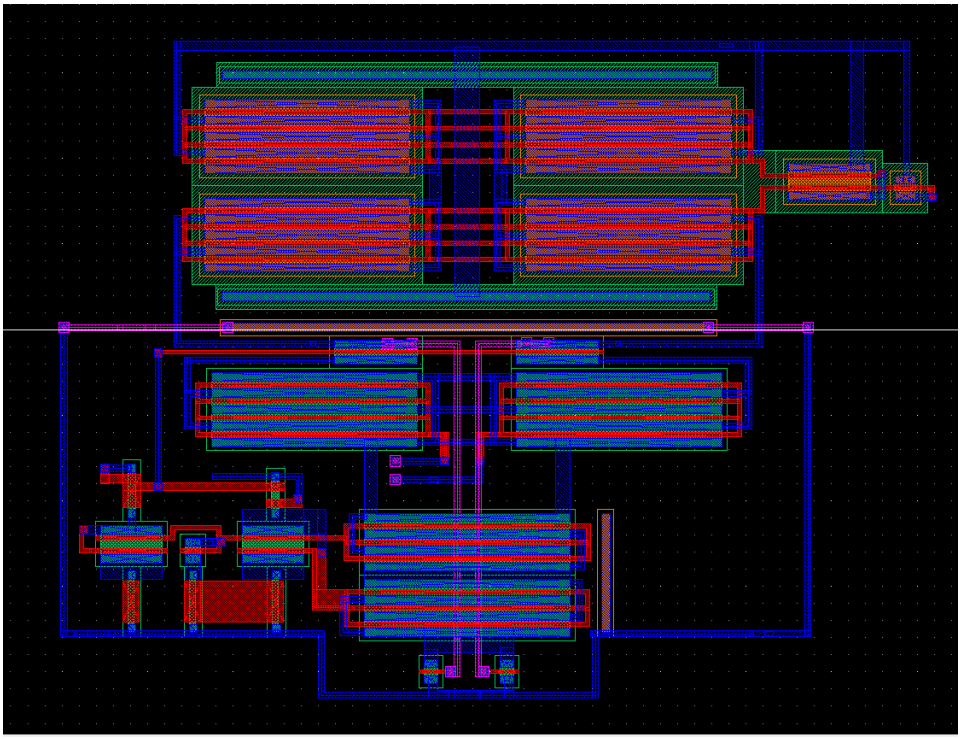

Figure 10: Op-Amp Layout with the biasing network and common mode feedback using triode mode transistors

References

[1]. A 1.9GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications, Jacques C. Rudell, Jia-JiunnOu, Thomas B. Cho, George Chien, Francesco Brianti, Jeffrey A. Weldon, Paul R. Gray, IEEE International Solid State Circuits Conference, pp. 304-305, 476, February 1997
[2]. Multi Stage Amplifier Topologies with Nested Gm-C Compensation, Fan You, Sherif H. K. Embabi, Member, IEEE and Edgar Sanchez-Sinencio, Fellow, IEEE, IEEE Journal of Solid State Circuits, Vol. 32, No. 12, December 1997
[3]. Data Converters by Franco Maloberti
[4]. CMOS Analog Circuit Design by Philip E. Allen Douglas R. Holberg
[5]. Design of Analog CMOS Integrated Circuits by BehzadRazavi