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Digitally Controlled Delay Lines

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Abstract: *In Digitally Controlled Delay Lines (DCDL) there are different ways to optimize the design of the circuit. DCDLs are used in number of applications such as phase locked loops and delay locked loops. They are used to mainly process the clock signals. These lines produce a programmable delay to the output with respect to the input and also adjust the relative difference between the two signals to produce the reliable data transfer. It is also finds its applications in digital- to-analog converter where time domain resolution is given more importance than the voltage resolution. A digital delay line includes a plurality of delay elements, arranged in sequence having an associated control input.*

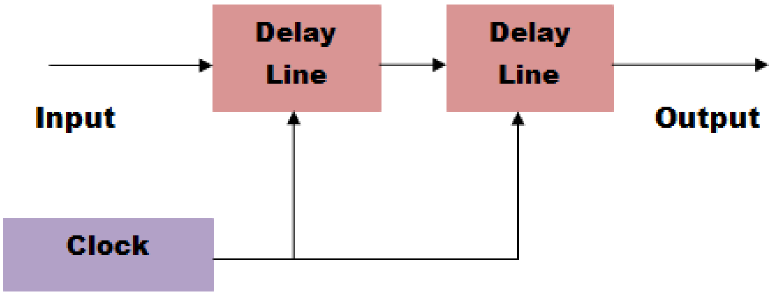


Figure 1: Delay line block diagram

I. Introduction

Basic delay circuit using NOR gates

The basic delay circuit has been constructed neither using NOR gates as shown in the figure below:

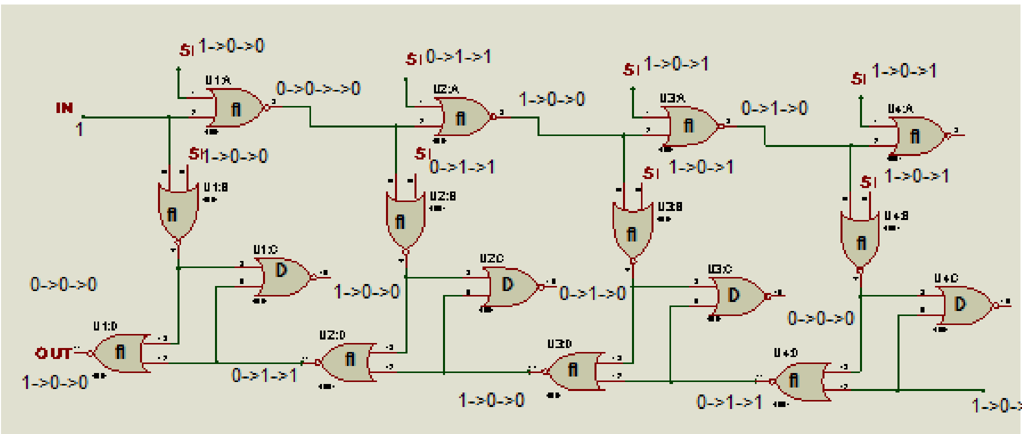


Figure 2: DCDL with NOR gates

In this circuit the NOR gates marked with 'A' are fast gates and the gates marked with 'D' are dummy gates used for load balancing. Here delay of the circuit is controlled by the control bit Si. When Si=0 the circuit is in pass state. If Si=1 it is in turn state.

The drawbacks of this circuit are the output of the circuit has glitch which leads to loss of data. To overcome the glitches the circuit has been modified to the circuit shown in figure 3.

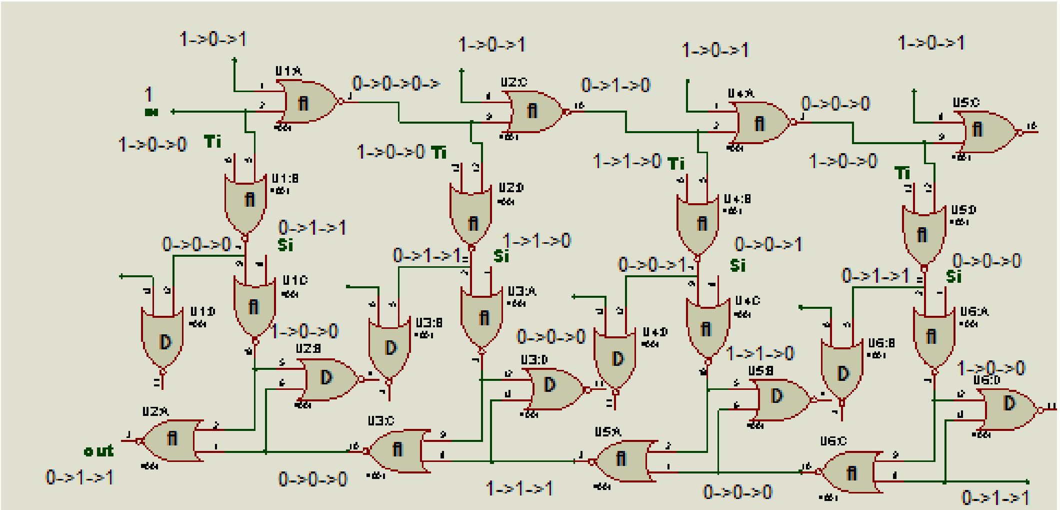


Figure 3: Modified DCDL circuit without glitches

In this figure “A” denotes the fast neither input of each NOR gate. Gates marked with “D” represents dummy cells added for load balancing. When Si=0 and Ti=1 the NOR “3” output is equal to 1 and the NOR “4” allows the signal propagation in the lower NOR gates chain. And if Si=1 and Ti=1, the state is turn state. In this state the upper input of the DE is passed to the output of NOR “3”. If Si=1 and Ti=0 the state is post-turn state. In this DE the output of the NOR “4” is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NOR “3” through NOR “4”. In this circuit the first DE is never in post-turn state, therefore T0 is always 1.

Power optimization of the circuit:

The power of the circuit can be optimized in 2 methods

1. Using an enable signal

In this method the input to the circuit is given through an AND gate whose inputs are the input to the circuit and an enable signal. Whenever enable is high the input is given to the circuit or else the input is disabled.

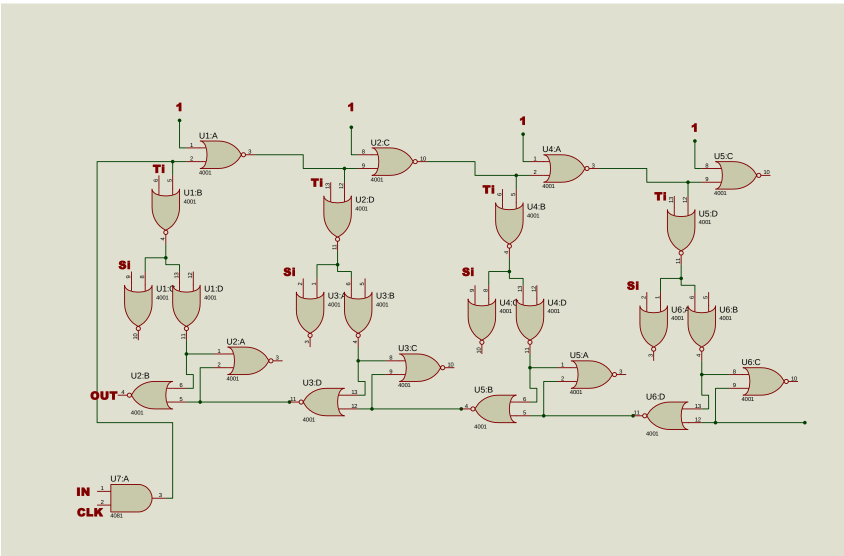


Figure 4: Optimization by clock gating for non-inverting NOR based DCDL

In this circuit the input to the first NOR gate is given with through an AND gate. Through this gate the input can be given to the circuit only when necessary. This process helps in reducing the power consumption of the circuit. In this method the leakage current can be reduced as there is no input when the clock is gated.

2. Using multiplexers in place of NOR gates

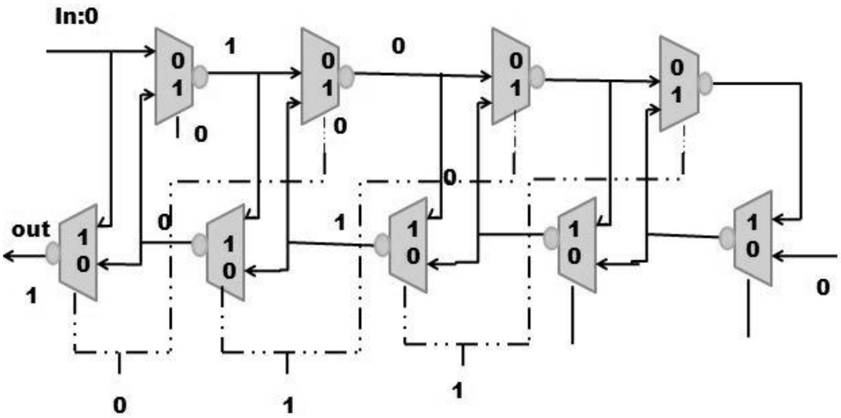


Figure 5 : Optimization by using Multiplexers

In this method all the each DE (delay element) in figure 3 are replaced by multiplexers as shown in figure 5. When multiplexers are used instead of delay elements the number of gates used in the circuit reduces. In any delay element used in a DCDL circuit without glitches there 6 NOR gates used whereas in a multiplexer that gives inverted output there are only 4 gates used. This reduces the area consumed by the circuit as well as the dynamic power consumed by the circuit.

II. Results

Simulation results for the DCDL circuit with glitches

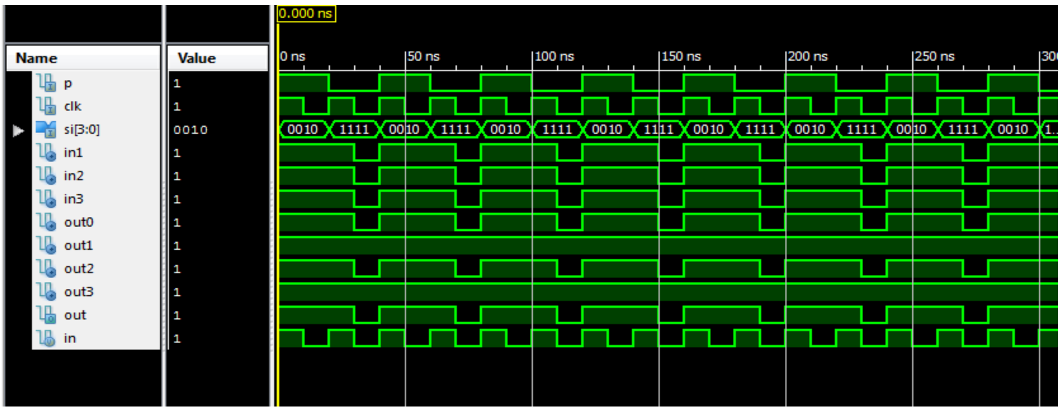
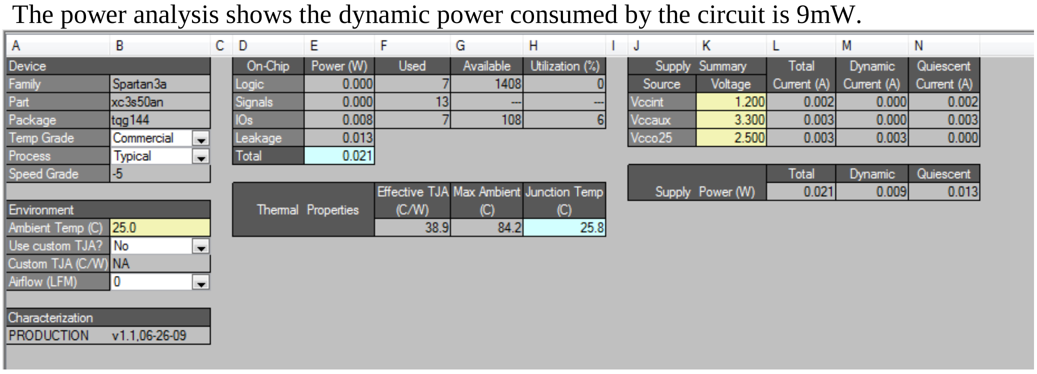


Figure 6: Simulation results for DCDL circuit with glitches

As seen in the above simulation due to glitches the high output runs for more time compared to the low output. This leads to loss of data in the circuits. To get over the loss of data the circuit, the DCDL circuit has been modified to the circuit shown in fig 3.

Power analysis for the DCDL circuit with glitches

The power analysis shows the dynamic power consumed by the circuit is 9mW.



Device	
Family	Spartan3a
Part	xc3s50an
Package	tqg144
Temp Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.1,06-26-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	7	1408	0
Signals	0.000	13	---	---
IOs	0.008	7	108	6
Leakage	0.013			
Total	0.021			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.9	84.2	25.8

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.002	0.000	0.002
Vccaux	3.300	0.003	0.000	0.003
Vcco25	2.500	0.003	0.003	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.021	0.009	0.013

Figure 7: power analysis of DCDL circuit with glitches

The figure below show the simulation results of the proposed DCDL circuit.

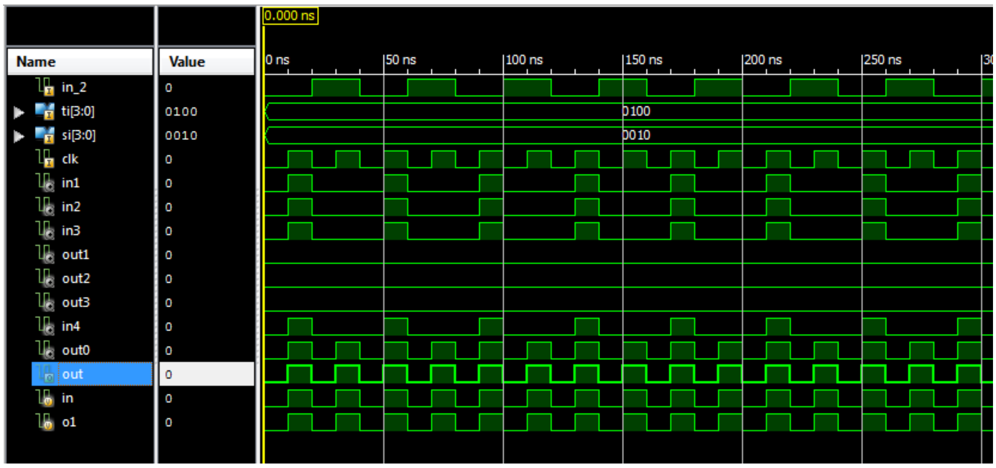


Figure 8: Simulation waveform of proposed DCDL without glitches

This simulation results show the DCDL circuit without glitches. 'in' is the input to the circuit, 'out' is the output of the circuit and the control signals are 'ti' and 'si'. The signals in1-in3 represent the outputs to the upper NOR gates and out1-out3 represent the outputs of the lower NOR gates 'o' represents the input to the last NOR gate in the lower row and 'in4' represents the second input to the upper NOR gates.

The power consumption of the circuit when checked on the FPGA is as shown below:

Device	
Family	Spartan3a
Part	xc3s50an
Package	tqg144
Temp Grade	Commercial
Process	Typical
Speed Grade	-4

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.1,06-26-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	4	1408	0
Signals	0.000	15	---	---
IOs	0.008	12	108	11
Leakage	0.013			
Total	0.021			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.9	84.2	25.8

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.002	0.000	0.002
Vccaux	3.300	0.003	0.000	0.003
Vcco25	2.500	0.003	0.003	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.021	0.008	0.013

Figure 9: Power consumption of the DCDL circuit without glitches

The figure below shows the simulation results of the DCDL circuit with the input given through an 'AND' gate.

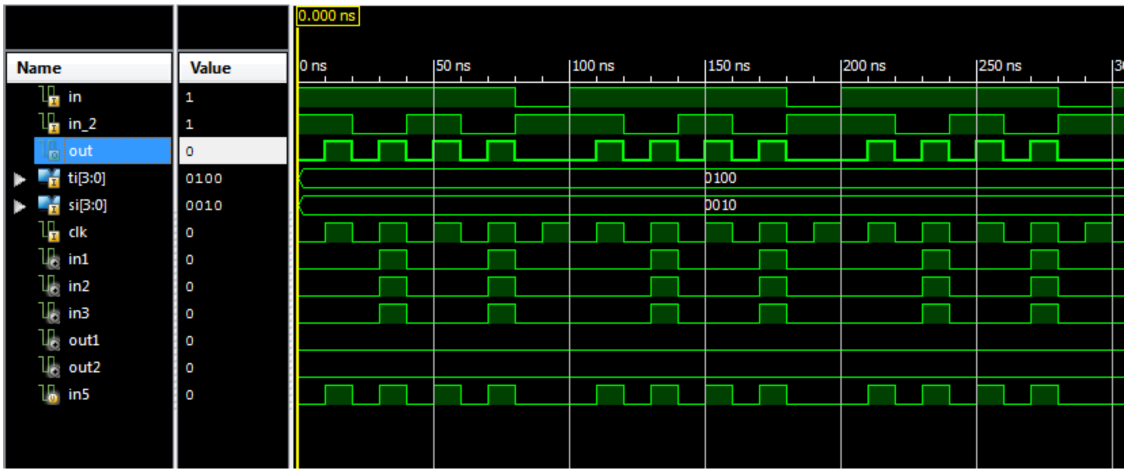


Figure 10: Simulation waveform of the DCDL circuit with input through AND gate

As seen in the simulation waveform above the input to the circuit is given only when 'in' which is the input to the AND gate is active. Thus the circuit is active only when the 'in' is high. The power consumption of the circuit is as shown below:

Device	
Family	Spartan3a
Part	xc3s50an
Package	tqg144
Temp Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.1,06-26-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	8	1408	1
Signals	0.000	20	---	---
IOs	0.008	13	108	12
Leakage	0.013			
Total	0.021			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.9	84.2	25.8

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.002	0.000	0.002
Vccaux	3.300	0.003	0.000	0.003
Vcco25	2.500	0.003	0.003	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.021	0.008	0.013

Figure 11: Power consumption of the DCDL circuit with input from AND gate

The figure below shows the simulation waveform of the DCDL circuit built using a multiplexer.

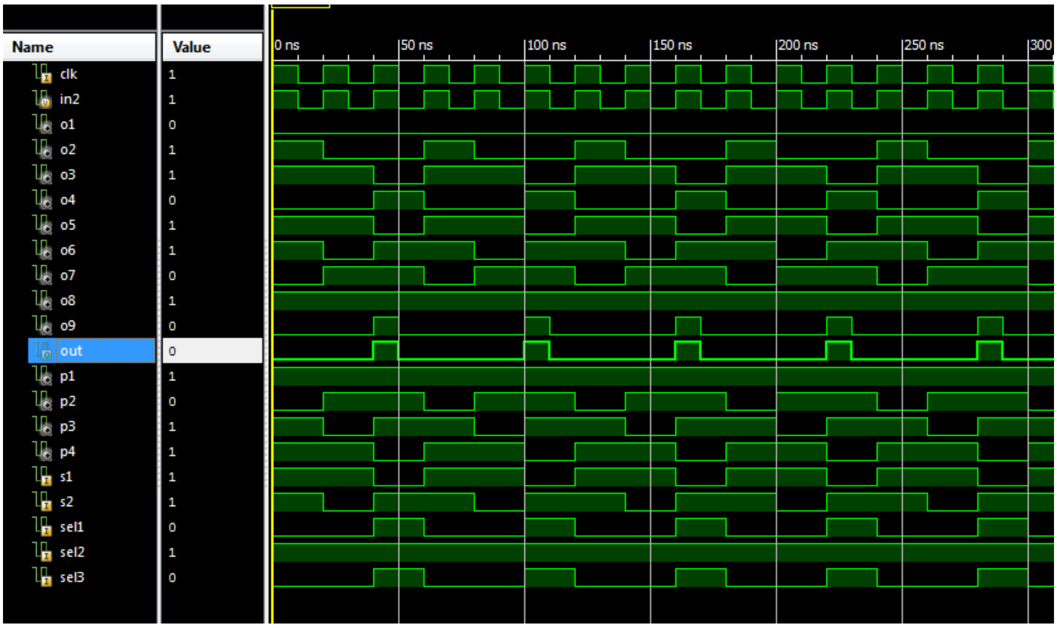


Figure 12: DCDL constructed using multiplexers

In this simulation results 'in' represents the input and 'out' the output of the DCDL. 's1', 's2', 'sel1', 'sel2', 'sel3' represent the select lines of the multiplexers used.

In the above simulation result the signals p1-p4 represent the inputs to the multiplexers and o1-o8 represent the outputs of the multiplexers.

The power consumption of the circuit is as shown in figure 11.

Device	
Family	Spartan3a
Part	xc3s50an
Package	tqg144
Temp Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.1,06-26-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	9	1408	1
Signals	0.000	15	---	---
IOs	0.004	7	108	6
Leakage	0.013			
Total	0.017			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.9	84.3	25.7

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.002	0.000	0.002
Vccaux	3.300	0.003	0.000	0.003
Vcco25	2.500	0.002	0.002	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.017	0.004	0.013

Figure 13: Power consumption of the DCDL circuit built using multiplexers

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III. Conclusion

On observing the power consumption each of the circuits, for the DCDL circuit with glitches (fig 2) has the maximum dynamic power (9mW) this is due to the glitches that are produced in the circuit. To overcome the glitches the DCDL circuit has been modified as shown in figure 3, as seen in the power report of this circuit the dynamic power consumption has reduced to 8mW which shows the reduction in the glitches.

On optimizing the power of the circuit by using an enable signal the power consumption in terms of dynamic power remains same as the all the gates of the circuit work all the time.

On optimizing the power of the circuit using multiplexers, the dynamic power reduces to 4mW as only half the gates in the circuit are active each time.

Reference

[1]. Chen P. L, Chung C. C, and Lee C.Y, “A portable digitally controlled oscillator using novel varactors,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 5, pp. 233–237, May 2011.

[2]. Chen P. L, Chung C. C, Yang J. N, and Lee C. Y., “A clock generator with cascaded dynamic frequency counting loops for wide multiplication range applications,” IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1275–1285, Jun. 2012.

[3]. Choi K. H, Shin J. B, Sim J. Y, and Park H. J, “An interpolating digitally controlled oscillator for a wide range all digital PLL,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 9, pp. 2055–2063, Sep. 2009.

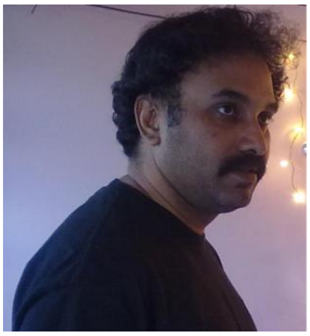
[4]. Matano T. M, Takai Y, Takahashi T, Sakito Y, Fujii I, Takaishi Y, Fujisawa H, Kubouchi S, Narui S, Arai M, Morino K, Nakamura M, Miyatake S, Sekiguchi T, and Koyama K, “A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer,” IEEE J. Solid-State Circuits, vol. 38, no. 5, pp. 762–768, May 2010.

[5]. Moon B. M, Park Y. J, and Jeong D. K, “Monotonic wide-range digitally controlled oscillator compensated for supply voltage variation,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 10, pp. 1036–1040, Oct. 2010.

[6]. Staszewski R.B, Muhammad K, Leipold D, Hung C.-M, Ho Y.-C, Wallberg J. L, Fernando C, Maggio K, Staszewski R, Jung T, Koh J, John S, Deng I.Y, Sarda V, Moreira-Tamayo O,Mayega V, Katz R, Friedman O, Eliezer O.E, de-Obaldia E, and Balsara P.T., “All-digital TX frequencysynthesizer and discrete-time receiver for bluetooth radio in 130-nm CMOS,”IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2278–2291, Dec. 2009.

[7]. Yang R. J and Liu S. I, “A 2.5 GHz all digital delay locked loop in 0.13 mm CMOS technology,” IEEE J. Solid-State Circuits, vol. 42, no. 11, pp. 2338–2347, Nov. 2011.

BIOGRAPHY



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