IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 6, Issue 2, Ver. I (Mar. -Apr. 2016), PP 16-20
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

32 Bit Floating Point Vedic Multiplier

Swapnil Suresh Mohite[1], Sanket Sanjay Nimbalkar[2], Madhav Makarand Bhatkhande[3], Mrs. Rashmi Rahul Kulkarni[4]

[1,2,3](*Department Of Electronics, Finolex Academy Of Management And Technology /Mumbai University, INDIA)*

[4](*Department Of Electronics And Telecommunication, Finolex Academy Of Management And Technology /Mumbai University, INDIA)*

Abstract : *A conventional way of performing multiplication of two 32 bit floating point number can be replaced by using Vedic mathematics. Vedic mathematics is an ancient Indian system of mathematics which has a unique technique of calculation based on sixteen sutras. This 32bit floating point Vedic multiplier which use "urdhwa- triyagbhyam" sutra is analysed to be a more convenient and efficient method because it reduces the processing delay and saves time. We have written the required code in Vhdl Using Xilink Ise Series.*

Keywords: *Carry looks ahead adder, Floating point Multiplier, Single precision, Urdhwa-triyagbhyam, Vedic mathematics*

I. Introduction

A multiplier is one of the key hardware in most digital systems. With advancement in technology many researchers have tried to design multipliers which offers either high speed or less area. Many techniques has been developed to enhance the efficiency of multiplier but principal behind multiplication was same in all the cases.

A Vedic mathematics approach is totally different and consider very close to the way of working of human brain. Vedic mathematics is ancient method of Indian mathematics which has a very unique technique of performing calculations. It is based on the sixteen sutras (formulae). "urdhwa-triyagbhyam" sutra is used for implementation of this 32 bit floating point multiplier.

This work deals with the designing of 32 bit floating point Vedic multiplier (single precision format) using Vedic mathematics sutra. In this project Vedic multiplication method is used for implementation of IEEE754 floating point multiplier with efficient use of carry look ahead adder. Numbers are applied in binary no system, ""urdhwa-triyagbhyam" sutra is used to design mantissa calculation unit while exponent is calculated using carry look ahead adder. IEEE 754 standard consist of the single precision format consisting 32 bit and double precision format consisting 64 bits. The formats consist of three units; sign unit, exponent unit, mantissa unit

II. Floating Point Representation

A. Single precision format: Single precision format represented using 32 bits. Starting 23bits (0to22) are Mantissa bits(M), next 8(23to30) bits are exponent bits(E), 31st bit i.e. MSB is a sign bit(S). It is used to represent numbers in between $2^{-127} to 2^{127}$

S(31)	E(30…….23)	M(22……..0)

B. Double precision format: Single precision format represented using 32 bits. Starting 52bits (0to51) are Mantissa bits(M), next 11(53to62) bits are exponent bits(E), 63rd bit i.e. MSB is a sign bit(S). It is used to represent numbers in between $2^{-1023} to 2^{1023}$.

S(63)	E(62……53)	M(53……..0)

III. Multipliers

A. Need of fast multipliers: Multiplication is one of the most important arithmetic operation. A multiplier is one of the key hardware in most digital processing systems. Speed of any digital system operation depends upon the speed of multiplier. With advancement in technology many researchers have tried to design multipliers which offers high speed.

B. Available multipliers:

1. **Array multiplier:** Array multiplier is well known due to it's regular structure. Multiplier circuit is based on add and shift algorithms. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required when N is the multiplier length.

2. **Booth multiplier:** It is powerful algorithm for signed number multiplication, which treats both positive and negative number uniformly. For the standard add-shift operation each multiplier bit generates one multiple of the multiplicand to be added to partial product. If the multiplier is very large, then a large number of multiplicands have to be added. In this case delay of multiplier is determined by the numbers of addition to be performed. If there is way to reduce number of additions the performance will get better. Booth algorithm is a method that reduce the number of multiplicands multiples uses totally different technique of multiplication. According to previous research papers Vedic multiplier is faster than other conventional multipliers.

C. Vedic mathematics: Vedic mathematics is an ancient Indian technique developed by shankaracharya shri bharti Krishna tirthaji maharaj. The word Vedic is derived from Sanskrit word 'Veda' which means store house of all knowledge[5]. Vedic mathematics is based on sixteen sutras (formulae), out of the sixteen sutra "urdhwa-triyagbhyam" sutra is used for multiplication.

D. Urdhwa-triyagbhyam sutra: sutra "urdhwa-triyagbhyam" sutra is used for multiplication. It is a general formula of multiplication. It is applicable to all the cases of multiplication[5]. Urdhwa means vertical and triyagbhyam means crosswise. Hence it is also called as vertical and crosswise method

IV. Floating Point Multiplication

A. Floating point multiplication algorithm: Floating point multiplication process can be divided in to four units; mantissa calculation unit, exponent calculation unit, sign calculation unit and normaliser unit [5]. Normalised floating point number have the form of $Z = (-1^s) * 2^{(E-bias)} * (1.M)$. To perform multiplication of two single precision floating point numbers following steps are followed:

Step1: Multiplication of significand i.e. (1.M_1*1.M_2).
Step2:Placing the decimal point in the result.
Step3:Addition of the exponent i.e. ($E_{1+}E_2 - bias$).
Step4:Obtaining the sign bit i.e. (S_1 XOR S_2).
Step5:Normalizing the result i.e. obtaining 1 at MSB of the results significand.
Step6: Rounding the result to fit in available bits
Step7: Checking for overflow /under flow

B. Design of 32bit floating point Vedic multiplier:

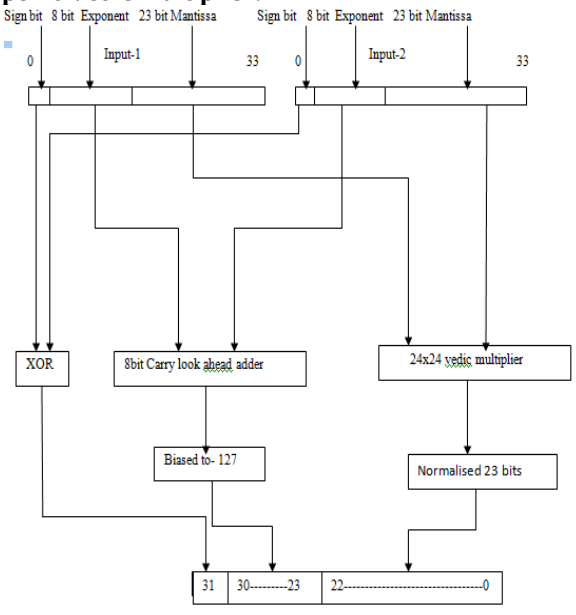


Figure 1: Block diagram of32bit Floating point multiplier

C. Mantissa Multiplication : Overall performance of designed multiplier depends upon the performance of mantissa multiplier unit faster the multiplication unit faster is the overall calculation. Mantissa multiplication unit is designed using Vedic multiplication technique. "Urdhwa-triyagbhyam" sutra is used for multiplication. 3by3 multiplier is used as basic multiplier. Vedic mathematics technique improves the performance of multiplier unit in terms of speed and power.

1. 24by24 Vedic multiplier block: This block is designed using 12by12 Vedic multipliers, 24bit carry look ahead adder & XOR gate.

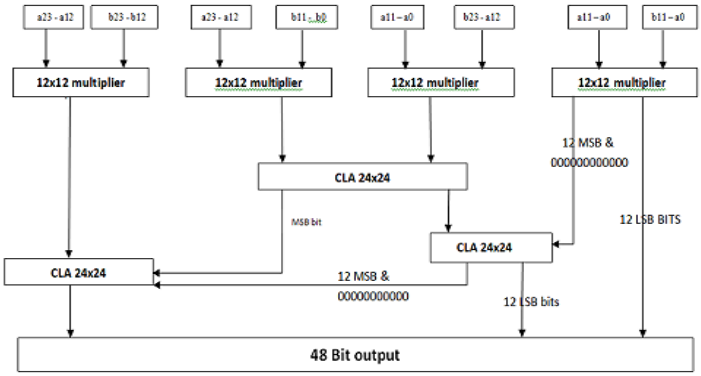


Fig.2.Block diagram of 24by24 multiplier

2. 12by12 Vedic multiplier block: This multiplier block is designed using 6by6 multipliers, 12bit carry look ahead adder & XOR gate.

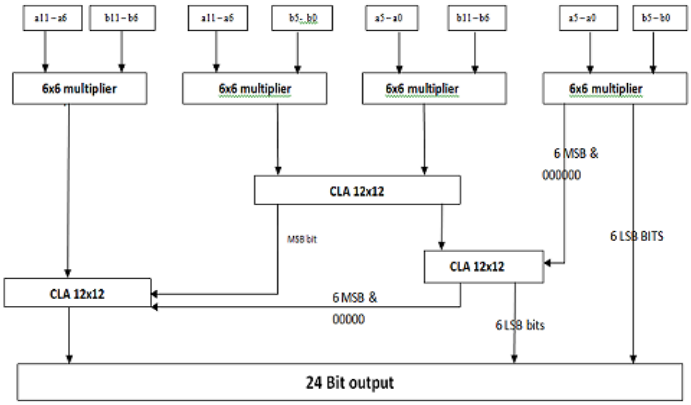


Figure2.Block diagram of 12 by12 multiplier

3. 6by6 Vedic multiplier block: This multiplier block is designed using 3by3 multipliers, 3bit carry look ahead adder & XOR gate.

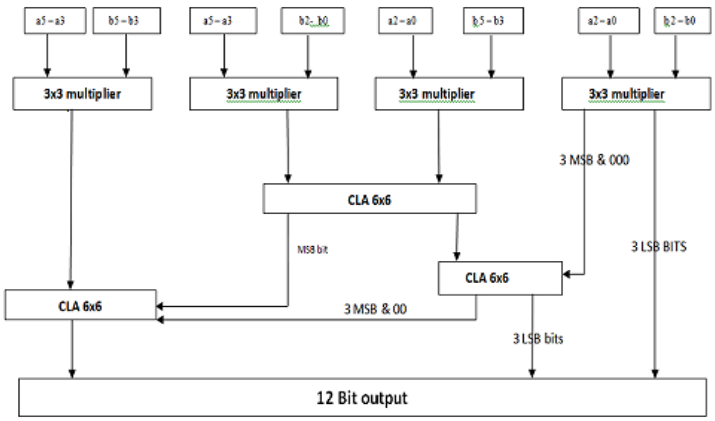


Figure2.Block diagram of 6 by 6 multiplier

D. Exponent Calculation: 8 bit carry look ahead adder is used for adding two 8 bit exponent. Exponent is represented in biased form manually. Output of adder is biased to-127 to generate exponent of output floating point number.

1. **Carry look ahead adder:** A carry look adder is used in digital logic. it reduces time required for determining the carry and hence improves speed . it doesn't wait for generation of carry. It is faster than ripple carry adder.

E. Generation of sign bit: Sign bit of both the input numbers are XORed using XOR gate to generate sign bit of output. '1'repersent negative sign while '0'represent positive sign.

V. Result

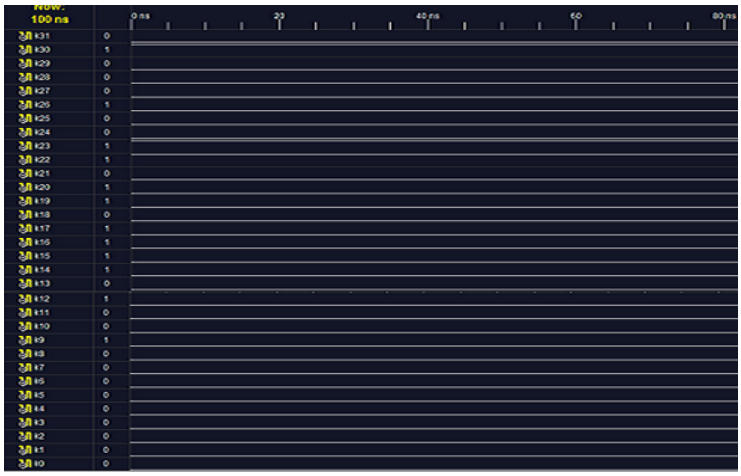
Table1: Performance analysis

Algorithm	Booth[2]	Vedic multiplier using Ripple Carry Adder[2]	Proposed System
Device	VirtexE	VirtexE	VirtexE
Critical path delay	121.737nS	94.770nS	71.293nS
No .of 4 input LUTs	1912	2015	1580
Number of slices	1062	1162	911
No. of bonded IOBs	101	100	96

The waveform shown below can be obtained by giving input to the simulator. Inputs are given in single precision format

1) A=80.5 = 1.0100001x2^6
   A= 0 10000101 01000010000000000000000
2) B= 18.25= 1.001001x2^4
   B= 0 10000011 00100100000000000000000

AxB= 1469.125= 1.0110111101001x2^10
AxB= 0 10001001 10110111101001000000000



VI. Conclusion

This paper presents designing of 32bit floating point vedic multiplier. This particular multiplier is faster than the conventional multipliers. The codes required for designing are coded using VHDL XILINX series. This multiplier performs multiplication operation using urdhwa-triyagbhyam sutra which increases speed of this multiplier.

The purposed multiplier circuit takes 71.239nS to perform multiplication of two 32 bit floating point binary numbers which is significantly less than Booth multiplier. Proposed design is faster than previously designed vedic multipliers using ripple carry adder.

References

Journal Papers:

[1]. Mr.S.S.Mohansundaram,A.Nirmalkumar,T.Arul Prakash "design of floating point multiplier using vedic mathematics" International journal of innovative science, engineering and technology, Vol 2 issue 1,January 2015

[2]. Pankaj Singh, Bhavinkakani "performance comparison of floating point multipliers by using different multiplication algorithm" International journal of electronics and communication, Vol.3 issue1,January 2015.
[3]. Ms. Rashmi Kulkarni ,"Comparison among different adders" ", International Organisation of science and research.Vol 5, Issue 6, 2015.
[4]. Yashkumar.M.Warkari, Prof.L.P.Thakre,Dr.A.Y.Deshmukh"Design of 6 bit vedic multiplier using vedic sutras" International journal of innovative science ,engineering and technology, Vol.3 issue 4,April 2014.
[5]. I.V.Vaibhav,K.V.Saicharan,V.Sravanthi, D. Shinivasulu "VHDL implementation of floating point multiplier using vedic mathematics".
[6]. Sneha Khobragade, Mayur Dhait,"Review of floating point multiplier using vedic mathematics" International journal of science and research.
[7]. Ms. Rashmi Kulkarni, "Parallel hardware implementation of convolution and deconvolution", International Organisation of science and research.Vol 1, Issue 4, 2012.

Books

[8]. Pandit ramanand shastri, "Vedic mathematics", Arihant publications,P.V.
[9]. Gaganpreet Kaur, "VHDL Basics to Programming", Pearson.
[10]. J. Bhasker, "VHDL PRIMER", Pearson Education Asia

Conference

[11]. Rashmi Lomte, Prof. Bhasker P.C. "High Speed Convolution and Deconvolution using udhwa-triyagbhyam" IEEE Computer society annual symposium on VLSI , July2011, IIT Madras

.