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A 2.4-6.0 GHz High Gain LNA for Broadband Applications.

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Abstract: *In this work 0.18 µm CMOS is used to achieve low-characteristics and best performance of in the band of 2.4 GHz to 6.0 GHz. Here simulation tool is used for simulation of lumped components with an inductor less concept. Designed broadband LNA supports multi standard wireless applications with High gain and low noise figure.*

Due to the accurate calculation and the proper impedance matching, the results are the forward gain (S_{21}) is 18dB and Noise figure is less than 2.4dB. Input impedance (S_{11}) and output impedance (S_{22}) also represent good performance. Third order intercept point is -5.25dBm is obtained with the linearity and the performance is good, so that the LNA circuit gives good availability for wireless applications and broadband applications.

Keywords: *LNA, gain, noise figure, s-parameters, dissipated power.*

I. Introduction

Increasing demands of higher data transfer rates and global mobility in current wireless communication environment has led to the development of the Third Generation (3G) mobile communication standard. Nowadays, large operators and small operators, served both developed and emerging market, which give benefits over 3G technologies. Communication system containing transmitter and receiver ,at the receiver end it contain attenuation and also interference. The signal range is in mili-volt range hence hamper the operation of demodulator; so it is require to boost-up the signal and the feeding it to the demodulator. Here amplifier increases the gain but also increase the noise.Therefor the LNA with less noise is required which is at the receiver side.

This paper describes the multi-standard structure of low noise amplifier as a bandwidth extension technique. For a multiple band Receiver, one requirement is to use tuned RF front-ends which is based on broad-band, and also tunable LNAs.

II. Overview On Aroad-Band

Applications

Immersive virtual environments have been moving towards to practical system from research from primarily research. Wireless communications and its application increasing day by day. Basic idea of this development is to give digital signal processing (DSP) in the wireless communication field. Where the CMOS technology give the integrated functionality of DSP, basically current front-end circuits uses mixture of semiconductor technologies, here by using GaAs to SiGe, on single chip the integration of communication system is possible. Recent advancements in CMOS technology, which are Radio Frequency (RF) CMOS Integrated Circuit (IC) it provide on a single chip the potential solution. Design and development of a new reconfigurable LNA architecture is believed to be one of the pioneering attempts in providing new trend of designing LNA for multi-standard multi-band RF receiver system. There is Strong demands for multi-standard multi-band devices with more functionality (i.e. video call, games, email etc.) the compact system design in wireless mobile device is given by RFIC. Nowadays, mobile devices support multiple functions by using several standards.

III. Designing Steps For Broad-Band

Low Noise Amplifier

When the LNA circuit is cascaded to the second stage, the inter stage parasitic reactance attenuated by the desired bandwidth of the low noise amplifier. Now a days, the designed LNAs used the cascode topology which gives lower current and also provide the options to select the band of interest. If it faces some difficulty then in that case, the Broad-band LNAs are choose and designed to cover the maximum number of standards.

However, design based on inductive greatly affects the silicon area which is of a higher fabrication cost. Figure 3 shows the multi standard LNA which is based on broad band. Which contain a resistive feedback stage and next to that a cascode amplifier which a high gain. A resonant load is provided by the active inductor

,which is controlled by a biased varactor device further which select the desired frequency band. Mentioned stages will be described as follows.

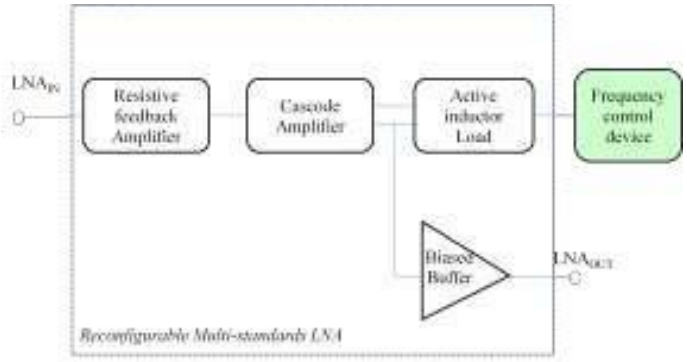

Figure 1: Shows Block diagram of the designed LNA

At the front end of the receiver one of the critical block is LNA. On the performance of the LNA the bandwidth of signal, noise figure, and gain and power consumption of the entire system depends. The proposed LNA consists of following stages.

A. Resistive feedback amplifier stage

One of the optimal topology is the resistive feedback amplifier due to its simplicity, also it has small area and comparative low noise figure than other topologies.

B. Cascode amplifier stage

Stability require good input and good output which is provided by the cascade amplifier which also give the high gain.

C. Active inductor load and Differential LNA

In the active inductor load and differential LNA consists of two transconductors connected which are back-to-back. In which the differential pair implement the first transconductor. On the other hand current mirror amplifier implements the second transconductor.

IV. Schematic View And Schematic Design For Low Noise Amplifier

The LNA circuit, consists of NMOS and PMOS transistors, so that it forms CMOS inverter. Biasing circuitry for LNA is designed by usingactive lumped component. Due to which the equivalent value of transconductance get increased from one level to another level by using dc current. The first part shows Resistive feedback Amplifier which the combination of two NMOS transistors to prevent from buffering in the circuit. Proper impedence matching and high gain is provided by the resistive feedback amplifier. Where as vertical transistor forms second stage i.e cascade amplifier. Also the resistors R_{c1} and R_{c2} are used for active biasing purpose. Active inductor is used at last that is at third stage which is used to supply load to cascade stage. Two transconductor are implemented first with the differential pair and another with current mirror amplifier. Between two transconductors resistance R_1 can be inserted which increase the quality factor of active inductor and for biasing resistance R2 is used.

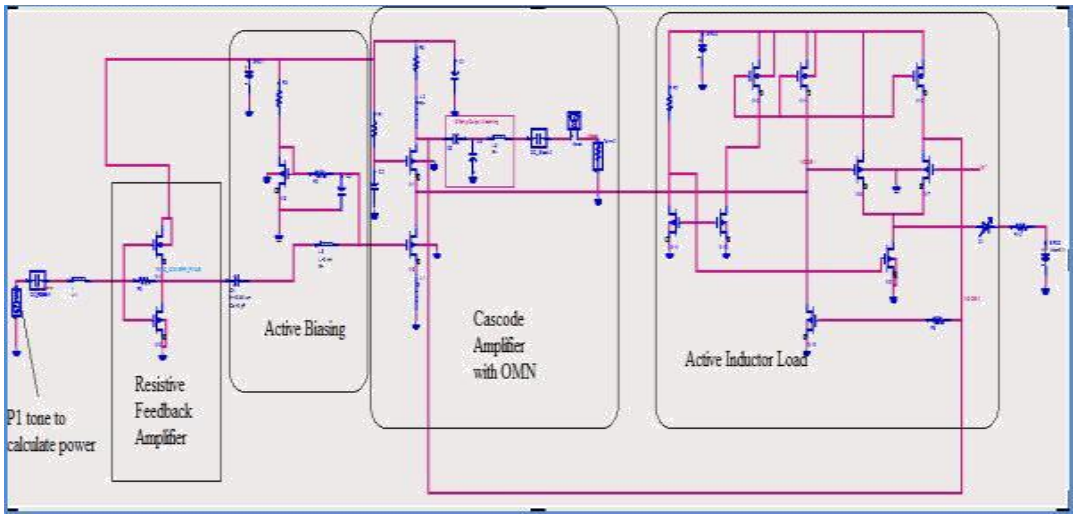

Figure 2: Schematic of Broad-band LNA circuit

V. Schematic Simulation Results For Lna Design: 2.4 Ghz To 6.0 Ghz

The amplifier is presented with high gain,low noise figure, and with input/output return loss in designing of multi-stage cascaded types of LNA. On the basis of simulation results the integrated circuit give the LNA with low power consumption and less number of input/output return losses. By using Agilent's ADS LNA schematic is simulated by using 0.18µm CMOS technology which gives (16-18) dB of gain (S_{21}), less than 2.4dB noise figure (NF).Return losses are also good. As there is tradeoff between low noise figure and return loss; the matching is shown in schematic of LNA. The power dissipation in the whole circuit is 25Mw from the supply of 1.8V.Also 1dB compression Gain for this LNA at Pin of - 13mW is 15dB with Pout of 2mW .While 3dB gain is 13dB at Pin-9.7mW with Pout of 4mW.

This proposed a new methodology for designing LNA for relatively broad-band system to support multi-standard and multi-band with just one single circuit implementation. The forward gain (S_{21}) achieved is (16.72-18.69) dB at the frequency range from (2.4-6.0) GHz as shown in Figure. Better bandwidth with the gain above 10dB is obtained.. The reverse isolation (S_{12}) obtained from the simulation is good which is more than the typical value which is normally -30 dB ;(- 55.8 to - 47.8) dB. The input losses and output losses, S_{11} and S_{22} of LNA are shown in Figure. For S_{11}, the simulations result produced an input return loss of -7 dB at the center frequency of 2.4GHz. For S_{22}, simulation result produced a value of (-6.0 to -10) dB at the frequency range from (2.4-6.0) GHz as shown in Figure. Therefore, by adjusting resistor and capacitor optimization is done. The output return loss achieved, however, is well below -10 dB along the bandwidth. Also noise figure less than2.4dB is obtained.

A two-tone test for the third-order intercept point is used to check the linearity requirement. For which The two tones were applied at frequencies of 2.4 GHz and 6.0 GHz respectively which contain equal power. The achieved IIP3 is -5.25 dBm and is shown in Figure. This achieved value has specification and also fulfill linearity requirements. The less amount of current in circuit is obtain by choosing best IIP3 value. The following table shows comparison with previous work which has been done for the low power LNA which support wireless communications in the frequency band of 2.4 GHz to 6.0 GHz.

Table 1: Circuit Simulation Parameters

LNA parameters	Simulation results	
Frequency Band	2.4 GHz	6.0 GHz
Supply voltage	1.8 V	
S_{11}	-7.0 dB	
S_{12}	-55.8 dB	-47.8dB
S_{21}	16.72 dB	18.69dB
S_{22}	-6.0 dB	-10 dB
Noise figure	< 2.4 dB	
Stability Factor	More than 1.0	
1 dB Gain	15.73 dB	
3 dB Gain	13.75 dB	
Power Dissipation	25 mW	
IIP3	-5.25dBm	

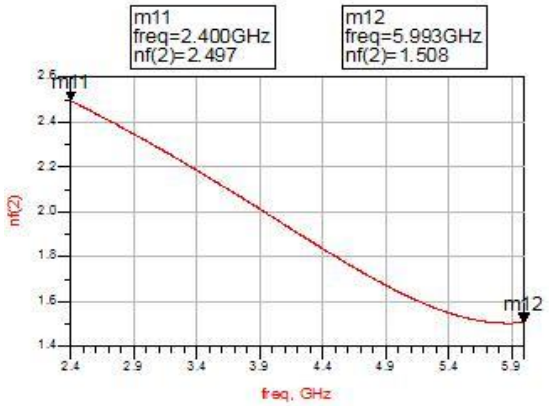

Figure 3: Noise figure of LNA (dB)

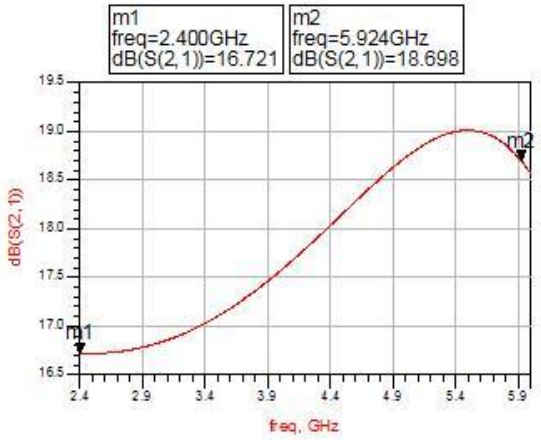

Figure 4: Gain (S_{21}) dB

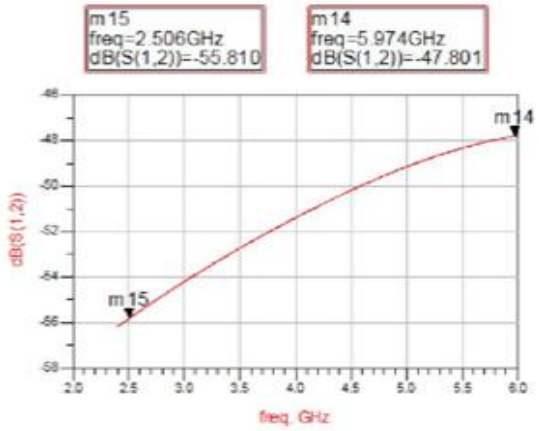

Figure 5: Reverse isolation (S_{12}) dB

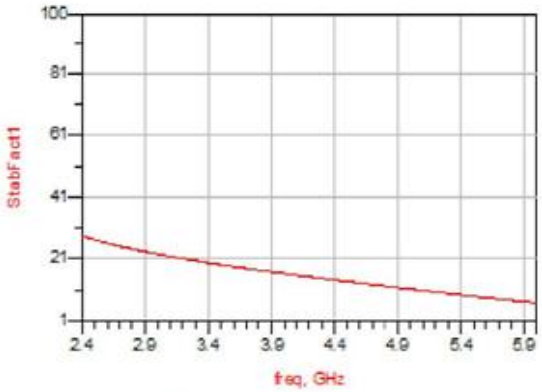

Figure 6: Stability Factor

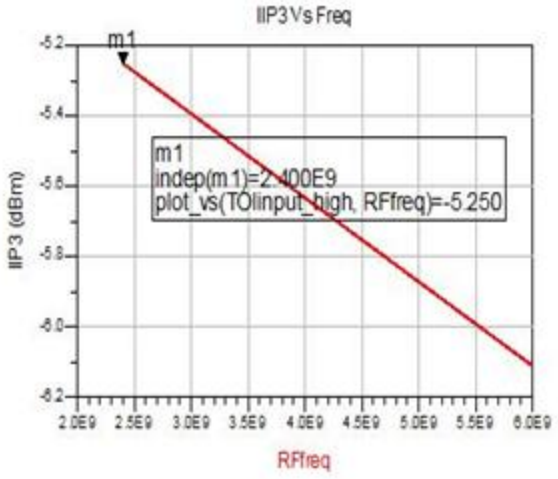

Figure 7: IIP3 (dBm)

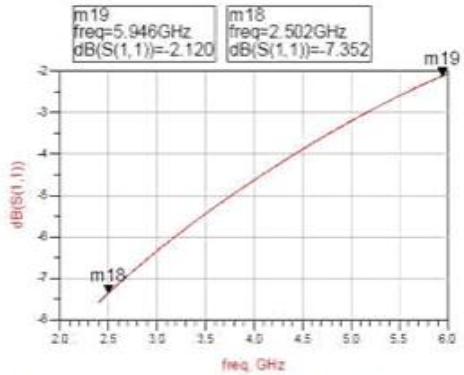

Figure 8: Input reflection coefficients (S_{11}) dB

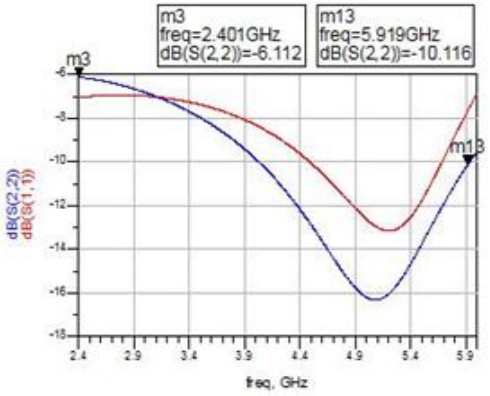

Figure 8: Output reflection coefficients (S_{22}) dB

VI. Conclusion And Disscussion

The amplifier is presented with high gain ,low noise figure, and with input/output return loss in designing of multi-stage cascaded types of LNA. On the basis of simulation results the integrated circuit give the LNA with low power consumption and less number of input/output return losses. By using Agilent's ADS LNA schematic is simulated by using 0.18µm CMOS technology which gives (16-18) dB of gain (S_{21}), less than 2.4dB noise figure (NF). As there is tradeoff between low noise figure and return loss; the matching is shown in schematic of LNA. The power dissipation in the whole circuit is 25Mw from the supply of 1.8V.Also 1dB compression Gain for this LNA at Pin of -13mW is 15dB with Pout of 2mW .While 3dB gain is 13dB at Pin-9.7mW with Pout of 4mW.

In addition, the results achieved are representation of the trade-off made between s-parameters, linearity, and NF and power consumption. However, some of the parameters still need an improvement i.e. Gain. This could be done by improving the circuit power by increasing the current of the circuit. But this action should be taken carefully as not to contradict with the low power design. Therefore, the proposed RF receiver architecture could solve this problem by using a reconfigurable concept. The reconfigurable architecture will have the capability to support multiple standards in one system but with fewer components which results in simpler, more compact, less expensive and less power consumption. Finally, the research carried out in this work has specifically achieved the followings results:

i. The RF receiver system simulation which has been carried out to find the mutual relationship between RF receiver system and RF components specifications provides the minimum and optimum requirement of the LNA's specifications. This will help in developing better RF system.
ii. The development and implementation of Broad band LNAs provides a new approach for designing the multi-standard multi-band LNA for a relatively system especially for mobile communication standards.
iii. The development and implementation of the reconfigurable multi-standard multiband LNA will further provide new methodology in the design of multi-standard LNA for multi-standard system.
iv. This technique which was also employed by the reconfigurable LNA consumes relatively lower power consumption compared to the design which uses buffer circuit for matching purposes.

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