Optimization of Digitally Controlled Oscillator with Low Power

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Abstract: *In this paper, CMOS digitally controlled oscillator (DCO) design is analyzed for 4-16 bits. The CMOS DCO is designed based on a ring oscillator. Simulations of the analyzed DCO using 250nm CMOS technology achieve controllable different frequency range with a wide linearity. A 4-bit digitally controlled CMOS oscillator (DCO) design is best by adjusting the width of p-MOS and n-MOS devices towards low power consumption of 2.2 MW at 1.6GHz with low jitter.*
Keywords: *DCO, Jitter, CMOS , Ring oscillator, Low power , Low Jitter*

I.   Introduction

Ring **DCO, Jitter, CMOS , Ring oscillator, Low power .**oscillator is a device composed of odd number of inverters attached in a chain. The output of last inverter is fed back to the first inverter as shown in Fig1.The circuit will oscillate and for every half period, the signal will propagate around the loop with an inversion. Thus, the change will propagate through all inverters. The frequency of the oscillation is given by

$$F=1/2Nt_d \qquad\qquad (1)$$

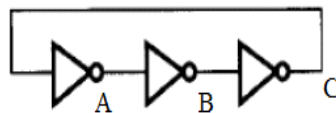N- no. of chains, t_{d-} time delay of each inverter

Fig 1 A ring oscillator realized using three Inverters

They can be used as voltage controlled oscillators in this application as clock recovery circuits [1], for serial data communication [1], on-chip clock distribution [1], in high-speed VLSI systems, clock is practically generated by an analog phase-locked loop. In analog, PLL includes phase frequency detector, a charge pump, a loop filter, voltage controlled Oscillator and a frequency dividers [2, 3]. Voltage controlled oscillator plays an important role in PLL. Nowadays efforts have been made towards the development of digital PLL because of their better noise immunity and dc offset. Digital control oscillator (DCO) is the replacement of VCO in fully digital PLL .In digital PLL frequency gain in current control is not necessary because of its greater immunity towards noise.

The delay of logic gates is computed as the product of RC, where R is the effective driver resistance and C is the load capacitance [4]. Logic gates use minimum –length devices for less delay, area, and power consumption. The delay of a logic gates depends on the transistor width of the gate and the capacitance of the load .So power consumption plays a major role in portable battery based system. [5]

Following sections we analyzed 4-16 bits DCO with binary controlled pass transistors using 250 nm CMOS technology.

II.   CMOS INVERTER

.   CMOS inverter is a circuit which is combination of n-mos transistor and p-mos transistor. Inverter is the basic logic gate in which the output is delivered as a negation of its input. This pair of transistor works as complementary switch without any passive components such as resistors and capacitors.
The principle of operation as follows

*   When the input is high ,pull-up p-mos transistor is switched off and pull down n-mos transistor is switched on and connects the output to GND=0V
*   When the input is low ,pull-up p-mos transistor is switched on and pull down n-mos transistor is switched off and connects the output to VDD
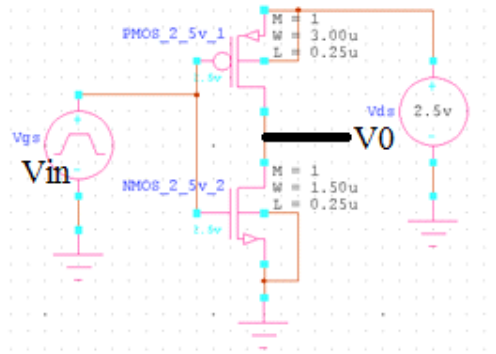
Fig-2 CMOS INVERTER CIRCUIT IN T-SPICE

In the CMOS inverter, the propagation delay is mainly due to parasitic capacitance. (i.e.) the gate and the source or drain, overlapping gate and diffusion region, between the drain of the transistors and the relevant substrate and gate. All such capacitance can be combined to form load capacitance. [5]
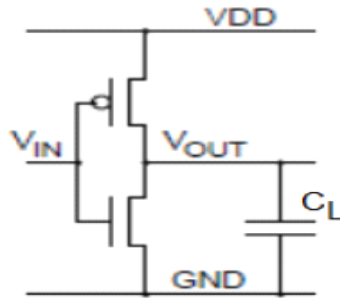

Fig-3 CMOS inverter with equivalent load   capacitance

Effective resistance is the ratio of Vds to Ids average across the switching interval of interest.

A unit n-mos transistor is defined to have effective resistance R. A unit p-mos transistor has greater resistance generally in the range of 2R-3R, because of its lower mobility. For simple analyzing purpose, we have considered a single-ended CMOS ring oscillator with equal-length n-MOS and p-MOS transistors. Assuming that Vtn=|Vtp|, the maximum total channel noise from n-MOS and p-MOS devices, when both the input and output are at Vdd/2 , is given by

$$\overline{I_n^2}/\Delta f = 4KT\gamma\,\mu_{eff}\,C_{ox}(W_{eff}/L)\,\Delta V \quad (2)$$

Where

$$W_{eff} = W_n + W_p$$

$$\mu_{eff} = (\mu_n W_n + \mu_p W_p)/(W_n + W_p)$$

And ΔV is the gate overdrive in the middle of transition, $\Delta V = (Vdd/2) - Vt$

Assuming $\mu_n W_n + \mu_p W_p$ to make the waveforms symmetric to the first order, the oscillation frequency for a load capacitance $C_L = 9.7f$ F is approximately given by

$$f_o = 1/2N\tau_p = 1/\eta N(t_r + t_f) = \mu_{eff}\,C_{ox}\,W_{eff}/(8\eta N L\,q_{max})\Delta V^2$$

(3)
Where

τ_p = propagation delay, t_r and t_f are the rise and   fall time respectively, associated with the maximum slope during a transition.

III. WORKING PRINCIPLE OF DCO AND DESIGN

Typical Digital controlled oscillator with enable input is shown in fig 5. The enable circuit provides a way to control the operation of the ring oscillator. When the user provides logic one on the enable pin, the ring oscillator operates and generates sustained oscillations. When the enable circuit input is logic zero, no oscillations are generated by the ring oscillator. Internal structure of inverter gate is shown in fig 6. D (0) to D (n-1) bits is called as digital control inputs which are applied through binary controlled pass transistor logic. If binary I/p for any particular gate is '0' then corresponding transistor will conduct, delay will be reduced, or reversely binary input is '1', reverse action will be there. Depends up on the position of control inputs, delay and generated oscillation frequency will be varied.
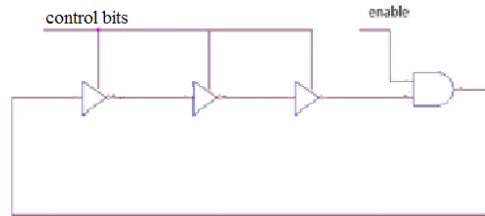
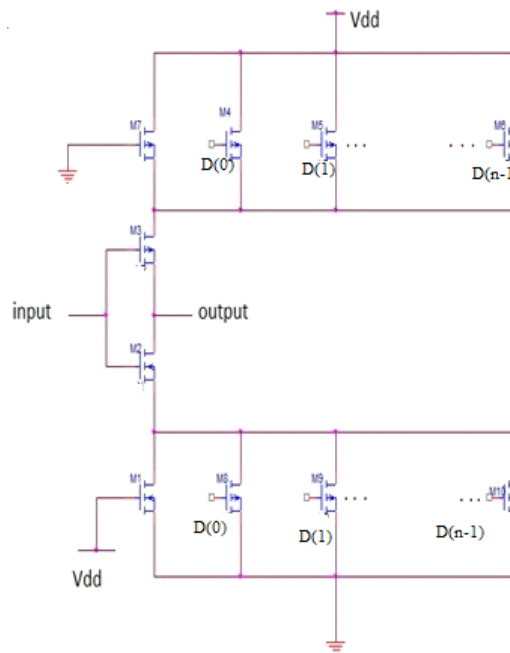Fig 5 Typical Digital controlled Oscillator with enable input

Fig 6 Internal structure of inverter gate

DCO should generate an oscillation period of T_{DCO}, which is the function of digital input word D and given by

$$T_{DCO} = f\,(d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + d_{n-3}2^{n-3} + d_{n-4}2^{n-4}\ldots\ldots + d_0 2^0) \qquad (4)$$

Where f = switching frequency, d = control bits

Typically DCO transfer function is defined by the period of oscillation $T_{DCO\ which}$ is linearly proportional to the Digital input control word D with an offset. Therefore oscillation period is evaluated as follows

$$T_{DCO} = T_{offset} + D.T_{step}. \qquad (5)$$

D- Digital control bits

Where T_{offset} is the constant offset period, T_{step} is the period of quantization step. For the conventional driving strength-controlled DCO shown in Figure 4 the constant delay of each cell is calculated as follows:

$$Tconstant = R1\,(C + C') + R2C', \qquad (6)$$

$$R1, 2\ \alpha\ 1/W1, 2,$$

where R1 and R 2are the equivalent resistances of   M and M' and C and C' are the total capacitances at the drain of M and *M '*, respectively, which mainly consist of drain to body and source to body capacitances.
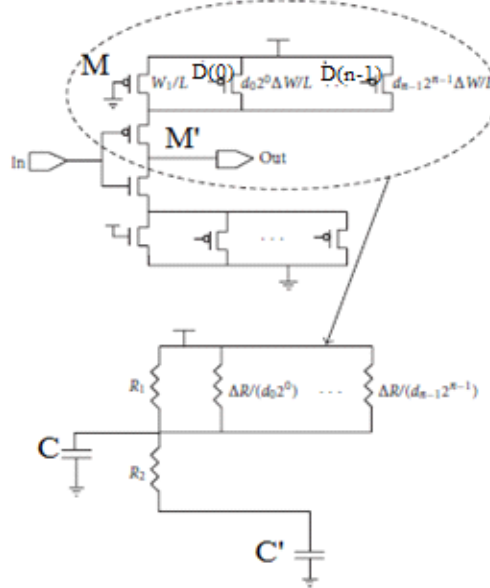

Fig 4 Digital Controlled Oscillator and its Equivalent circuit to calculate constant delay and delay tuning range.

In order to have good tuning range the width of PMOS transistor has to be increased .Consequently R1 will decrease resulting in smaller delay tuning range. [4].

IV.   RESULTS AND DISCUSSION

Results are analyzed in 250nm CMOS technology using TSPICE. Initially the width of PMOS and NMOS is set as 1µ and 0.5µ respectively   For 16 bit digital control inputs , 5 inverter chains , V_{dd}=2.5v, we obtained the following results.

Table 1-Impact of delay for 16 bit digital control inputs

Control bits	Total Delay (ns)
00000000	1.284
00000001	1.282
00000010	1.281
11111111	1.258
Operating range= 778MHz to 794MHz	

Next for the same width size, delay is analyzed for 8 bits control digital inputs with 5 inverter chains, V_{dd} =2.5v .Following results are obtained.

Table 2- Impact of delay for 8 bit digital control inputs

Control bits	Delay for each cell (ps)
0000	90
0100	97
0010	115
1111	128
Operating frequency range = 0.8GHz to 1.09GHz	

Table -3-Characterization of DCO structure

Items	Coarse delay	Fine delay
Resolution	4 bit	4 bit
Max DCO gain	13 ps	0.5ps
Avg DCO gain	9ps	0.3ps
Operating range	1.6GHz to 1.8 GHz	
Power consumption	2.3mW at 1.6 GHz	

Next for the same width size, delay is analyzed for 4 bits control digital inputs with 5 inverter chains. Results are obtained as follows:

Table -4- Impact of delay for 4 bit digital control inputs

Control bits	Delay for each cell (ps)
00	90
01	97
10	115
11	128
Operating range = 1.6GHz to 2.0GHz.	
Power consumption= 2.2mW at 1.6GHz.	

Next width of PMOS and NMOS is adjusted to 3μ and 1.5μ respectively, 4 bits digital control inputs, 3 inverter chains are connected. Results are obtained as follows

Table – 5 - Impact of delay for 2 bit digital control inputs by doubling the width size

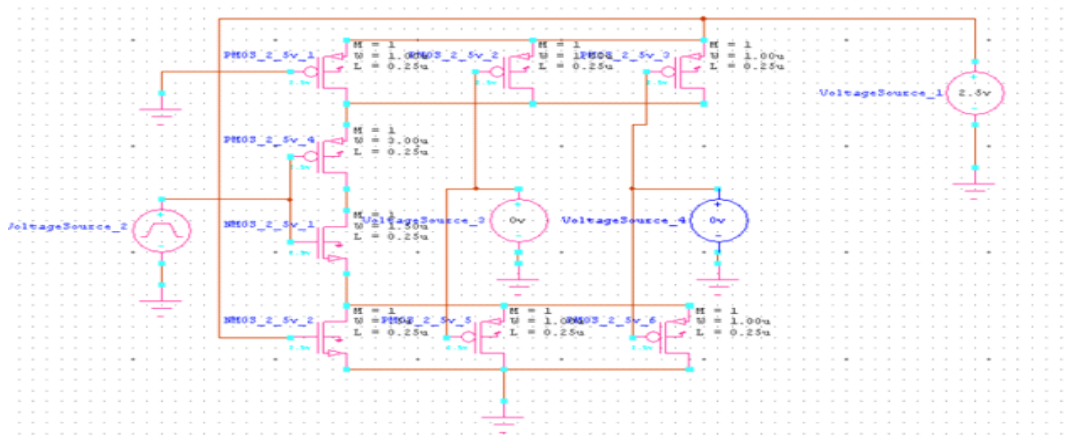| Control bits	Delay for each cell (ps)
00	80
01	82
10	84
11	88
Operating range = 1.6GHz to 2.0GHz.	
Power consumption= 2.2mW at 1.6GHz.	

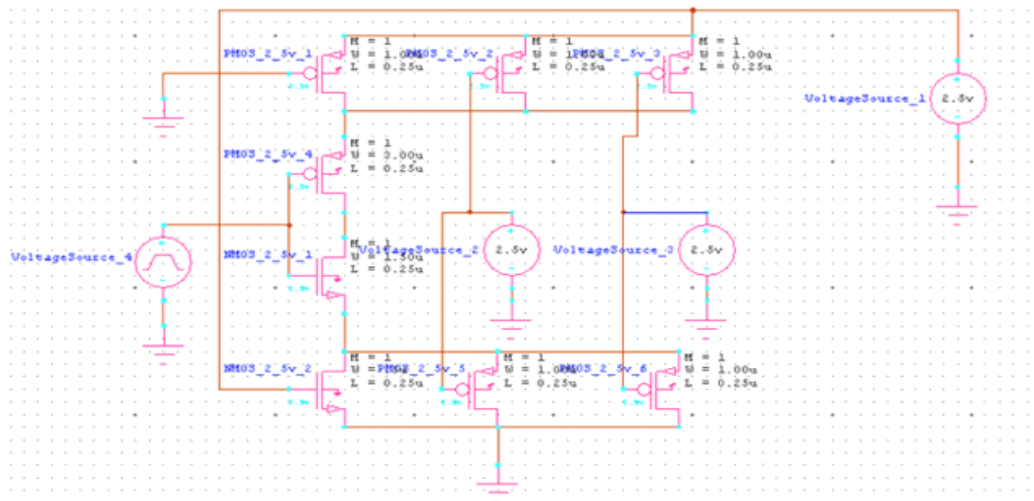**Fig 5 control bit 00-width of p-mos is 1μ and n-mos is 0.5μ**

Fig 6 control bit 11- width of p-mos is 1μ and n-mos is 0.5μ

Dynamic power consumption is given by

$$P = C_L V_{dd}^2 f \text{ watts.} \qquad (7)$$

Where C_L = load capacitance

V_{dd} = supply voltage

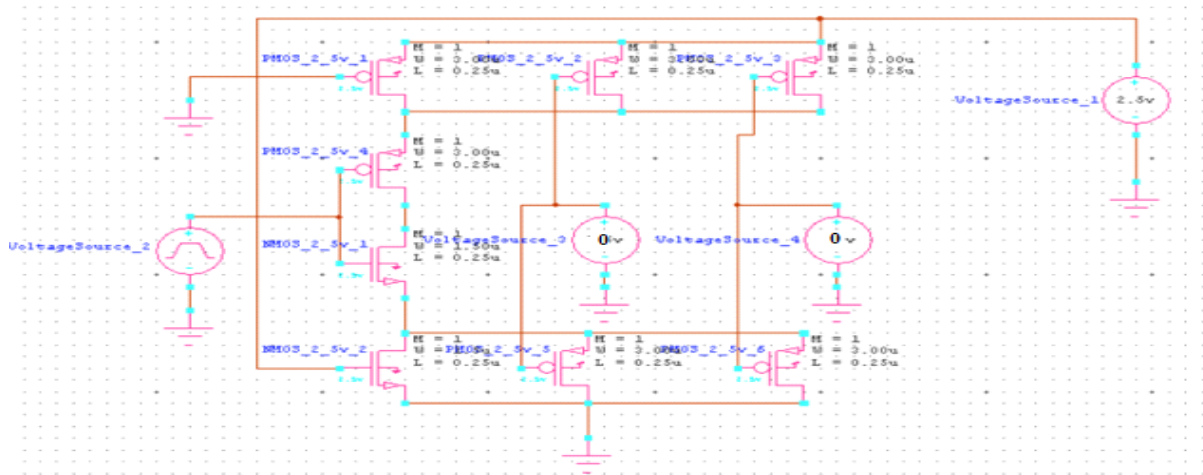f = frequency of switching

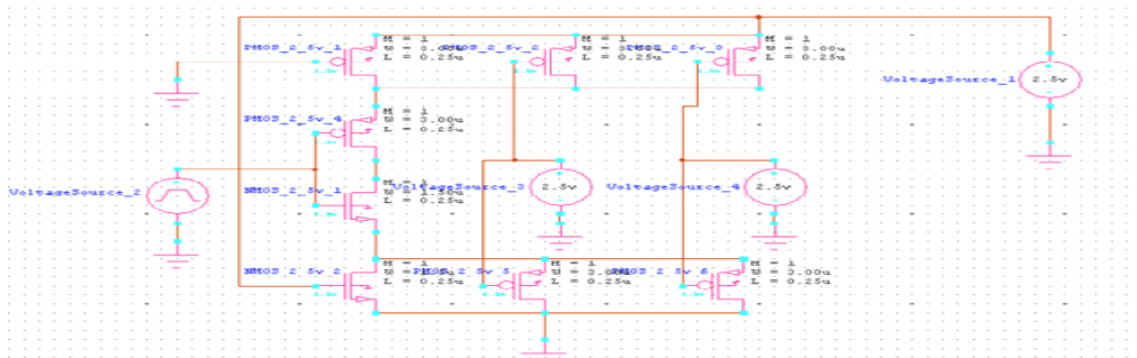**Fig 7 control bit 00-width of p-mos is 3μ and n-mos is 1.5μ**

Fig 8 control bit 11- width of p-mos is 3μ and n-mos is 1.5μ

In [4] power was estimated as 2.3mW at 850 MHz with 12 bit control inputs. But in our work, power was estimated as 2.3mW at 1.6GHz with 8 bit digital control inputs. By the way of reducing activity through reducing digital control inputs, power is reduced. By adjusting the width as 3μ and 1.5μ for PMOS and NMOS respectively, 4 bits digital control inputs, delays are very much reduced. Power consumption is also reduced through reducing switching activity as 2.2mW at 1.6GHz

V. CONCLUSION

Thus CMOS digitally controlled oscillator was designed and analyzed for 4-16 bits ,where 4-bits DCO with width of 3μ and 1.5μ for PMOS and NMOS is good robustness to process, voltage, and temperature variations and also low power consumption with low switching activity. The performance, flexibility, and robustness make the proposed DCO viable for high performance fully digital PLL application

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