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Multi-level CMOS LDO-Voltage Circuit with Differential Current Circuit Steering and Regulated Voltage

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Abstract:*The basic purposes of an Amplifier are to do just that, to amplify (a signal). However, the way different types of amplifiers do this can vary greatly, and an amplifier can do other tasks besides amplifying. Generally when we speak of amplifiers we mean increase the power of a signal. We are starting to get into the building blocks that make up part of a radio system. Signals that we actually amplify in radio and communications are very often not sine waves, though many times they are. For our discussion we will consider that we are amplifying a sine wave(s) of alternating voltage or current. In this paper the purpose is on setting up a CMOS LDO (Low Dropout) voltage circuit which can deliver a significant drop and a regulated voltage at multi-level ports so as to enable a SoC or a NoC to have only one power supply along with a single power distribution circuit or a network.*

Keywords:*CMOS, Low dropout, NoC, SoC, Voltage Regulator*

I. Introduction

CMOS (complementary metal-oxide semiconductor) is the semiconductor technology used in the transistors that are manufactured into most of today's computer microchips. Semiconductors are made of silicon and germanium, materials which "sort of" conduct electricity, but not enthusiastically. Areas of these materials that are "doped" by adding impurities become full-scale conductors of either extra electrons with a negative charge (N-type transistors) or of positive charge carriers (P-type transistors). In CMOS technology, both kinds of transistors are used in a complementary way to form a current gate that forms an effective means of electrical control. CMOS transistors use almost no power when not needed. As the current direction changes more rapidly, however, the transistors become hot. This characteristic tends to limit the speed at which microprocessors can operate. Low dropout voltage regulators often require a large off chip external output capacitor for stability and improved transient-response, which cannot be integrated on the SoC. Capacitor-free LDOs completely eliminate the off-chip capacitor [1].

With the rapid development of system-on-chip designs, there is a growing trend toward power-management integration. On-chip and local LDOs are utilized to power up sunblock's of a system individually, and this can significantly reduce crosstalk, improve the voltage regulation and eliminate load transient voltage spikes from bond wire inductances. In addition, system-on-chip designs with on-chip and local LDOs can reduce both board space and external pins significantly.

Low dropout regulators (LDOs) are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. They are easy to design with and use. For most applications, the parameters in an LDO datasheet are usually very clear and easy to understand. However, other applications require the designer to examine the datasheet more closely to determine whether or not the LDO is suitable for the specific circuit conditions. Unfortunately, datasheets can't provide all parameters under all possible operating conditions. To the designer must interpret and extrapolate the available information to determine the performance under non-specified conditions. For standard regulators, the pass element is either a Darlington NPN or PNP output stage. Fig. 1 shows that a Darlington transistor has a high collector-to-emitter voltage drop because the gate drive voltage encounters two base-to-emitter drops before reaching the output. Standard linear regulators have voltage drops as high as 2 V which are acceptable for applications with large input-to-output voltage difference such as generating 2.5 V from a 5 V input.

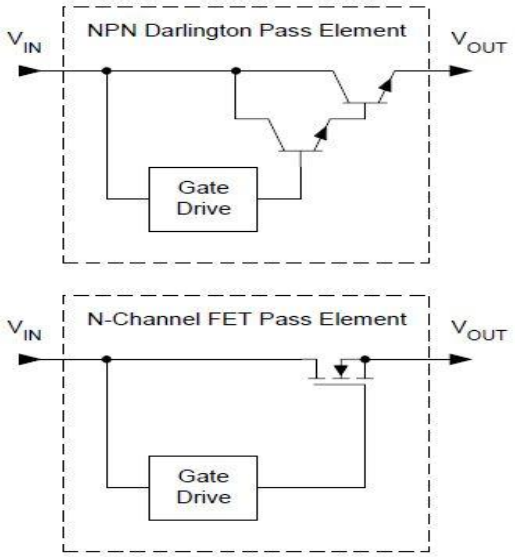

Fig. 1. LDO Pass Element [2]

A. General Architecture of LDO

As a given specification value of CLis 1uF and for maximum capacity current (200mA) size of pass transistor is large so result of which gate capacitor of pass transistor is also large in the range of few hundred of pF. This value of gate capacitor of pass transistor is large compare to the output capacitor of error amplifier.

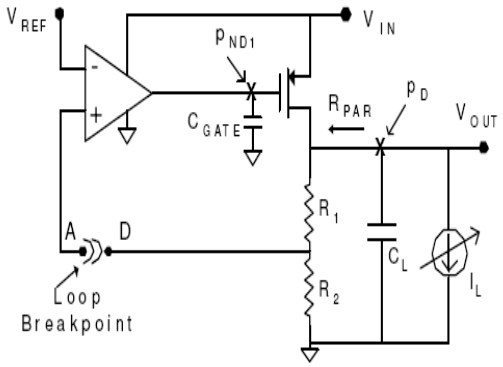

Fig. 2. Typical LDO Open Loop Representations

The output impedance (R_{PAR}) follows variations in load because both R_L and r_{DS} are functions of the load current.

II. LDO Performance Metric Definitions

LDO use a specific set of performance metrics to characterize their performance. In this section each metric is explained individually. All the measurements obtained in this work follow these performance metrics.

A. AC Performance

The AC performance is mainly characterized by the phase margin test. It is essential, like in most systems, that the open loop phase margin stay above 45º throughout the complete current load range.

B. Dropout Voltage

The dropout voltage is the minimum voltage drop across the input and output terminals of the LDO with which the system is able to adjust.

C. Transient Response

In real world operation the LDO operates in closed loop with the input at the source end of the pass transistor, and one output at the drain of the pass transistor. Full-load transient settling time, deflection voltage,

maximum over/undershoot and startup time are all features extracted from an LDO's response to stepped output loads. Fig. 4 shows the definition of each of these transient parameters except for startup time.
The deflection voltage is defined as the difference between the steady state final values for V_{OUT} of high and low current load cycles. The maximum over and undershoots are shown in Fig. 4 to be the maximum peak of the output waveform during the load transition phase [3], [4].

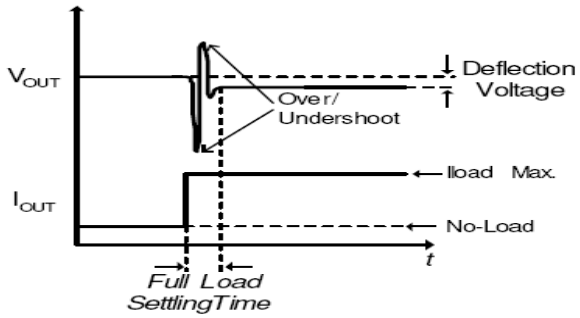

Fig. 3. Transient Response Characteristics.

D. Load Regulation

Load regulation is the ability of the regulator to sustain the desired output voltage with any changes in load current.

E. Line Regulation

Line regulation is the ability of the circuit to sustain the specified output voltage without any effects from variations in input voltage.

F. PSRR

Power supply rejection ratio (PSRR), also known as ripple rejection, is the measure of the circuit's ability to maintain a regulated output voltage nevertheless of input voltage variations.

III. Methodology

A. LDO with Current sampling Differential Amplifier:

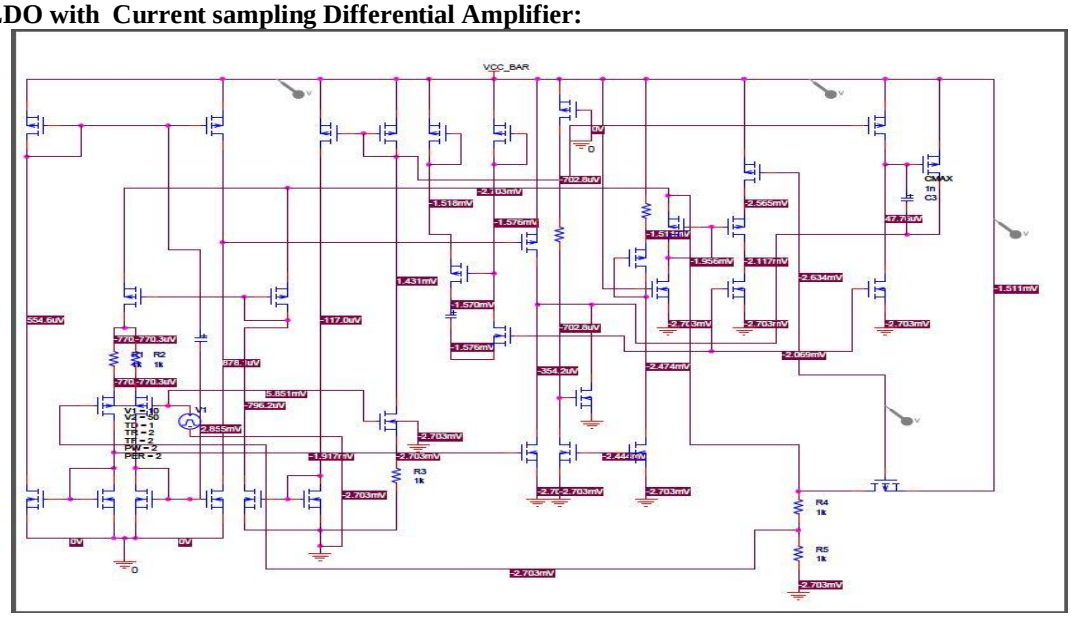

Fig. 4.Reference circuit LDO with Current sampling Differential Amplifier

Circuit implementation: In the designed circuit we have used several networks to obtain the low dropout regulated voltage. However the use of low dropout voltage can be understand in the context of digital circuits where the required input voltage for many digital components is less than 5V. It may drop down to the order of mV. To drop down the received voltage from the main power supply up to a certain extent to make it appropriate for the digital circuits.

Firstly it has the start-up circuit which initiates the differential circuit current generator to operate at the received high input voltage.

Differential circuit current generator is an amplifier whose differential input voltage produces an output current and a low and optimized voltage. Thus, it is a voltage controlled current source (VCCS), it is somewhat similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

Dynamic frequency driver is a technique used in amplifiers, to avoid the unintentional creation of positive feedback, which will cause the amplifier to oscillate, and to control overshoot and ringing in the amplifier's step response.

Along with these two important networks current steering, current sampling and pass feedback element circuits are used to generate the regulated low dropout voltage

B. Design of The Proposed LDO:

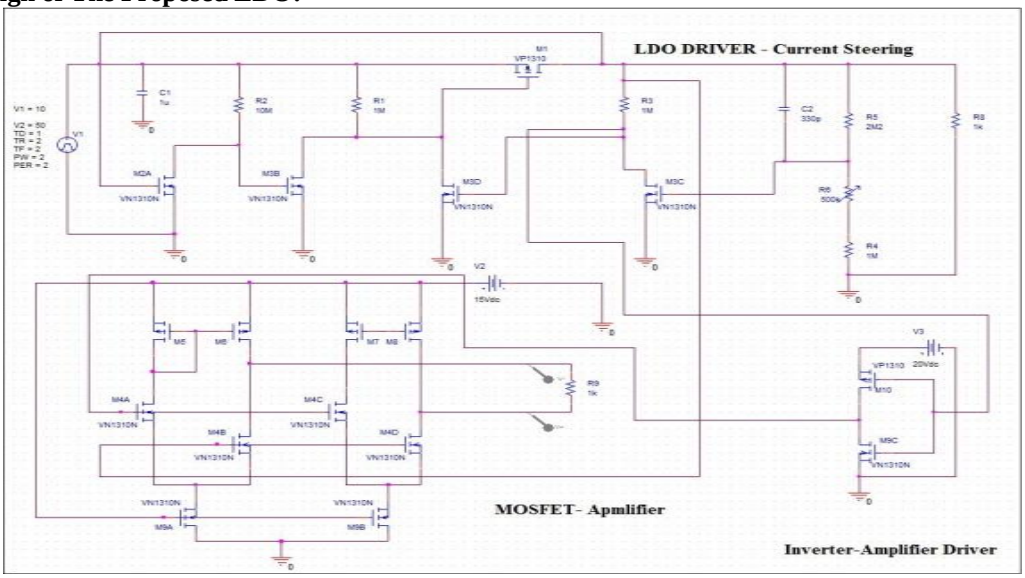

Fig. 5. Schematic diagram of the proposed LDO linear voltage regulator with NMOS driven amplifier

Circuit implementation: The proposed LDO linear voltage regulator is the modification of the LDO with Current sampling Differential Amplifier. A complex LDO circuit is first designed to lower down the voltage, using the current steering and the current sampling circuit in combination of the voltage driver network which reduces the voltage level of the whole circuit however at different circuit levels or at different junctions of the circuit multiple voltage levels can be obtained which can utilized by the parent circuit if required, to regulate the voltage level at 1.5V, a NMOS driven CMOS amplifier has been designed in order to obtain the regulated and a stable result, its response time is approximately 18ns and it can be operated up to 100V, as the test results show. However the possibility of its range for handling the voltage level above 100V cannot be ruled out completely.

IV. Simulated And Experimental Results

The proposed voltage regulator was designed and simulated in CMOS process with the help Cadence tools.

A. Results of LDO with Current sampling Differential Amplifier:

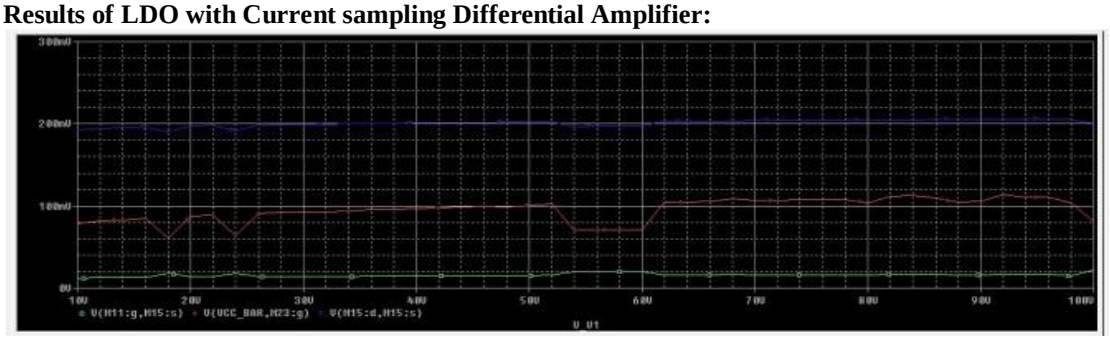

Fig. 6.Simulated output voltage at multi-level

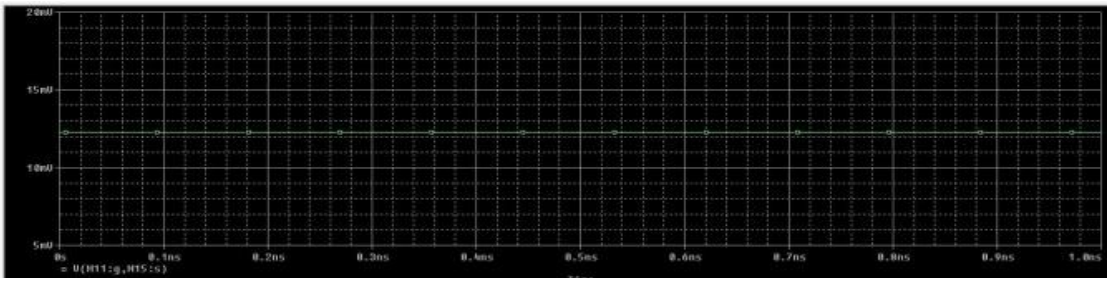

Fig. 7.Simulated Response time

B. Results of LDO with NMOS driven amplifier:

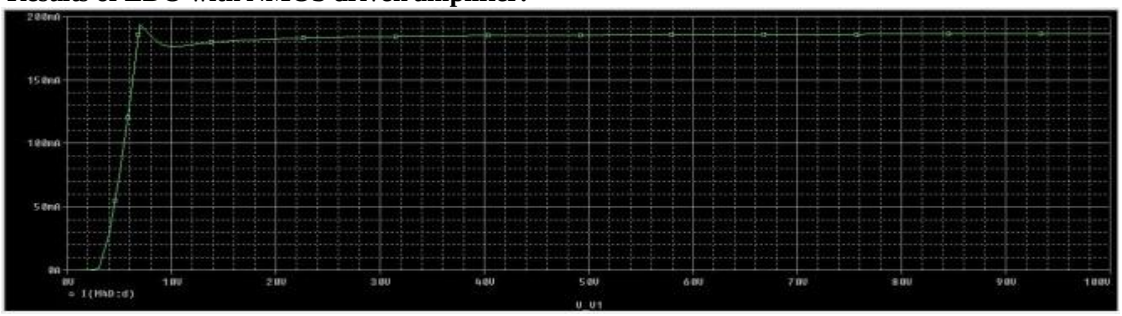

Fig. 8.Simulated output Current Current_M4D

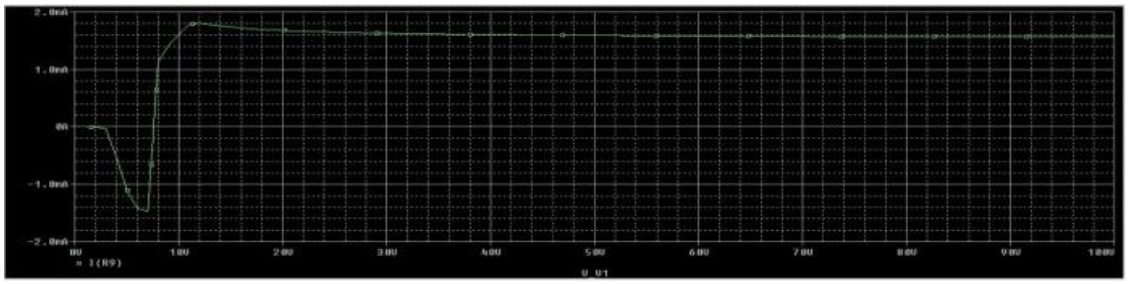

Fig. 9.Simulated output Current Current_R9

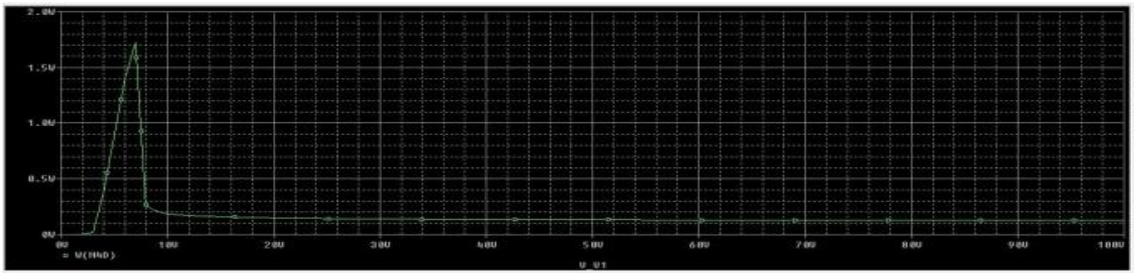

Fig. 10.Simulated output Power_M4D

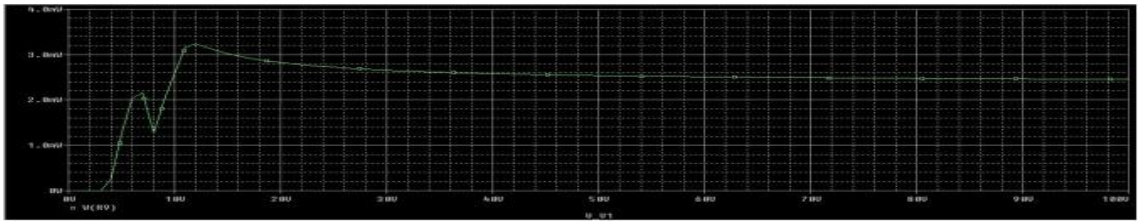

Fig. 11.Simulated output Power_R9

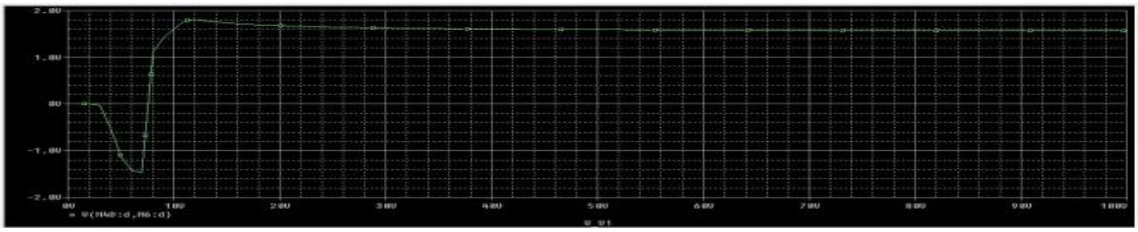

Fig. 12.Simulated output Voltage_M4D

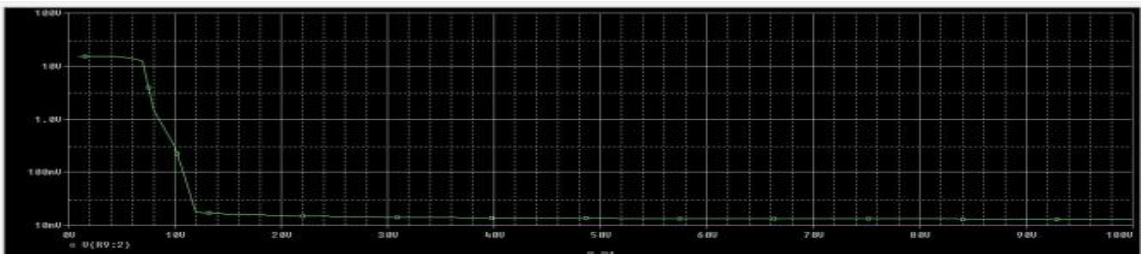

Fig. 13.Simulated output Voltage_R9

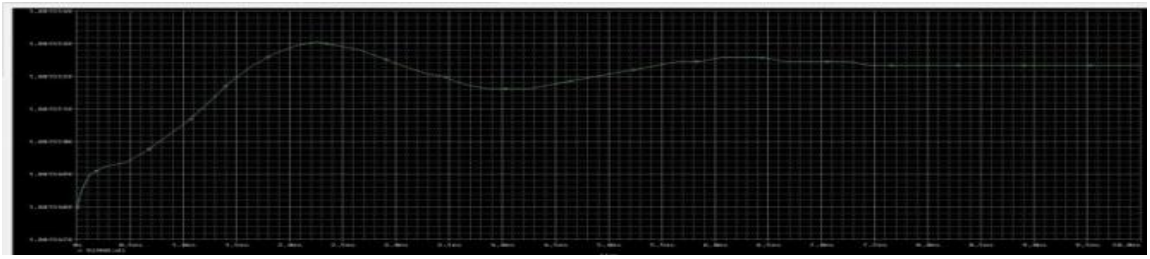

Fig. 14.Simulated Response time (7.45ns)

Table No.1 Measured performance summary of the Proposed LDO

Input voltage range	10-100V
Regulated output voltage VOUT	12mV-5V(at multiple ports)
Dropout Voltage	0.152 V
Bandwidth_Bandpass_3dB:	4.92685
Cutoff_Highpass_3dB:	8.57016
Cutoff_Lowpass_3dB:	7.13096
Gain	68DB
Min(V(Vout))	12.74487mV
Max(V(Vout))	15V
Simulated Response time	7.45ns

V. Conclusión

An improved LDO linear voltage regulator is presented in this paper. LDOs are very important for the digital circuits, as these circuits are designed to work on very low power and are not supposed to expose to a high voltage power supply, here LDOs plays an important role. In this paper two methodologies have been presented, first method suggests an idea of supplying the voltage to a digital circuit of the order of mV which is going to be very essential with the next generation of digital circuits and digital ICs which are scalable up to 14nm.

However the second method generates the voltage of the order of mV, V and a slightly higher range voltage of approximately 20V which make it more flexible when it comes to connect multiple digital circuits and they are supposed to work independently, however data communication may play a vital role in their functioning, to facilitates power supply to such SoCs and NoCs this LDO design will prove to be of great utility. Additionally, the circuit is able to produce higher gain than the reference circuit. The design also succeeds low space as the resistors and capacitor are avoided.

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