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An Inductor-Less Broadband Low Noise Amplifier Using Switched Capacitor with Composite Transistor Pair in 90 nm CMOS Technology

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Abstract: *Low-Noise Amplifier (LNA), with a broadband circuit appears attractive because of the reduced cost realized by area reduction due to replacing of resistor with switch capacitor. The demand for a low-cost but high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuit has been carried out. The goal is to minimize the cost and enhance the performance, low power consumption design. To design a Low Noise Amplifier one of the method which we have used is an inductor-less noise cancelling broadband using switch capacitor with composite transistor pair. The composite pair of NMOS/PMOS cross coupled transistor is used to amplify the input signal while reducing noise figure. It reduces the noise figure by partially cancelling noise which is generated by the input transistor pair. In this technique it does not rely on the matching between the devices which makes this architecture more beneficial to implement practically. Circuit implementation was done in cadence tools using gpdk90nm CMOS technology.*

Keywords: *Composite transistor pair, Switched Capacitor, low noise amplifier, noise cancellation, broadband.*

I. Introduction

The modern wireless industry is now motivated by the global trend of developing multi-band/multi-standard terminals for low-cost and multifunction transceivers [1–3]. Broadband front-end faces many challenging problem including very low noise figure, high linearity requirements, and low area consumption. Upcoming software-defined and multi-standard radio architectures demand broadband LNAs [1]. In contrast to a multi-LNA solution, a broadband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip balun with low losses are typically narrowband so that several balun would be required in case of broadband operation. On the other hand, broadband passive balun typically have high loss, degrading the overall NF of a receiver significantly. Combining the balun and LNA functionality into a single integrated circuit is an attractive option to realize a broadband low noise receiver front-end. Broadband low-noise amplifiers (LNAs) are key building blocks in broadband front-ends. Inductor-less topology has been proposed to reduce the area consumption [4–12]. These LNAs usually rely on resistive feedback techniques for broadband input matching, which leads to poor noise figure, and hence, poor sensitivity. Broadband LNAs find application in communication system and instrumentation equipment. A low noise amplifier is the first component in any RF part. There are 3 purposes of the LNA. First, is to provide the isolation between the local oscillator or mixer stages and the antenna. The isolation is very much needed because the mixer is not totally unilateral, therefore some oscillator signal can be allowed to go through the antenna from the mixer

Second, is to improve the image frequency rejection and lastly to provide some selectivity. By using the LNA, we can increase the gain and thus better sensitivity. The LNA can also improve noise characteristics. Putting an LNA in the line between the mixer and the antenna limits the signal that is radiated to the atmosphere via the antenna

II. System Implementation

This architecture is similar to the conventional broadband LNA with resistive matching, however, the overall noise figure is reduced by incorporating the transistor M_p and connecting the gate of M_p to the gate of M_n in a cross-coupled fashion. The composite configuration of the NMOS and PMOS transistors reduces the output noise of the two transistors and results in a lower output noise. The NMOS and PMOS transistors appear in series, and the inputs are assumed to be V_1 and . Ideally, if the two inputs have the same amplitude and phase, then the source voltage of the two transistors, , is the same as the input leading to a zero output current. On the

other hand, if the two inputs have the same amplitude but differ in phase then V_s, is an AC ground resulting in a finite output current. Hence, this configuration amplifies the differential voltage and rejects the common-mode one.

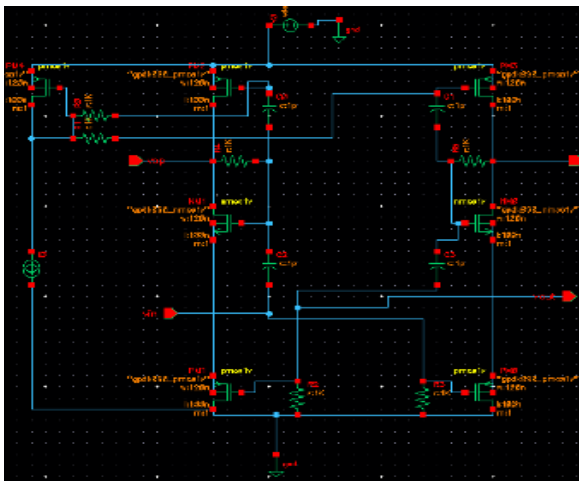

Fig 1.Broadband LNA with resistive feedback

III. Switched Capacitor

A switched capacitor is an electronic circuit used for discrete time signal processing. C_1 gets fully charged when switch S1 is closed and S2 is open and discharged through S2 when S1 is open and S2 is closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously. This makes them much more suitable for use within integrated circuit. The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S1 and S2 which connect the capacitor with a given frequency alternately to the input and output of the SC. The primary advantage of switched capacitor filters is that they can be easily implemented on an integrated circuit. You can get performance similar to an analog RC op-amp based filter using a switched capacitor topology, while avoiding the need for an ADC, DSP, and DAC on a chip. Switched capacitor circuits use capacitors and switches to emulate the behavior of resistors. Additionally, the frequency response is determined by the ratio of the capacitors, so even low frequency filters can be easily realized on-chip. The real benefit for IC implementations is that while the absolute value of capacitances and resistances have a poor tolerance, the matching between similar devices is very good. This makes it possible to implement relatively high precision analog filters on a chip.

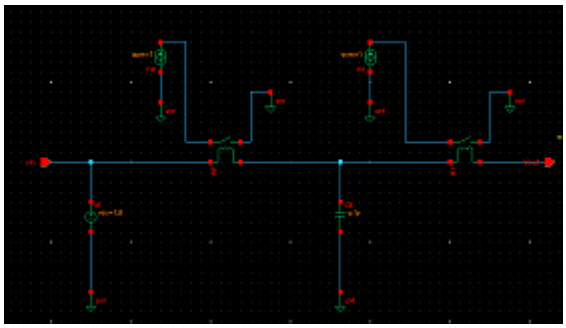

Fig 2. Switched Capacitor circuit

$$Q_{x=} C_x V_x \qquad (1)$$

C_1 charged to V_1 and then V_2 during each clock period. $R_{eq} = \frac{T}{C_1}$ (2)

$$\Delta Q_1 = C_1(V_1 - V_2) \qquad (3)$$

Equivalent average current

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T} \qquad (4)$$

Where T is the clock period.

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}} \qquad (5)$$

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \qquad (6)$$

IV. Proposed Broadband Lna

Fig. 3 shows the simplified schematic of the proposed broadband LNA architecture with switched capacitor .Switched capacitor is used instead of resistor because resistor consumes large area in integrated circuit. In order to minimize the area and making the device smaller switch capacitor is used. The overall noise figure is reduced by incorporating the transistor and connecting the gate of M_p to the gate of M_n in a cross-coupled fashion. This transistor serves two main purposes: 1) to provide the DC current biasing, and 2) to provide an additional gain to increase the overall gain and reduce the noise figure of the LNA. The DC biasing is adjusted with the current source , which is mirrored through the current mirror . This current also determines the gate-source voltages of and , and therefore no additional DC biasing circuit is required. The DC voltage of the output node is determined from the gate-source voltages of and , i.e. . The gate of is biased to ground through the resistance , which is much higher than the value of the source resistance, . Transistor also provides an additional transconductance to increase the overall gain of the LNA. The composite configuration of the NMOS and PMOS transistors. As shown below, this composite configuration of the NMOS and PMOS transistors reduces the output noise of the two transistors and results in a lower output noise. In this configuration, the NMOS and PMOS transistors appear in series. The composite NMOS/PMOS transistors are sized in a way to maximize the bandwidth. In this subsection, a design methodology is presented to find the optimum width of the NMOS and PMOS transistor. Considering the noise generated by the NMOS and PMOS transistors, the cross connection leads to partial noise cancellation of the generated noise. The partial noise cancellation is clarified qualitatively for the proposed architectures.Hence, this configuration amplifies the differential voltage and rejects the common-mode one. Due to series configuration of the two transistors, the transconductance is given by the series combination of the NMOS and PMOS transistors.

In the below given table the $(\frac{W}{L})_{M_N}$ stands for the width and length of the channel in NMOS whereas $(\frac{W}{L})_{M_P}$ denote the width and length of the channel in PMOS. The biasing current is constant of 5 mA and base biasing current is of 9.5 mA. The resistor is replaced by the switched capacitor and its value depends on the capacitor and frequency of the clock period. The value of the resistor decreases with increasing switching frequency or increasing capacitance.

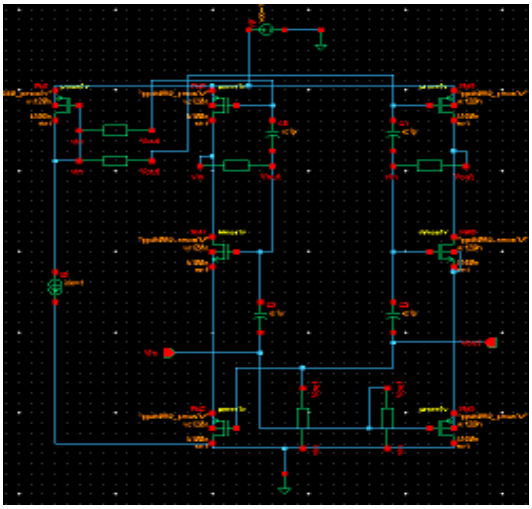

Fig 3.Broadband LNA using switched capacitor

TABLE NO. 1 Circuit element values and Transistor aspect ratios for the implemented LNA

$(\frac{W}{L})_{M_{N1}}$	$(\frac{W}{L})_{M_{P1}}$	$(\frac{W}{L})_{M_{P2}}$	$R_{eq} = \frac{1}{C_1 f_S}$	C_c	$R_b = \frac{1}{C_b f_S}$
$\frac{170um}{0.1um}$	$\frac{465um}{0.1um}$	$\frac{152um}{0.1um}$	1KΩ	7.8pF	100KΩ
$(\frac{W}{L})_{M_{B1}}$	$(\frac{W}{L})_{M_{B2}}$	C_{b_3}	$R_{b_3} = \frac{1}{C_3 f_S}$	$I_{bias,B}$	I_{bias}
$\frac{330um}{0.1um}$	$\frac{80um}{0.1um}$	7.8pF	14KΩ	9.5mA	5mA

Fig 4.shows the complete schematic of broadband LNA .The buffer circuit is used to drive the 50Ω load impedance. The balun function is used to convert the differential input into single output. One end of the LNA is connected to balun function to provide the single input at the input terminal. The other end is connected to buffer. The port is connected at both the end to provide the matching between the devices.

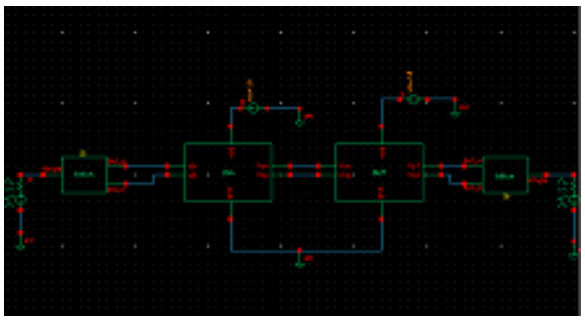

Fig 4.Complete schematic of Broadband LNA

V. Simulation Results

Noise Figure

The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF) (Equation7). Another related and often talked about parameter in RF applications is the Signal-to-Noise Ratio (SNR), which is the ratio of the signal power and the noise power .The Noise Factor is equivalent to the ratio of the SNR at the input and that at the output of the LNA (Equation 8). Hence, the Noise Factor is a measure of to what extent the LNA degrades the SNR.

$$NF = 10\log (F) \qquad (7)$$

$$SNR = \frac{P_{signal}}{P_{noise}} \qquad (8)$$

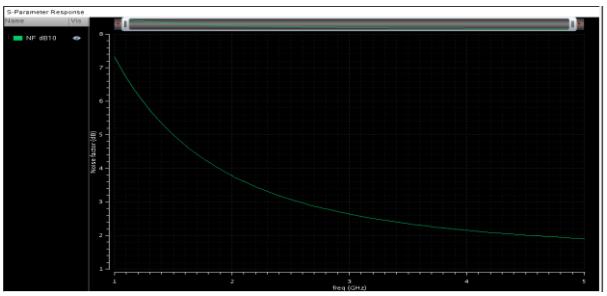

Fig 5.Noise Figure

Scattering Parameters or S-parameters are complex numbers that exhibit how voltage waves propagate in the radio-frequency (RF) environment. In matrix form they characterize the complete RF behaviour of a network. At this point it is necessary to introduce the concept of 2-ports. It is fundamental in RF circuit analysis and simulation as it enables representation of networks by a single device.

As the properties of the individual components and those of the physical structure of the circuit are effectively taken out of the equation, circuit analysis is greatly simplified. The characteristics of the 2-port is

represented by a set of four S-parameters: S_{11}, S_{12}, S_{21} and S_{22}, which correspond to input reflection coefficient, reverse gain coefficient, forward gain coefficient and output reflection coefficient respectively. There are alternative descriptive parameters for 2-ports, such as impedance parameters, admittance parameters, chain parameters and hybrid parameters. These are all measured on the basis of short- and open circuit tests which are hard to carry out accurately at high frequencies. S-parameters, on the other hand, are measured under matched and mismatched conditions. This is why S parameters are favoured in microwave applications. S-parameters are both frequency and system impedance dependent so although manufacturers typically supply S-parameter data with their devices it is not always applicable. Under such circumstances, it becomes necessary to measure the parameters. These measurements are carried out by measuring wave ratios while systematically altering the termination to cancel either forward gain or reverse gain according to the following equations:

$$S_{11} = \frac{b_1}{a_1} \text{ when } a_2 = 0 \qquad (9)$$

$$S_{12} = \frac{b_1}{a_2} \text{ when } a_1 = 0 \qquad (10)$$

$$S_{21} = \frac{b_2}{a_1} \text{ when } a_2 = 0 \qquad (11)$$

$$S_{22} = \frac{b_2}{a_2} \text{ when } a_1 = 0 \qquad (12)$$

Conclusively, the S-parameters relate the four waves in the following fashion:

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad (13)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad (14)$$

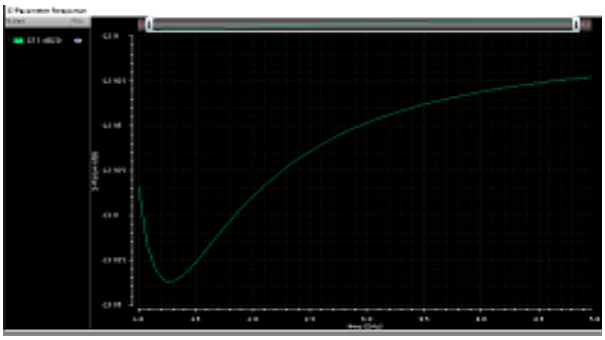

Fig 6. S_{11} Input Reflection Coefficient

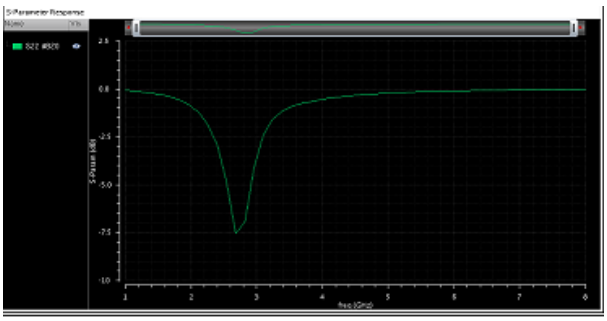

Fig 7. S22 Output Reflection Coefficient

In a stability perspective, an LNA can be either unconditionally stable or potentially unstable. Given the former condition, the LNA will not oscillate regardless of what passive source- and load impedance it is connected to. In a 2-port network, oscillation may occur when some load and source termination cause the input- and output impedance to have a negative real part. There are three main causes for this scenario: internal feedback, external feedback and excessive gain at out-of-band frequencies. In practice, this is done with filtering and resistive loading to attenuate gain. The condition for unconditional stability, in terms of S-parameters is

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad (15)$$

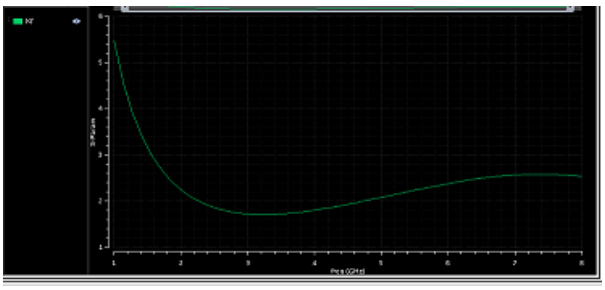

Fig 8.Stability

VI. Conclusion

In this paper An Inductor-less Low Noise Amplifier using Switched Capacitor with cross coupled Transistor pair using 90nm CMOS Technology has been presented. The simulations of the circuit are carried out using gpdk 90nm CMOS Technology in Cadence Virtuoso. The LNA design, we obtained a noise figure, scattering parameter and stability at supply voltage of 1.8 V is reported here. The performance results of simulations are reported. The proposed circuit is observed to have higher stability and better scattering parameter .

A switched capacitor broadband LNA has been designed and implemented in cadence gpdk 90nm CMOS technology.The simulation results found to be Noise figure is 3.1 dB. S11 is -12.97 dBm, S22 is - 5.5 dBm and stability is 1.8 which is greater than 1 means LNA is highly stable.

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