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Arbiter for Runtime Traffic Permutation Using Multi Stage Switching

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Abstract: *Multi processor system on chip (MPSOC) has been consider as the best candidate for applications such as networking, telecommunication, multimedia, etc. which have need of high computational demand, high performance, flexibility, high energy efficiency and low cost design. Multistage switching networks are best suited for applications which use large number of parallel systems and memories.MPSOCS are well associated with switching networks to perform variety of scientific applications and parallel processing.*
The proposed design presents a programmable and configurable arbiter in on chip networks adapted with MPsocs. The network used in design exploits a pipe lined circuit switching scheme associated with dynamic path set up. This scheme is taken to provide guaranteed bandwidth for runtime traffic permutation and it provides dedicated path dynamically under multistage switching networks. The programmable arbiter can be used to increase efficiency of the system by programming with required arbitration schemes. The presence of a multiple scheme arbiter enables us to follow a scheme which is suitable for the application currently using the processor so that efficiency is increased.

Index terms**:** *Multistage switching networks, Pipelined circuit switching, Dynamic path setup, Network on chip, MPSOCs, on chip network topology*.

I. Introduction

Multiprocessor on-chip networks have risen in the past decade as an important class of VLSI family. AMPSoC is a on-chip system that combines most or all the components essential for an application that uses different programmable processors as system components. [1] These designs are mainly used where we need high data transfer rates like telecommunication, signal processing etc. Most of the present trends are emerged with switching networks for multiprocessors. These are mainly used in scientific applications for parallel processing.

A multiprocessor system on chip is generally consists of different heterogeneous processing elements those may be distributed heterogeneously. Sometimes MPSoCs involves large amount of memory. Uniprocessor may not provide enough performance. These processors can handle limited number of PEs and small data. For real time applications multiprocessor Socs are compulsory to meet design constraints like power, area etc. MPSocs can reduce energy consumption and saves power. MPSocs are having so many challenges. Software development is the major challenge and this software should be in a position to gain enhanced performance. Each multiprocessor requires its own software development environment. There are different factors need to be considered for MPsocs like design methodologies and hardware architectures (which CPU is used, what processor is used and what interconnect and topology is used. Over the past decade, various research attempts have encouraged primary enhancements. When formerly evolved systems embedded a single processor, the master of the chip, multiple masters must now share the overall control. The first Multiprocessor System on Chip (MPSocs) was developed. They combine several embedded processors, memories and specialized circuitry (accelerators, I/Os) interconnected through a dedicated framework to provide a complete integrated system. Converse to Socs, Mpsocs incorporate two or more main processors heading the application methodology, attaining higher productions[2].

The paper presents a novel design for proposed guaranteed bandwidth arbitration algorithm for arbiter in multi stage switch circuit. The scheme offers better efficiency for the systems which involves large data rates at high speed .The scheme is proposed for multi stage MPSocs by overcoming drawbacks of previous arbitration schemes like round robin and fixed priority schemes. It also offers pipelined circuit switching with dynamic path setup for runtime traffic permutations.

The rest of this paper is organized as follows. Section II presents the overview of multistage switching networks for MPSocs Section III gives the design approach for proposed design, Section IV presents simulation results and analysis, and finally, Section V concludes this paper and outlines the further researches.

II. Multi Processor System On Chip With Multistage Switch Circuit

Developments in semi conductor technology brought sensational changes in integrated circuit design by scaling down its size. The technology is kept on increasing from single chip, soc and multiple chips. But the services provided by this technology not sufficient because needs and demands are increased. The technology has grown and demands for applications also let the discovery of MPsocs and these has become a major class of VLSI technology. MPSocs have to serve with limited power applications with limited area. MPsocs must fulfill real time deadlines. Mpsocs generally designed with processing Elements, mini architectural blocks and interconnects with particular design parameters [5], [11].

A. On chip network topology

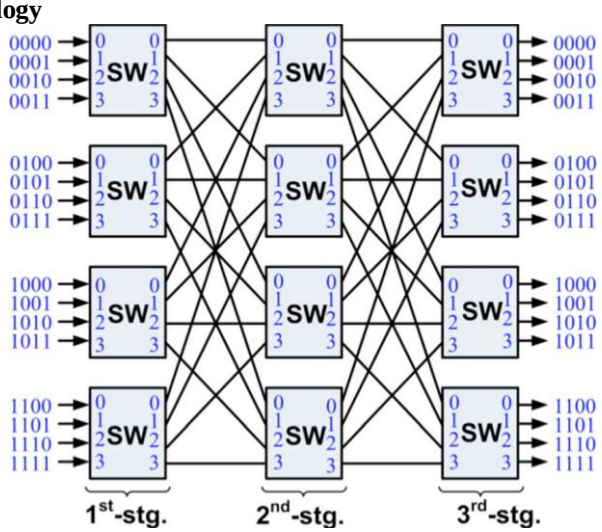

Fig.1. Proposed on-chip network topology with port addressing scheme

The on chip network topology belongs to clos network topology. It is used for commercial applications and it is best suit for MPsocs to support dynamic changes. It employs pipelining concept combined with dynamic path set up. The dynamic path-setup scheme enables arbitrary traffic permutations in run time. Because of dedicated path by circuit switching, data is guarantee reached to output. No data is missed. The circuit-switching approach offers a guarantee of permuted data. The proposed design involves configuration and programming of Arbiter in switch circuit.

Clos network, also one of the important network topology families. It is more importantly used in MPsocs and each network consists of thousands of nodes. The figure shows a three-stage Clos network is named as f(p, q, r), where q represents the number of inputs in each of r first-stage switches and p is the number of second-stage switches. In order to support a parallelism degree of 16 as in most practical MPSoCs, we proposed to use f(4,4,4) as a topology for the designed network (see Fig 1). The peculiar behaviour of this topology is its rearrangeble property. Depends on our obligation we will lessen number of stages so that we reduce wiring costs there by implementation cost.

B .Common switch architecture and Programmable arbiter

These switches are all same as regular switch construction modelling shown in Fig.4.3. The difference between each switch is each one having different probing algorithms. The switch architecture has three main components: INPUT CONTROLs (ICs), OUTPUT CONTROLs (OCs), an ARBITER, and a CROSSBAR. To save the wiring costs Incoming probes are send through data paths. The ARBITER has two main functions:

- Connection of the Ans_Outs and the ICs with the Grant bus,
- As a ref for the solicitations from the Ics.

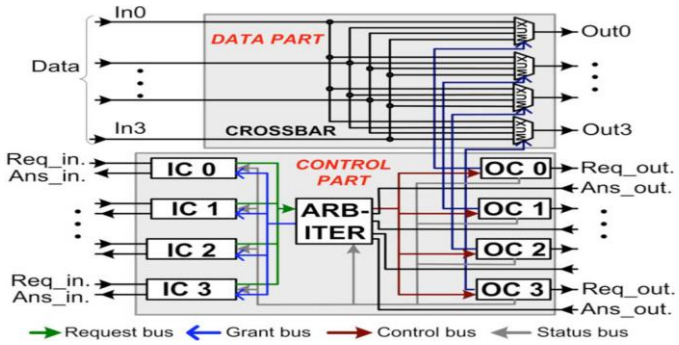

Fig.2. Common switch architecture

The IC is used to cheque the output status through status bus when more than one incoming requests are reached at input and requests the ARBITER to connect to the requested OC through the Request bus. The ARBITER cross-connects the corresponding Ans_Out with the IC through the Grant bus When accepting this request. The programmed ARBITER will apply its pre defined arbitration schemes and it solves the data conflict problem. When connection is happened only one output is selected, where as remaining routes are blocked.

Programmable Arbiter

In the previous design, the switch circuit consists of Arbiter as shown in above figure 2. This arbiter can be programmed and configurable with different arbitration schemes To overcome drawback in the previous system with arbitration schemes ,new design is proposed with new arbitration scheme for better efficiency. The previous schemes are itself are having drawbacks and these schemes are not suitable for all the real time applications.

Proposed Arbitration scheme-Guaranteed Bandwidth (GBW) Scheme

In this scheme, all tasks or devices will get access those who put request for grant to communicate with other device. By overcoming drawbacks of above two schemes, means inefficiency in round robin, starvation problem in fixed priority, and this scheme provides better results so that the efficiency is increased

How this scheme works?

For example, four devices are trying for accessing or communicate with other device. All devices has put request for grant. We first initially assign priorities. Initially the highest priority device gets access. What about other devices? Now the highest priority will get decreased by one value in next clock cycle or after getting first access. This process will continue until to the next highest priority value. Now the second highest priority device will get access. This process will continue to the next highest priority value and so on. In this all the devices will get access those devices put request for grant. So all the drawbacks are overcome and efficiency is increased.

III. Design For Proposed Arbitration Scheme

Fig 3 shows block diagram of proposed arbitration scheme. When arbitrate signal is high arbitration can be happened. Arbitrate signal is used to programming the all arbiters which are presented in the switch circuit and the current master priority value stored in corresponding address in priority table and also current master value decremented by one value. Master number and priority signals are inputs for Multiplexer. Write signal at input side of Multiplexer is used for programming masters with priorities and it is high while programming. The output write signal is used to write the data and address in priority table. Then the request vector and priorities are logical ANDedbitwisely and the output is given to parallel comparator. The parallel comparator compares all values and gives highest priority signal as output. The actual output of parallel comparator is the priority value. Then only feedback from current master to the multiplexer is possible. The current master will always get access. In this way all devices will get grant to access the data. So that the throughput of system is increased.

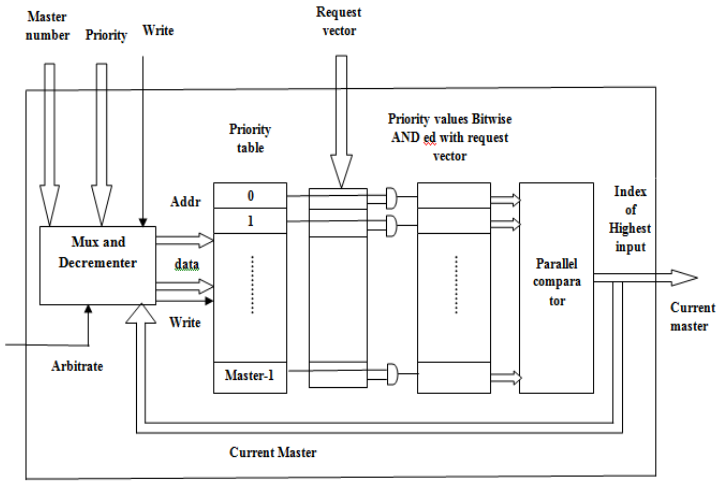

Fig.3. Block Diagram for proposed arbitration scheme

IV. Simulation Results

In multistage switching networks there are several stages involved in real time for traffic permutations. These permutations dynamically changes as per availability of path for connection. Here, the network employs a 3x4 on chip switch network topology, each stage having four switches and each switch having four inputs. Any device from input side can send data to any device on output side. For example, any of four devices wants to communicate with same output at output side, for this we need to put high request on signals. The output has to appear at required destination. Initially, arbiters are programmed with priorities for each device or input. In the simulation results, four devices or requests for same output at destination. In the proposed arbitration scheme, the data of four inputs reach the required destination and each device gets access. Efficiency is increased. Verilog HDL language is used for programming and ModelSim are used for simulating the proposed circuit.

The proposed on chip topology is a 3 stage switch circuit. At input side, four switches are present and each switch consists of 4 inputs. So totally there are 16 inputs. To explain arbitration, for example 4 ports are requesting for same output at destination. Since all ports are requesting the same output, the requested address is same. Here it is written as 0_0_2. That means 0^{th} arbiter,0^{th} port in the 2^{nd} stage. The output has to be reached to that address location. The below figures shows simulation results

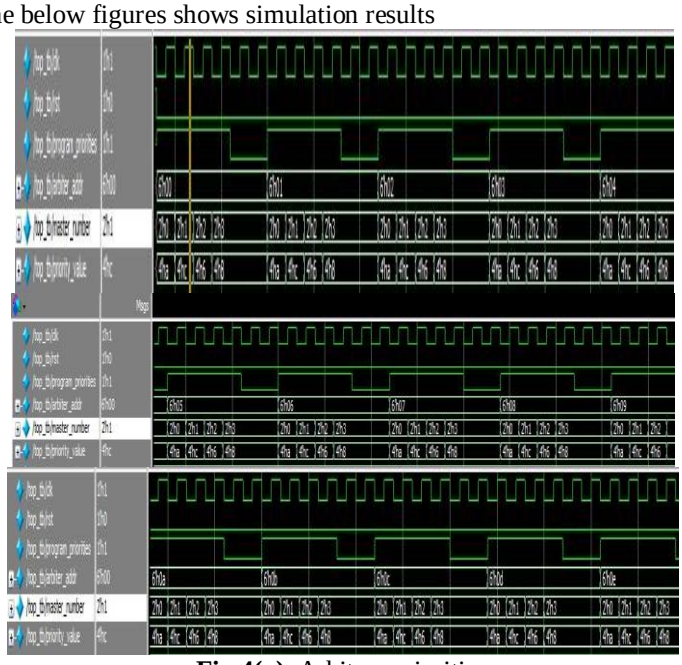

Fig.4(a). Arbiters priorities

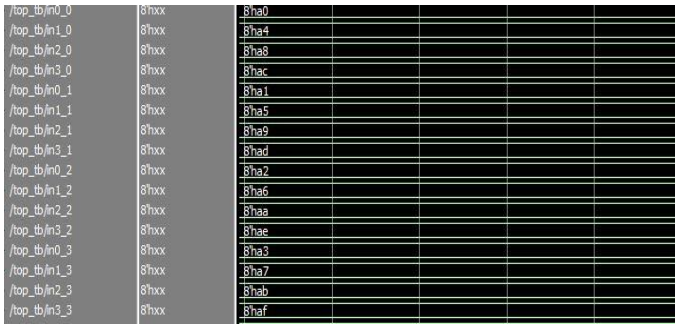

Fig.4(b). Data at input ports

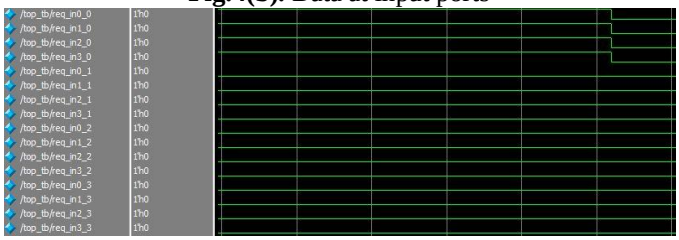

Fig.4(c). Request signals for the required destination

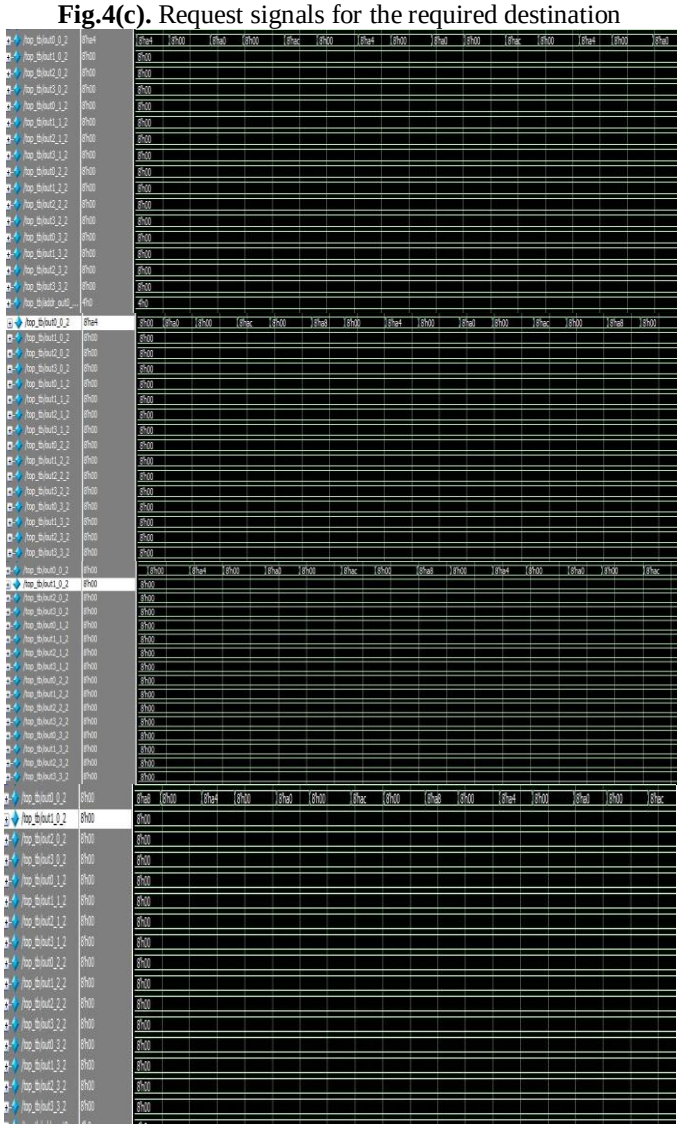

Fig.4(d). Output at required destination port (0_0_2)

V. Conclusion

Heavy traffic permutation in multistage switch circuits is sustained. The design uses a circuit-switching approach combined with dynamic path-setup scheme under a closed network topology. The proposed design offers a configurable and programmable arbiter with different arbitration schemes for arbitrary traffic permutation in runtime and the throughput is increased so that the efficiency of system also improved compared to the earlier design. This design may meet the present real time switching network applications which involves high data rates.

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