

Comparison And Performance Analysis Of Phase Frequency Detector With Charge Pump And Voltage Controlled Oscillator For PLL In 180nm Technology

Atul A. Jadhav, S. K. Parchandekar.

Department of Electronics, Walchand College of Engineering, Sangli, India.
Department of Electronics, Walchand College of Engineering, Sangli, India.

Abstract: This paper presents the performance analysis between two different Phase Frequency Detector approaches with Charge Pump. The Phase Frequency Detector (PFD) is an important building block of phase locked loop (PLL). The conventional and modified architecture of phase frequency detector with charge pump are compared in terms of area and power consumption. The phase frequency detector and charge pump are designed and simulated using Cadence tool in GPDK 180nm technology. The modified phase frequency detector has either UP or DOWN signals at a time. The conventional PFD also has one output either UP or DOWN at a time. The charge pump varies VCONTROL voltage according to the UP or DOWN signal which in turn controls frequency of voltage controlled oscillator (VCO).

Keywords: Charge Pump, Loop Filter, PFD, PLL, VCO.

I. Introduction

Phase locked loops or PLL's are widely used circuits for clock generation and distribution. PLL can be found in various system applications where data needs to be clocked, this includes DSP's, FPGA's, processors and micro-controllers etc. In simple terms PLL is a feedback system that generates a signal which has fixed relation with the phase of incoming reference signal. The PLL consists of phase detector and voltage controlled oscillator (VCO). The purpose of the phase detector is to compare the phase variation of the signals applied at its two inputs. Reference signal is treated as one input while output of VCO is treated as second input. This is commonly known as feedback loop. A PLL is a control loop consisting of four fundamental components. These are a phase detector (sometimes called phase comparator), loop filter, voltage controlled oscillator (VCO) and a frequency divider as shown in fig. 1.

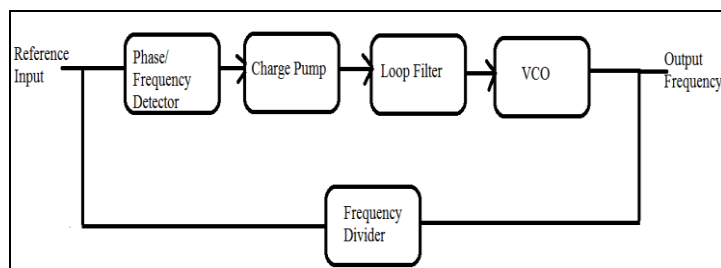


Fig. 1: Basic Building Blocks of Phase Locked Loop

The capture range of a PLL is the frequency range centered about the VCO's free-running frequency, over which the loop can acquire lock with the input signal. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the lock range.

II. Phase Frequency Detector

The conventional PFD is as shown in fig. 2 consists of two D- F/F and one NAND gate [1]. PFD takes two inputs that is one is reference signal and other is VCO. The VCO output is directly taken or not that depends upon requirement. These two inputs may differ in phase or frequency. The PFD produces two signals known as UP and DOWN. UP signal is generated when phase of reference signal has a value greater than feedback signal whereas DOWN signal is generated when reference signal has a value less than feedback signal. The output of this PFD drives the charge pump to produce V_{BIAS} voltage for the VCO. Depending upon the output of PFD the control voltage i.e. output of the charge pump may increase or decrease. If UP signal is at logic high then control

voltage may increase and if DOWN signal is at logic high then control voltage may decrease. The input signal may differ in either phase or frequency. The PFD produces output for both of these variations.

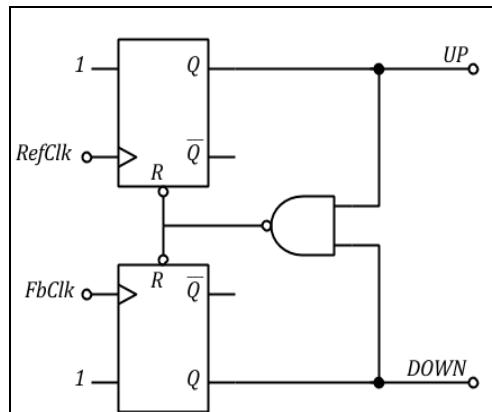


Fig. 2: Phase Frequency Detector

The fig. 3 below is showing architecture of modified PFD into the Cadence GPDK180nm technology [2]. The proper output required is either UP signal is generated or DOWN depending upon leading and lagging of reference clock with respect to VCO output. Figures 3, 4, 5, 6 shows circuit diagram, Layout of PFD, generated UP signal and DOWN signal respectively.

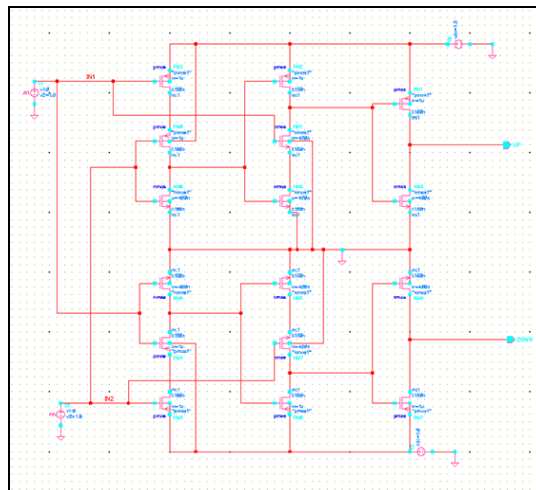


Fig. 3: Schematic of modified PFD1 in Cadence tool

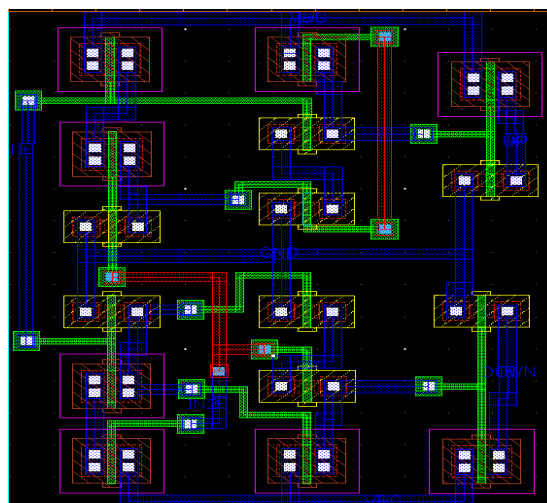


Fig. 4: Layout of modified PFD1 in Cadence tool

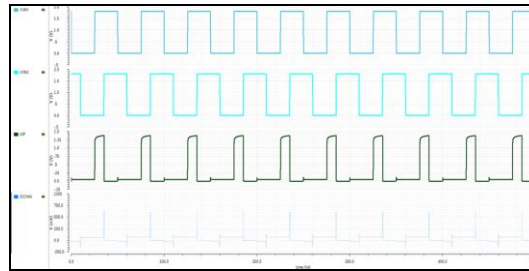


Fig. 5: Output waveform of UP signal

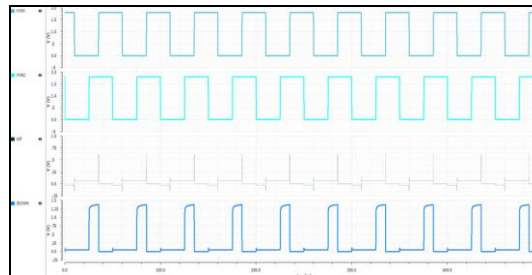


Fig. 6: Output waveform of DOWN signal

Another design of PFD2 is as shown in fig. 7 [3]. This PFD is constructed in Cadence virtuoso tool using GPDK 180nm technology. When V_{IN1} signal is leading with respect to V_{IN2} then PFD generates UP signal and PFD produces DOWN signal when V_{IN2} is leading. The fig. 9 and 10 shows the transient output UP & DOWN signal of PFD.

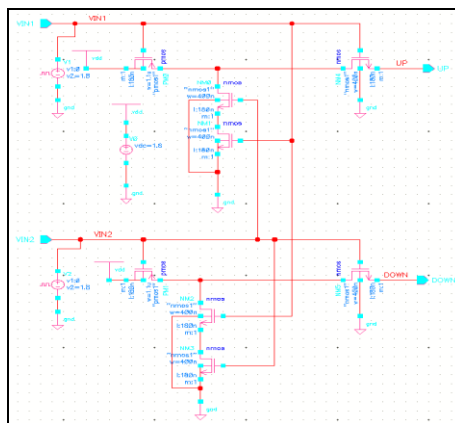


Fig. 7: Schematic of modified PFD2

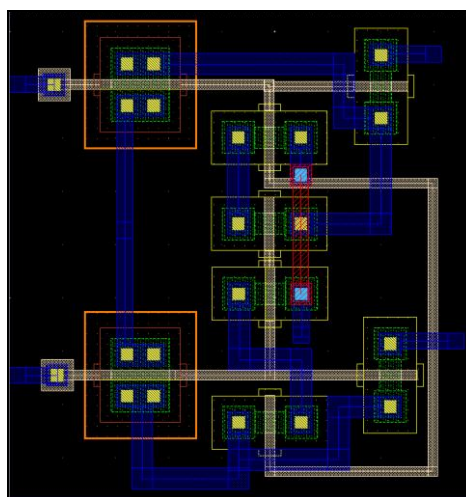


Fig. 8: Layout of modified PFD2 in Cadence tool

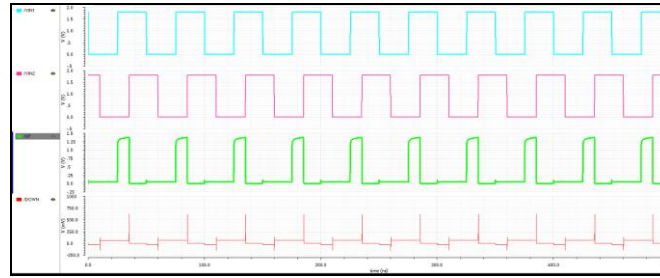


Fig. 9: Output waveform of UP signal

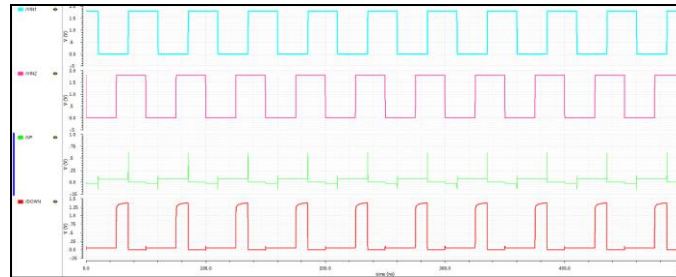


Fig. 10: Output waveform of DOWN signal

III. Charge Pump

Various charge pumps can be constructed by using MOSFET's only. We have considered the two types of charge pumps. The charge pumps can produce the voltages as double voltage, triple voltage, halves, invert, fractionally multiply or scale the voltages such as (3/2, 4/3, 2/3, etc.) and generate arbitrary voltages by quickly alternating between modes depending on the circuit topology. But when charge pump is used in PLL then it can supply positive and negative current pulses into loop filter of PLL. But it cannot produce higher or lower voltages than its power and ground supply levels.

The charge pump takes input from PFD i.e. continuous pulses of UP or DOWN signal and generates a control voltage. Generally a charge pump is used with loop filter or with only a capacitor. A capacitor is charged or discharged according to UP and DOWN signal. When UP signal is generated then current flows into the loop filter and capacitor gets charged. When DOWN signal is generated then current flows out of the loop filter and capacitor gets discharged. Fig. 11 shows one type of charge pump. It has two PMOS and two NMOS. The upper PMOS and lower NMOS acts as current sources. The second PMOS is provided with UP signal and NMOS is provided with DOWN signal.

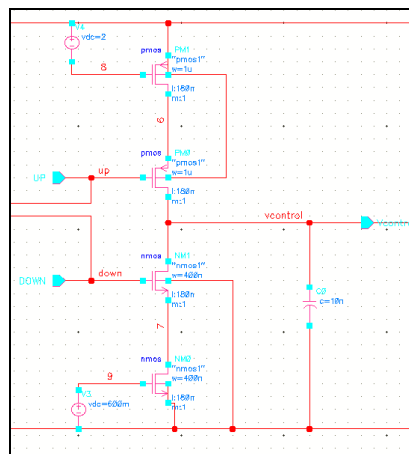


Fig. 11: Charge Pump Type – I

The second type of charge pump is as shown fig. 12 [4]. This charge pump uses the current source of 20uA signal. By using this charge pump we can also vary the control signal depending upon the UP and DOWN signal. The output shows the variation i.e. $V_{CONTROL}$ goes on changing depending on UP and DOWN signal.

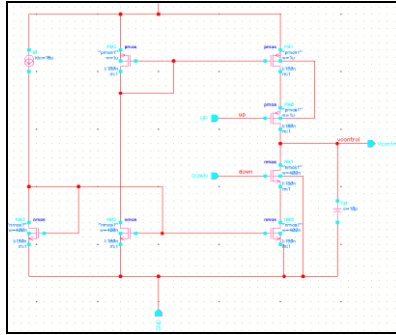


Fig. 12: Modified Charge Pump

The use of current mirror is preferred instead of current source. Fig. 13 shows the current mirror which produces the same current as that of current source.

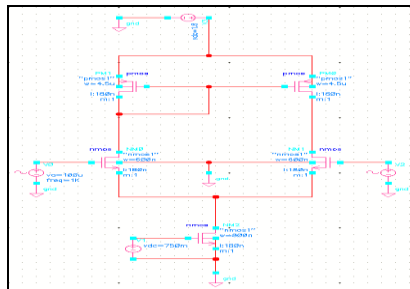


Fig. 13: Current mirror

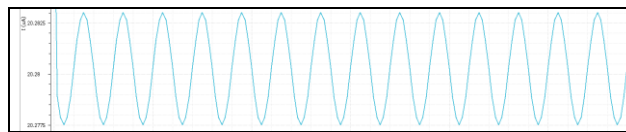


Fig. 14: Output of Current Mirror

We cannot produce the layout of any source in CADENCE GPDK tool. Hence we replace the current source by current mirror. Fig. 15 and 16 shows the schematic and layout of the charge pump respectively.

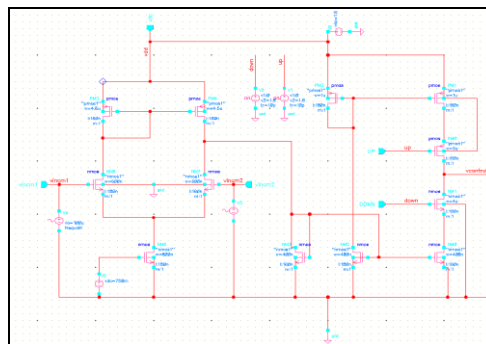


Fig. 15: Charge Pump with Current Mirror

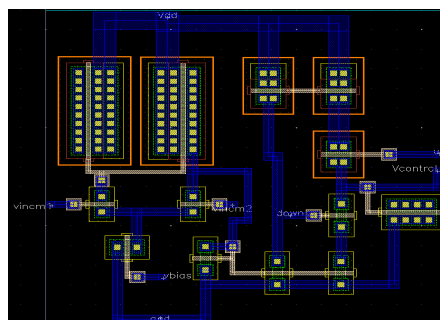


Fig. 16: Layout of charge pump

In the Cadence tool, we also can extract the parasitic components. Parasitic components are those components which are undesirable and unavoidable. Fig. 17 shows extracted parasites of charge pump. Figure 18 showing the zoomed result of parasite components i.e. showing capacitors and resistors.

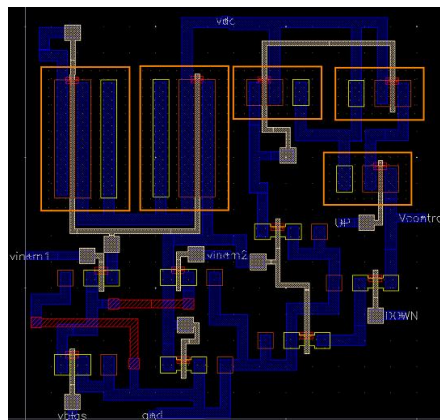


Fig. 17: Av_Extracted of charge pump

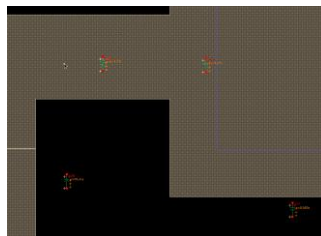


Fig. 18: Zoomed Av_Extracted of charge pump

IV. Loop filter

PLL is generally has a charge pump with loop filter. Loop filter is low pass filter which plays important part in stabilizing of our entire system. Loop filter is a low pass filter. The loop filter can be implemented as shown in fig. 19. The main function of loop filter is to convert signal from PFD to a ripple free DC control voltage. When we use two capacitors then circuit becomes 3rd order. Hence we have to choose $C_2 \leq 0.2C_1$, where C_1 is used to store a charge, R_1 provides stability, and C_2 is used to cancel the ripple present in $V_{CONTROL}$.

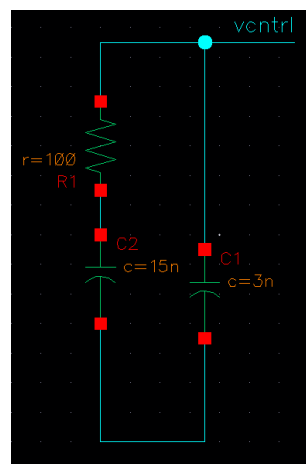


Fig. 19: Loop Filter

Charge pump with loop filter

The two input signals are compared at PFD and the two outputs UP and DOWN signals are generated depending upon the phase difference between two input signals. When these two signals are given to the charge pump with loop filter then either $V_{CONTROL}$ signal goes high or goes low respectively. Fig. 20 and 21 shows the output when $V_{CONTROL}$ goes high and low respectively.

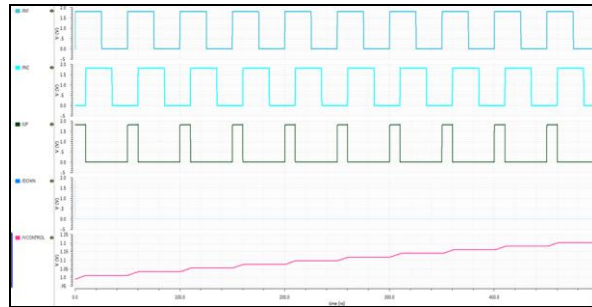


Fig. 20: Output of Charge Pump with Current Mirror showing $V_{CONTROL}$ goes on increasing while UP signal is High

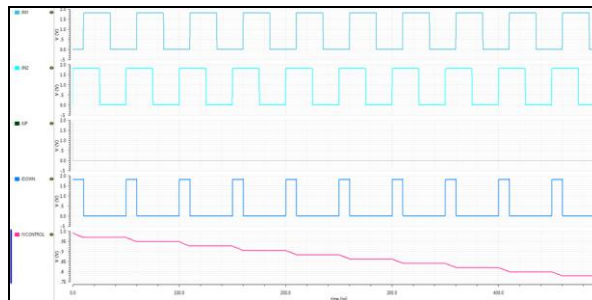


Fig. 21: Output of Charge Pump with Current Mirror showing $V_{CONTROL}$ goes on decreasing while DOWN signal is High

V. Voltage Controlled Oscillator

Fig. 22 is showing three stage ring oscillator with one more NMOS device acting as control bias voltage to the oscillator [4]. When the circuit is with both the PMOS and NMOS device i.e. both pull up and pull down device respectively then called as current starved VCO. In the proposed design only NMOS devices are used. The voltage source V_{BIAS} used to control the current through the oscillator. The last inverter is used only to get the square wave output. The schematic and layout of the VCO is as shown in fig. 22 and 23 respectively.

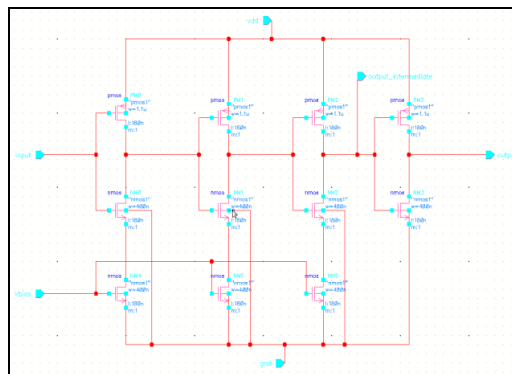


Fig. 22: Schematic of the VCO

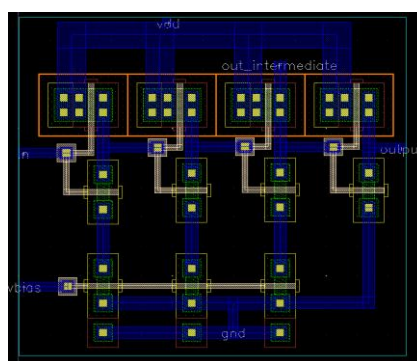


Fig. 23: Layout of the VCO

The input to the VCO is DC voltage given by the loop filter. The loop filter output is dependent on the charge pump. If current through the charge pump is increasing, then output voltage of loop filter goes on increasing hence output of VCO. If current through the charge pump is decreasing, then output voltage of loop filter goes on decreasing hence output of VCO. The parasitic components of this VCO are extracted and are shown in below table I, & fig. 24.

Table I. Summary for VCO/av_extracted

Lib	Cell	View	Total
analogLib	pcapcitor	symbol	116
analogLib	presistor	symbol	43
gpdk180	Nmos	ivpcell	7
gpdk180	Pmos	ivpcell	4

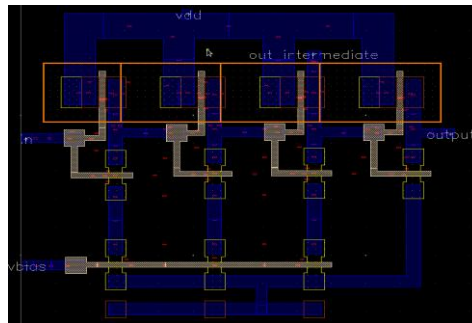


Fig. 24: Parasites extracted of the VCO

VI. Phase Locked Loop

The complete PLL schematic is as shown in fig. 25. The charge pump used is with loop filter. The analysis is done for 400nsec. The output of total PLL is shown in fig. 26. The power consumption is 2.182mw. The output frequency of VCO is 3.75GHz for both PFD1 and PFD2. We can use any PFD to get the same frequency. Some noise may occur in output frequency.

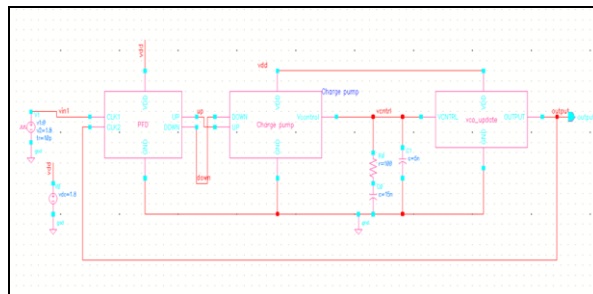


Fig. 25: Schematic of PLL

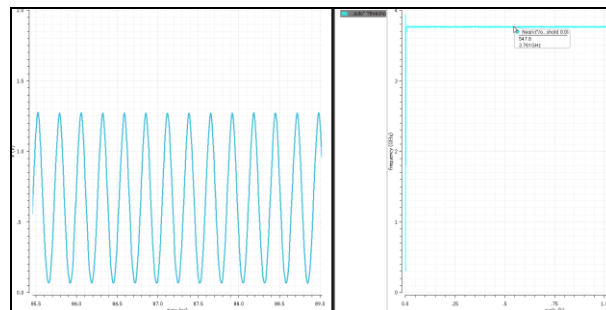


Fig. 26: Output frequency of PLL

VII. Results

The power and area requirement of the PFD are shown in table II. The power consumption is also depends upon the VDD source used. The power consumed and area acquired by PFD2 is less than PFD1 due to less number of transistors required. The power consumed by PFD1 is 217pW and that of PFD2 is 16.2pW. Also area acquired by PFD1 and PFD2 is 194.53 and 79.32 μm^2 respectively.

Table II. Summary for PFD

Schematic	Power (pW)	Area (μm^2)
PFD1	217	194.53
PFD2	16.2	79.32

The area required for the charge pump is $253.84 \mu\text{m}^2$ and to that of VCO is $144.41 \mu\text{m}^2$. The power consumption for the charge pump and VCO are $195 \mu\text{W}$ and $324.7 \mu\text{W}$ respectively.

VIII. Conclusion

PFD takes the two inputs as reference clock signal and VCO output signal and according to leading and lagging phase of reference it produces UP and DOWN signal. The charge pump takes these two signals and controls the voltage output at loop filter. The frequency of VCO goes on changing depending on V_{CONTROL} signal. The PLL with PFD2 consumes less power and requires less area. The proposed PLL generates a stable frequency output with PFD1 and PFD2.

References

- [1]. Md Monirul Islam; Ankit Shivhare, "The design of a low power floating gate based phase frequency detector and charge pump implementation," International Journal of VLSI design & Communication Systems (VLSICS), Vol.4, No.2, April 2013.
- [2]. Kailuke, A.C.; Agrawal, P.; Kshirsagar, R.V., "Design of Phase Frequency Detector and Charge Pump for Low Voltage High Frequency PLL," Electronic Systems, Signal Processing and Computing Technologies (ICESC), 2014 International Conference on , vol., no., pp.74,78, 9-11 Jan. 2014
- [3]. Majeed, K.K.A.; Kailath, B.J., "Low power, high frequency, free dead zone PFD for a PLL design," Faible Tension Faible Consommation (FTFC), 2013 IEEE , vol., no., pp.1,4, 20-21 June 2013
- [4]. Sreehari, P.; Devulapalli, P.; Kewale, D.; Asbe, O.; Krishna Prasad, K.S.R., "Power optimized PLL implementation in 180nm CMOS technology," VLSI Design and Test, 18th International Symposium on , vol., no., pp.1,2, 16-18 July 2014.