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Built in Self Test for Programmable System on Chip's Analog to Digital Converter

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Abstract: *In this paper the built in self test for analog to digital converter of programmable system on chip is implemented. The new approach for finding out static errors in ADC is based on time. This approach uses ramp signal and determines time difference between two successive samples, which in turn leads to finding out the static error like DNL, INL of the ADC. The proposed work uses PSoC devices which enable us to design a complete mixed signal system with few off chip components To test static parameter of ADC on chip components are used. Ramp signal is generated by using on chip IDAC of PSoC. The BIST circuit implemented here calculate DNL, INL based on timing i.e. a new approach to calculate DNL, INL is implemented and verified.*
Keywords: *BIST, Mixed Signal, ADC, PSoC*

I. Introduction

It is well known that simple electronic medical equipment consist of not only digital part but also analog part used for converting analog output if sensor into its digital equivalent. Testing of all the circuits is done and at various level. Every electronic circuit undergoes many tests before packaging. Some of the circuits need to be tested very frequently after packaging also while operating in field like health monitoring system, Aeronautical systems and many more safety critical systems. BUILT IN SELF TEST (BIST) is a technique used to test the circuit itself. This technique is used to test the circuit in field.

The instruments used for monitoring and control health related parameters like blood pressure, sugar etc in hospitals are checked and calibrated after fixed interval. Thus instruments used in hospitals are reliable and gives correct information about health. The growing electronics industry has also developed health monitoring system for homecare. Now we also have some devices to check level of sugar and blood pressure at home. Homecare can be made feasible if the medical equipment is reliable. For sophisticated medical equipment to be reliable it is necessary to test the equipment frequently and calibrate. To make the system reliable BIST technique can be used to test the system.

II. Liturature Review

Any health care or safety critical equipment has to deal with real world signal; this means that the inner circuitry must be composed of signal processing unit, Analog to Digital Converter (ADC) etc.

Till now, many researchers have worked on different methods for testing ADC. Yun-Che Wen and Kuen-Jong Lee suggested a technique to test ADC in which a ramp input signal is generated by integrator [1,2,4]. Square wave input to this ramp generator is given from the microcontroller. This ramp signal is applied to ADC as input. Output of ADC is compared with output of the counter. Testing procedure is carried with the help of testing circuit. In this technique only sample number in which DNL or INL present is detected [1].

Jiun-Lang Huang, Chee-Kian Ong, and Kwang-Ting Cheng suggested deltasigma modulation based approach in which delta sigma modulator converts the desired signal to one bit digital bit stream which is applied to one bit DAC followed by LPF [3].

Zbigniew Czaja [2,7] implemented microcontroller based built in self testing method. A simple embedded mixed signal system contains both digital and analog circuit. The analog part is used to convert analog signal into digital i.e. ADC. To test ADC of such system BIST circuit can be implemented in the controller itself and a reconfigurable BIST can be created only during the testing time. The analog input generated by integrator in [2] is converted back into its square pulses and time duration of the pulses is measured and fault is detected according to measurement results.

Zbigniew Czaja in [7] presented a BIST on ATMEGA16 microcontroller. In this approach the 8 bit internal timer is used to generate square wave which is used as input of integrator. Output of integrator is ramp signal. This ramp signal is used as test input to ADC. The ADC samples the input ramp signal at moments assigned by another 16 bit timer. The results are then stored and calculation of DNL and INL is done latter.

Many researchers used DAC to generate input analog signal. The DAC used for generating input analog signal must be at least 3 bit higher resolution then ADC under test [4]. The BIST scheme presented by Jason

Wibbenmeyer and Chien-In Henrt Chen utilizes an on chip ROM to store the digital test signal. The digital test signal is applied to on chip DAC and converted analog signal is applied to ADC under test. Output of ADC is then applied to a Fast Fourier transform for further analysis.

III. Proposed Architucture

The ramp signal generated by current DAC is applied to the ADC of PSoC. The ramp generator and ADC are synchronized. ADC take samples continuously and converted digital values are stored in temporary memory. Two different approaches are used to calculate the DNL and INL of ADC. One is based on the time to appear next code on output of ADC and another is based on comparison of output of ADC with expected output.

In first approach the time taken to appear next code on output of ADC is measured. Difference of time duration of successive code is taken. For DNL to be 0 the time of two successive codes must be same, if difference of time duration of two successive codes is not 0 then DNL error is localized here. According to difference observed in time duration DNL and INL are calculated. A 16 bit timer is used to measure the timing of codes. If time taken in changing the output of ADC from n to (n+1) is t_n us and time taken in changing the output of ADC from (n+1) to (n+2) is t_{n+1} us. If the expected time to change output is t us then DNL can be calculated by following formula.

$$DNL(N) = ((t_n - t_{n-1})/t) \qquad (1)$$

The above formula is derievd from conventional formula given in equation below

$$DNL(N) = \frac{[Vn\text{-}Vn_{-1}]\text{-}V_{LSB}}{V_{LSB}} \qquad (2)$$

To derive the formula let us assume that input is a ramp signal. Now if input is a ramp signal then time elapsed between two successive sample must be constant for DNL to be zero. If time elapsed between to successive sample is not equal to a predetermined constant value then DNL error is localized here.

Let us assume that expected time duration i.e. difference of time between two successive sample is t this time can be takrn equivalent to $V_{LSB.}$ Where V_{LSB} is difference between to successive voltage.

$$V_{LSB} = Vn - Vn\text{-}1 \sim t$$

From avove equation put value of V_{LSB} in equation (2)

$$DNL(N) = \frac{[Vn\text{-}Vn_{-1}]\text{-}[V_{n-1}\text{-}V_{n-2}]}{[V_{n-1}\text{-}V]}$$

$$DNL(N) = \frac{t_n\text{-}t_{n-1}}{t}$$

In second method the expected output of ADC is calculated according to formula derived previously and compared with observed values and DNL, INL is calculated. In this approach difference of expected output and observed value is calculated. Digital equivalent value of V_{LSB} is subtracted from this difference and finally result of this stage is divided by digital equivalent of V_{LSB}.

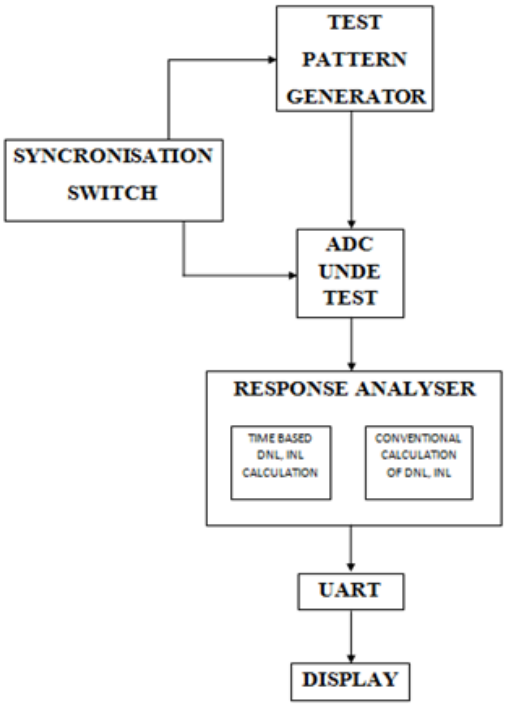

Figure1. Proposed Architecture

IV. WHY PSOC

The BIST implemented in this project could also be implemented on other platforms such as given below

- FPGA
- ARM processor
- ATMEGA series of controllers
- MSP controllers.

The main idea of using PSoC for this project is based on the motivation of the project. The project is developed here keeping in mind the requirement of BIST for ADC of medical equipment made for home care. It can be seen on the website of Cypress Semiconductor that PSoC architecture can be used to implement blood pressure monitoring system. Thus the whole system can be implemented on single device.

The PSoC is used here because it has many advantages over other available platforms. PSoC is most flexible of all architectures available today for mixed signal systems. It is very easy and less time consuming to use flexible and reconfigurable architecture of PSoC. The whole BIST can be implemented on PSoC minimum number of external components is required i.e. only 2 resistors and one potentiometer are used in the project externally

V. Conclusion And Future Work

The project implemented here using on chip component of PSoC few external component are used. New approach of calculating DNL and INL is implemented successfully. DNL, INL are tested and compared with conventional formula of calculation of DNL, INL and were found to be same. The INL were found to be 3 lsb, 5 lsb and 6 lsb. Histogram for different time interval appeared is shown below in figure 2.

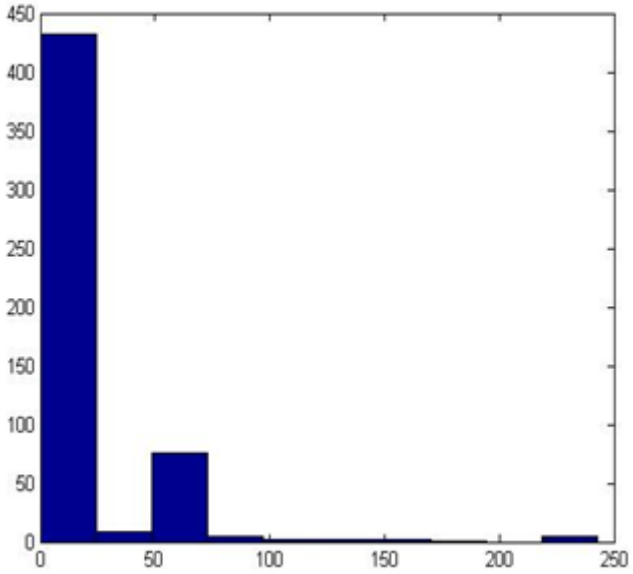

Figure 2 Histogram for different time interval

In this work DNL and INL is calculated by using time difference between successive samples. As we know that the time difference between two successive samples will appear same most times, thus we just need to take care of this constant time which makes calculation easy, whereas in conventional approach we need to consider full range of voltage for histogram,. in this way it can be concluded that no of memory element required is less in time based approach.

Currently the work presented over here is meant for medical equipments, normally which operates at low frequency, thus the present BIST architecture considers only linear error, so scope is still there for nonlinear error which normally presents in an ADC operating in the high frequency ranges. The project is implemented here keeping in mind the medical equipment made for home care, thus in future the whole equipment can also be implemented on PSoC.

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