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An Efficient Dynamically Reconfigurable Fir Filter Using Multiprecision Razor Based Multiplier with Frequency Scaling

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Abstract: *This paper presents a multiprecision (MP) dynamic and partially reconfigurable fir filter that incorporates variable precision, parallel processing (PP) multiplier, razor-based error detection, dynamic frequency scaling and dedicated operands scheduling to give optimum performance for a variety of operating conditions. Each of the building blocks of the proposed architecture can either work as independent smaller-precision systems or work in parallel to execute higher-precision system. Our aim is to realize a less-delay; area-efficient reconfigurable digital signal processing design that is implemented using Xilinx Synthesis Tool on Virtex5 FPGA kit. The proposed design provides area efficiency and flexibility by permitting dynamically insertion and/or removal of the individual modules to execute various taps for the partial reconfigurable FIR filters. The FIR Filters are being designed using HDL languages since speed is an important interest in this era; the main objective is to improve the speed of the system. In the whole system if the speed of the individual block is improved the overall speed of the system is enhanced. The synthesis results show that the proposed MP design features a minimum-delay and also a reduction in circuit area when compared with reconfigurable fir filter using conventional fixed-width multiplier.*

Keywords: *Reconfigurable Fir Filter, Razor Flipflops, Opearands Scheduler*

I. Introduction

FIR filters are implemented in majority digital signal processing (DSP) systems. The emerging of various applications (image, audio/video processing and coding, filtering, etc.) in terms of power, area, speed, performance, system compatibility and reusability make it vital to design the reconfigurable architecture. This paper presents a partially reconfigurable multiprecision FIR filter design that aims at meeting all the goals (low-power consumption, reconfigurability etc) .Fpga (Field Programmable Gate Arrays) are programmable logic structures that allows the implementation of digital systems. Most of the FPGA systems can only be configured statically. Static reconfiguration refers to configure the device completely before execution. If reconfiguration is required, it is essential to stop system execution and reconfigure the system all over again. Several FPGAs support performing partial reconfiguration, which reconfigures only a given subset of internal modules.

Dynamic Partial Reconfiguration (DPR) sanctions the required module of FPGA be modified while the rest of the system operates without getting affected. Module-predicated partial reconfiguration was proposed by Xilinx which allows the designer to divide the whole system into modules.

Multiplication is an important fundamental arithmetic operation and its applications such as multiply and accumulate (MAC) are implemented in Digital Signal Processing (DSP) applications such as DFT, Finite Fourier Transform (FFT), convolution, etc. Since multiplication increases the execution time of most DSP algorithms, there is a requisite for high speed multiplier. Reducing the power consumption and time delay are some crucial requisites for many applications. Minimizing power consumption for digital designs involves optimization at every caliber of the design. This optimization depends on the technology used in implementing the digital circuits. Suitable multiplier architecture is selected based on the application and implemented in fir filter. Latency and throughput are the two foremost delay concerns for multiplication algorithms performed in DSP applications. Latency refers to the real delay of processing a function; a measure of stability of the inputs to a device and throughput can be defined as the measure of how many multiplications can be done in a given period of time. Multiplier is not only a high delay structure but a major source of power dissipation. To reduce power utilization, it is important to reduce the delay by utilizing different delay optimizations.

Since consumers demand for portable and high performance electronic products, the constraints on the power consumption of individual components have increased drastically. Of these, multipliers perform complex arithmetic operations in DSPs such as fir filters. For embedded applications, it has become crucial to implement power-aware multipliers. The complex structure of multipliers results in unbalanced paths and hence unwanted glitch generation and propagation. Through optimization at architectural and transistor-level, internal paths are balanced and the switching rate can be reduced and thereby reducing internal path delays. Dynamic power

reduction also can be obtained by controlling the effective dynamic range of the input operands and thereby disabling unutilized sections of the multiplier. The majority of today's application-specific integrated circuits (ASICs) and full-custom DSPs are developed for a fixed maximum word-length so that it can hold the worst case scenario. Hence an 8-bit multiplication performed on a 32-bit Booth multiplier could cause unwanted switching activity and power loss. A flexible approach is using several multipliers grouped together to grant higher precisions and hence reconfigurability. This paper involves a group of multipliers of various precisions, with each optimized. Each pair of arriving operands is routed to the smallest filter that computes the result and thereby achieving lower energy utilization of the smaller circuit. But this can result in increased chip area. Sharing and reusing some functional modules within the system can tackle this issue. Pipelining also can improve the multiplier's performance. Combining multiprecision (MP) with dynamic frequency scaling (DFS) can offer a considerable reduction in power utilization by adjusting the frequency based on the circuit's run-time workload rather than setting it for the worst case scenario. A recovery mechanism using razor flip flops is then applied to identify error occurrences and restore the accurate data. As it entirely removes worst case safety margins, error-tolerant DFS techniques can further reduce power consumption and thereby minimizing the delay.

II. System Overview And Operation

The proposed system comprises five different modules that are as follows:
1) Dynamical reconfigurable FIR filter.
2) The multiprecision multiplier;
3) The input operands scheduler (IOS) whose task is to reorganize the input data stream into a buffer and thereby decrease the voltage transitions;
4) The frequency scaling unit produces the necessary operating frequency of the multiplier;
5) The MP multiplier has razor flip-flops which can report timing errors related to unsatisfactorily high voltage supply levels.

The main objective is to design and implement a minimum delay reconfigurable filter design that combines MP multiplier with an error-tolerant DFS technique based on razor flip-flops. This deals with the study, design and implementation of multiprecision array multiplier with parallel processing. Architecture of fir filter based on partial reconfiguration is designed here. Hardware Implementation of this system has been done on virtex5 Board.

III. Reconfigurable FIR Filter Design

The FIR filter calculates an output from a group of input samples. The group of input samples is multiplied by a group of coefficients and then added together to generate the output as shown in Fig. 1. Realization of FIR filters can be done in either hardware or software .A software implementation would involve sequential execution of the filter functions while hardware implementation of FIR filters permits the filter functions to be processed in a parallel manner, that enhances processing speed but less flexible for changes. Thus, the proposed system offers both the flexibility of computer software and the capability to create custom high performance systems.

Fig. 2 shows the partial reconfigurable m n order FIR filter that comprises of m n order filter modules and right side module which has m filter modules, connected by bus macros on FPGA. Each filter module comprises of n/2 reconfigurable multiply-accumulate (rMAC) unit, which can be implemented through serial-to-parallel registers to get coefficient inputs in a sequential manner.

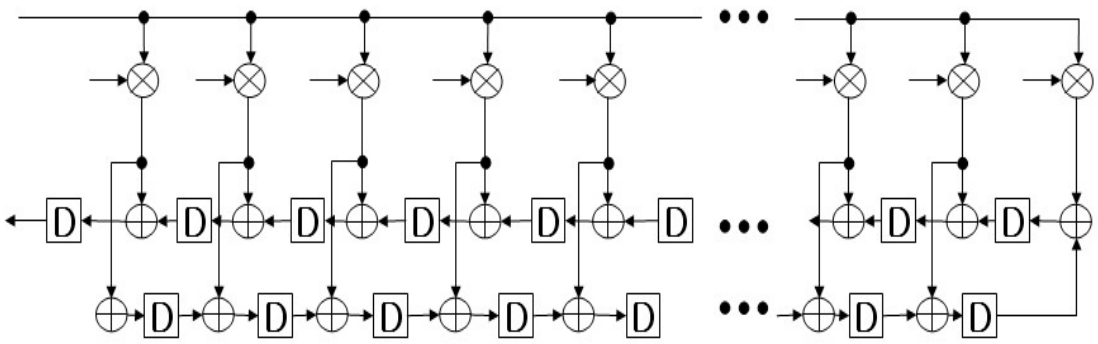

Fig.1. N-tap transposed FIR filter

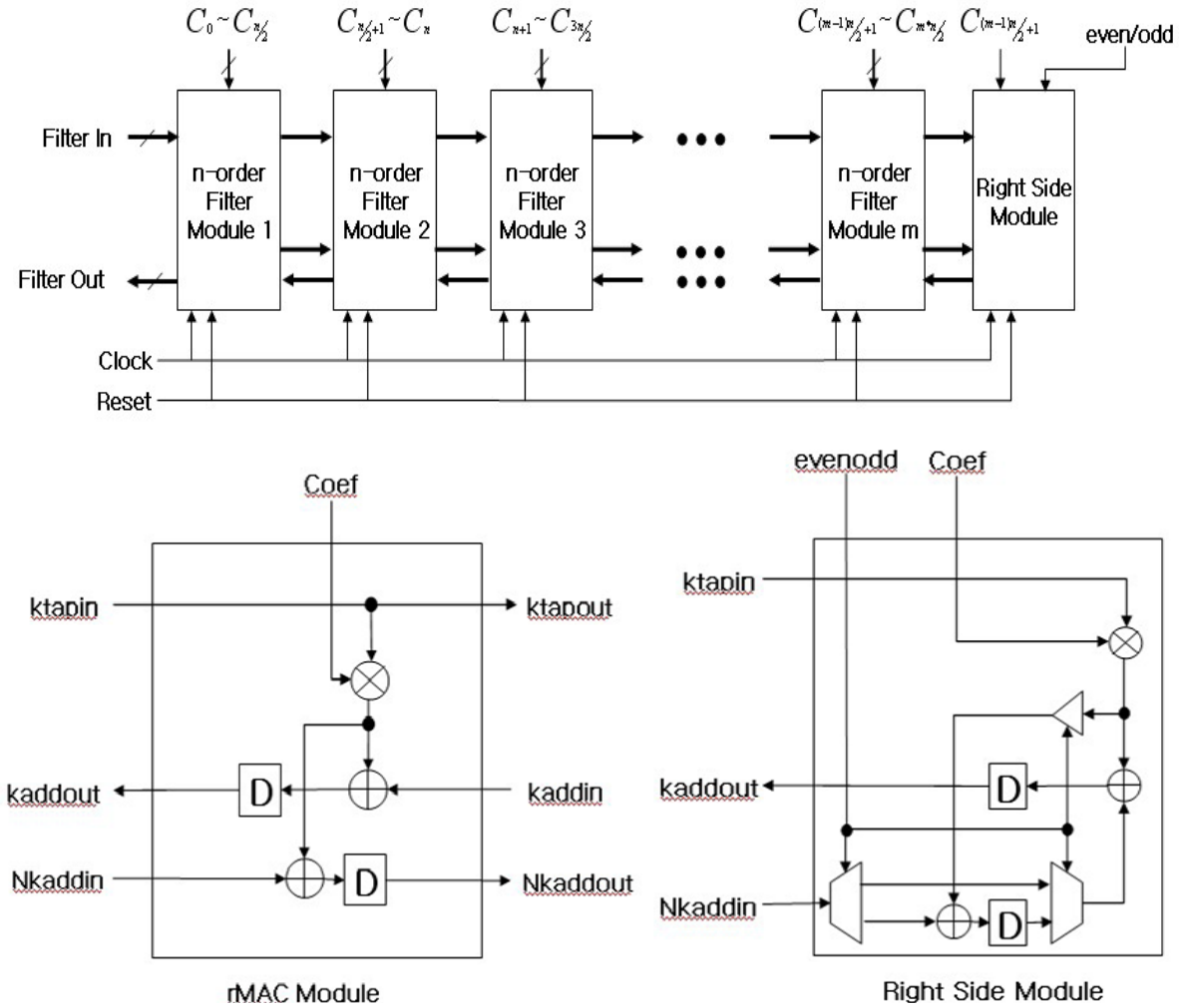

Fig.2. Block diagram of (a) partial reconfigurable m n order FIR filter, (b) reconfigurable multiply-accumulate (rMAC) modules

IV. Dynamic Frequency Scaling Unit

In the proposed system, dynamic frequency tuning is used to obtain throughput requirements. The output frequency can be scaled up from 5 to 50 MHz using three control bits (5 MHz/step). This frequency range is chosen to obtain the requirements of common purpose DSP applications. For 5–50 MHz operating range, the filter increases up to 4 × 50 = 200 MIPS.

The system has building blocks that can either work as four independent 8*8 multipliers or work in parallel to execute one or two 16 × 16 bit multiplications or a single-32 × 32 bit operation. Parallel processing can be used to enhance the throughput or lessen the supply voltage level for low power operation.

A clock signal is required for sequential circuits to operate. Generally the clock signal generates from a crystal oscillator on-board. The oscillator built on FPGA boards usually ranges from 50 MHz to 100 MHz. A simple circuit that can divide the clock frequency by half is shown below.

Assume clkdiv is high initially. As din inverts the signal clkdiv, din is initially low. When the first rising edge of clock arrives, clkdiv is updated by the current din value and changes to '0'. As soon as clkdiv changes to '0', din will be pulled up to logic '1' by the inverter. When the next rising edge of clk occurs, clkdiv will change to logic '1' and din will change back to '0' after the propagation delay of the inverter. The waveform of the circuit is shown below. As a result, the period of clkdiv (the time between two adjacent rising edges) doubles the period of clk (i.e., the frequency of clkdiv is half of the clk frequency). With this circuit, we can actually divide the clock by cascading the previous circuit.

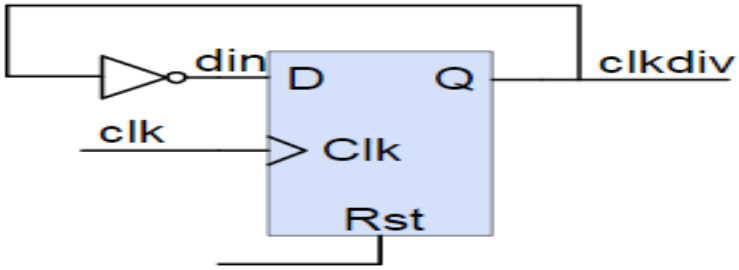

Fig.3. Clock Divider

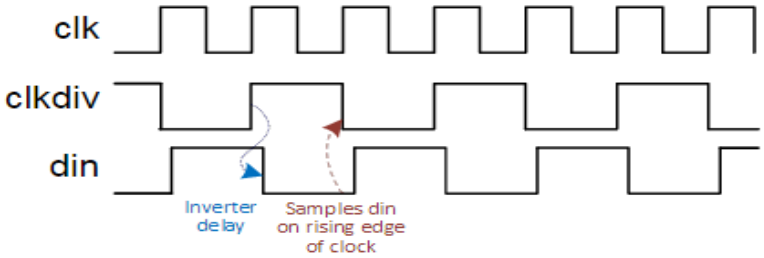

Fig.4. Waveform of Clock Divider

V. Implementation Of Razor Flip-Flops

The razor technology removes the safety margins by obtaining variable tolerance through in-situ timing error detection and rectification capability. The proposed technique is based on a razor flip-flop, which identifies and rectifies delay errors by a technique called double sampling. It involves a razor flip-flop whose figure is shown below. It operates as a standard positive edge triggered flip-flop that also include a shadow latch that samples at the negative edge of that clock. Hence, the input data is given during the positive clock edge to settle down to its proper state before being sampled by the shadow latch. The minimum permissible supply voltage has to be fixed, such that even for the worst case scenarios the shadow latch always clocks the correct data. This requirement is fulfilled given that the shadow latch is clocked later than the main flip-flop. A comparator detects a timing error when it identifies a difference between the data sampled at the main flip-flop and the accurate data sampled at the shadow latch.

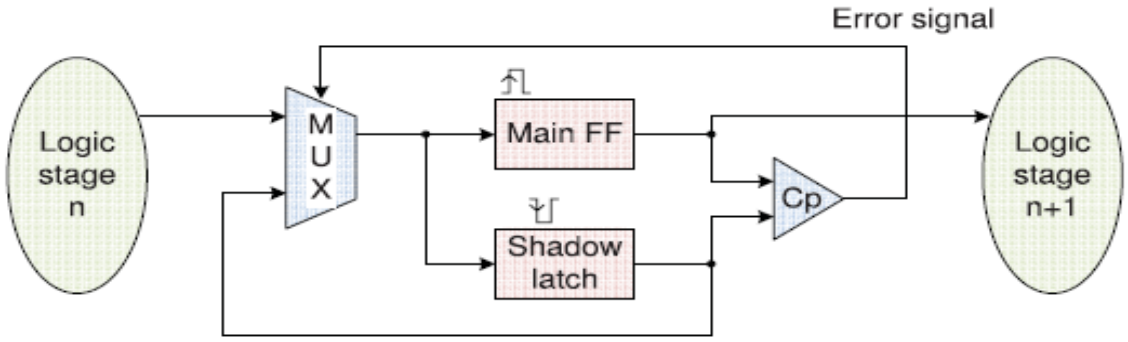

Fig.5. Architecture of Razor Flipflop

The correct signal would consequently overwrite the incorrect signal. The theory behind razor flip-flops is that if an error is identified at a given pipeline stage N, then operations are only re-executed through the subsequent pipeline stage N + 1. This is feasible because the correct sampled value would be stored by the shadow latch. This technique made sure that forward progress of data through the complete pipeline at the cost of a single-clock cycle. An error detection technique, based on global clock gating can be realized. In this correction technique, error and clock signals are used to decide when the entire pipeline has to be delayed for a single clock cycle.

When an error happens, results can be recomputed at any pipeline stage by means of the subsequent input of the shadow latch. Hence, the correct data can be forwarded to the subsequent next stages. Given that all stages can perform these recompilations in parallel, the adopted global clock gating can endure any number of errors within a given clock cycle. Normal pipeline operation can resume after one clock cycle. The actual

realization of razor flip-flops requires careful designing to achieve timing constraints and avoid system failure. For example, the use of a delayed clock for the shadow latch may create a short-path in the combinational logic to corrupt the data in the shadow latch. This can result in a short-path delay constraint at the input of each razor flip-flop.

VI. Input Operands Scheduler

In some technologies such as artificial neural networks, the input data stream may involve mixed-precision operands. While our multiplier includes three different precision modes (16 × 16 bit, 8 × 8 bit, 4 × 4 bit), the supply voltage have to transmit dynamically and moreover, these transitions may not always be achievable within one clock cycle. To minimize the overall delay, an IOS that is introduced which reorganize the input data stream such that same-precision operands are grouped together into a buffer
The block diagram of the IOS is shown below.

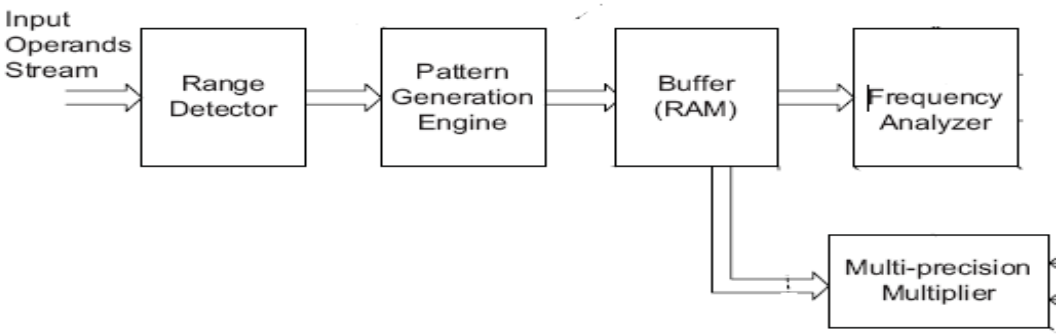

Fig.6. Architecture of IOS

It involves an operand range detector, a pattern generation engine and a buffer-(RAM).The scheduler operates as follows. The inputs operands are first supplied to the range detector, which arranges them according to their precision: 16, 8 or 4-bit. The data is then organized by the pattern generation engine, which arranges same-precision data into three different 16-bit data patterns: 1) pattern 1 corresponds to original 16-bit input operand data; 2) pattern 2 combines two 8-bit operands data and 3) pattern 3 combines four 4-bit operand data. At every clock cycle, a 16-bit data pattern can be executed, due to the parallel processing ability of the proposed system and thus providing the MP and PP capability into real effect. The three different data patterns are grouped and stored into a buffer along with the respective clock frequencies at which they should be processed.

VII. Performance Evaluation

This paper implemented a 16 × 16 bit reconfigurable filter. The operating mode of the system is controlled by three external signals.

The operating frequency is tuned automatically by design depending on the actual workload of the system. The design is tested by giving in randomly generated operands. The various precision data samples include data with an effective word-length of 4, 8 and 16 bits.

The design provides complete functionality across a frequency range of 5–50 MHz. Energy savings due to razor technology achieved from the removal of safety margins. As a result of parallel processing, the operating frequency can be reduced to 1/3 of the original one; hence the voltage can be reduced. The proposed scheme ensures the most reconfigurability while also providing the minimum relative area. The proposed design requires a much lesser area when compared with the designs with the same maximum word-length.

Therefore this paper shows a realization that not only provides multiprecision reconfigurable data path, but also achieves a reduction in both area and delay, as compared with fixed width multipliers.

Table 1. Comparison Of Various Architectures With Proposed Architecture With Respect To Delay.

ARCHITECTURE	DELAY (ns)	FREQUENCY (MHz)
K. Gunasekaran,et al.,[17]	36.196	Nil
J Britto Pari,et al., [19]	19.618	50.973
Proposed	5.230	191.196

Table 2. Comparison Of Various Architectures With Proposed Architecture With Respect To Area .

ARCHITECTURE	SLICE	LUT
Yeong-Jae Oh,et al., [11]	4,733	8,427
Proposed (multiprecision)	2,010	2,211
Proposed (single precision)	9,74	1,029

For dynamic partial reconfiguration implementation, the partial reconfigurable module1 and module2 were realized as bypass module and 4-tap module respectively. For verification, two methods had been performed. The 20-tap FIR filter and 20-tap reconfigurable FIR filter had been simulated on FPGA test board using Xilinx ChipScope Pro Analyzer to verify that both the output results are same. This result describes that module2 is reconfigured partially from 14-tap module to bypass module. For performance evaluation, we have designed FIR filter using variable multipliers. Table 1 shows the utilization of slice, LUT and delay after technology mapping. The proposed novel adds flexibility and hence achieving dynamically inserting and/or removing the coefficient taps.

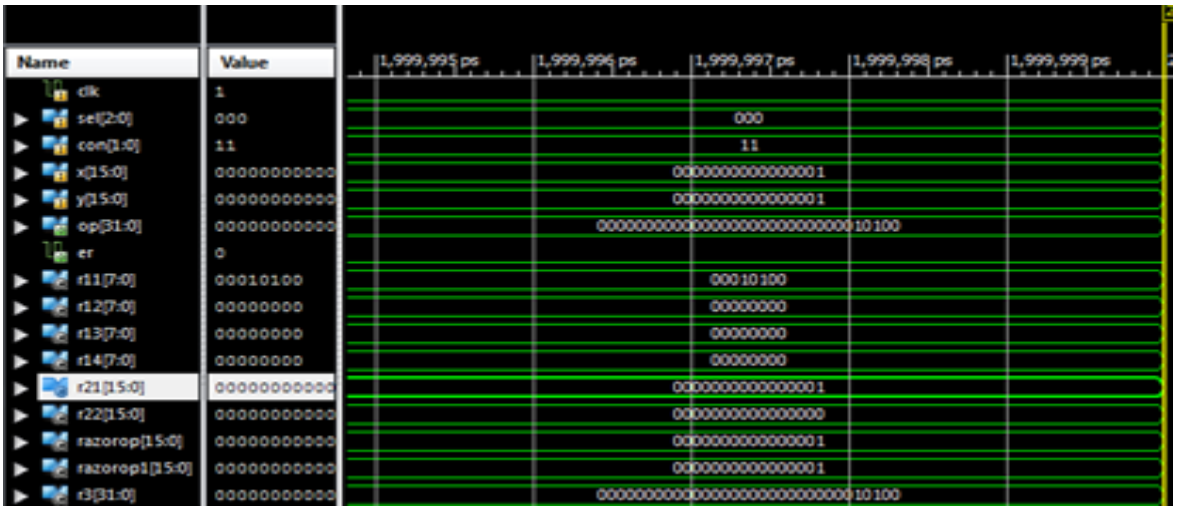

Fig.7 Reconfigurable Fir Filters With Four 4- bit Multipliers

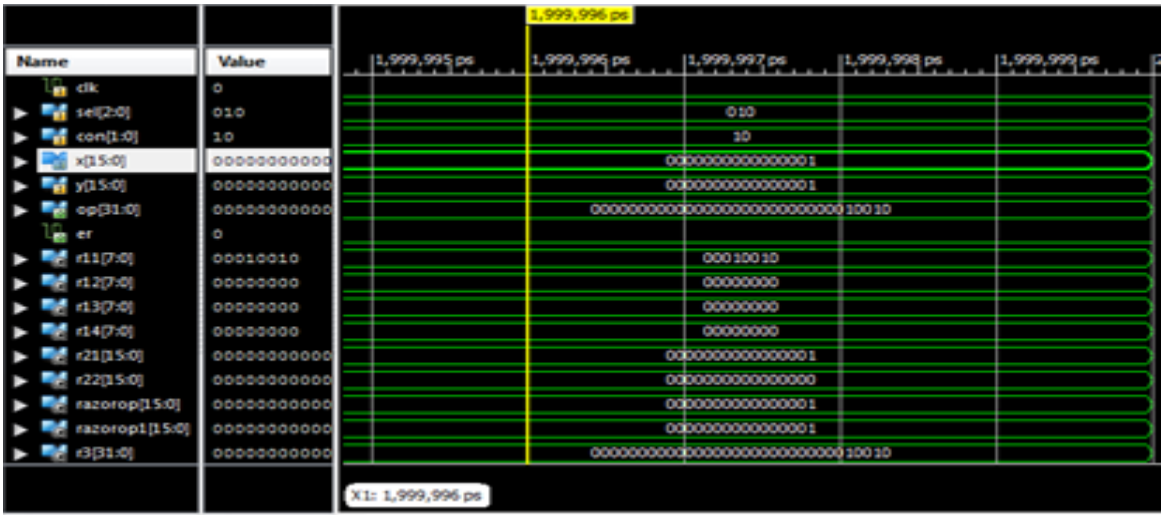

FIG 8. Reconfigurable Fir Filters With 0ne 16-BIT Multiplier

VIII. Conclusion

This paper introduces a FIR filter design using partial reconfiguration, which provides area efficiency, flexibility and frequency improvement by inserting and/or removing the partial modules dynamically. The proposed technique also provides a reduction in hardware cost and thereby allows performing partial reconfiguration. In future applications, self-reconfigurable hardware platform is a promising solution for digital circuit in the run-time environment.

When combining this MP multiplier architecture with an error-tolerant razor-based flip flops, dynamic frequency scaling and the proposed operands scheduler, total delay reduction was obtained with a negligible silicon area overhead which can be reduced by reconfigurability. The design achieves run-time adaptation to the actual workload by processing at the minimum clock frequency while meeting throughput requirements. The dedicated operand scheduler rearranges input operands, thereby reducing the number of transitions of the supply voltage and, in turn, minimized the overall delay of the system. The proposed system provided a solution toward enabling full computational flexibility for various general purpose low-power applications.

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