IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 5, Issue 3, Ver. I (May - Jun. 2015), PP 28-32
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and Implementation of Low power Carry Select Adder Using Transmission Gate Logic

Chandan Kumar Ray[1], K.Srinivasarao[2.]
[1,2.] *(ECE Mewaruniversity, India)*

Abstract : *Now A days power Reduction techniques play important Role in Low power VLSI Applications. Adder is digital circuit it performing addition operation used in many application like microprocessor and DSP In this paper Low power XOR gate has been designed using transmission gate logic, it is implemented carry select adder for low power VLSI application and compared with CMOS technology . The simulation is performed using a SPICE circuit simulator at 180nm technology node & 1.8V standard CMOS process. Comparison between these techniques has shown a significant power saving to the extent of 60% in case of Transmission gate logic design carry select adder , as compared to CMOS logic in 10- 100MHz transition frequency range.*

Keywords - *Adder, carry select Adder , Mux , T_SPICE , XOR gate*

I. Introduction

The increasing demand for Low power VLSI Application at Different Level like Circuit level, Architectural and Layout such way that low power reduction requirement plays very important role for portable devices and heat generated systems. Carry select adder is fast adder compared with other adder like ripple carry adder , carry save adder, carry skip adder but area is somewhat increased as compared with others. Now a days major problem is power dissipation and delay in ADDERS . So In this paper used transmission gate logic adder to achieve low power and less delay .

The proposed circuit is the transmission gate logic XOR gate further implemented into 1_ bit carry select adder ,4_bit carry select adder and performance parameters like power, delay & power delay product were observed. Also it is compared with conventional CMOS logic circuit. Performance parameter curves shows that proposed circuit is efficient for low power application.

This paper has been classified into six sections. Section II describes the working of XOR gate . Section III describes operation of 1_bit carry select adder Section IV describes 4_bit carry select adder Section V and VI are about simulation results and conclusion respectively

II. XOR Gate Designed Using Transmission Gate

When the two input are in one or zero at that time output is Zero and Reaming condition it is one from the figure 2.1 designed transmission gate , here total 8 transistor is used to achieve XOR gate function , In the case of CMOS technology 22 transistor used, for XOR gate function. From the graph 5.2 As we increased frequency power dissipation also increased . but In the case of transmission gate based XOR got the less power dissipation

Truth table 1.1

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

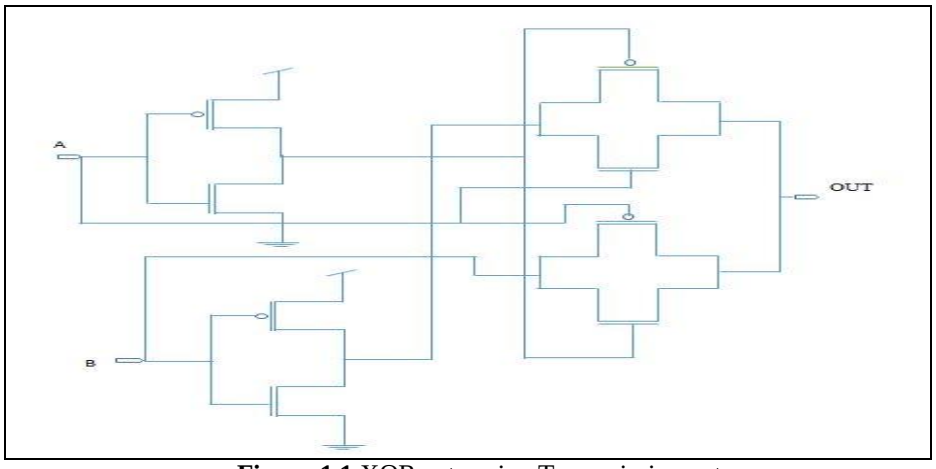

Figure 1.1 XOR gate using Transmission gate

III. Bit Carry Select Adder Designed Using Transmission Gate Based XOR Gate

In digital electronics adder is a digital circuit that performs addition of numbers, here 1_bit full adder performing addition operation of three input bit and it is designed using two half adders. Carry select adder is designed with two Adder, if carry one selecting one adder and carry zero selecting another adder, In this way delay of carry select adder reduced compared with Normal Ripple carry select adder. But area is increased .From the graph 5.3, by using transmission gate logic circuits getting less power dissipation compared with CMOS technology.

Truth table

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. Bit Carry Select Adder Designed Using Transmission Gate Based XOR Gate

The carry-select adder play important role to reduce the carry propagation delay. One for an input carry of logical zero and one for an input carry of logical one.

From the Figure 4 4_bit Addition operation is performing depending on input signal zero (or) one Adders are selected and finally based on multiplexer select line output sum and carry will be generated simultaneously. Due to this carry select adder speed of operation increased at the cost of doubling area.

From the Figure 5.6 it may be observed that as frequency increases, power dissipation of both the 4_bit carry select adders are increases whereas Transmission gate logic 4_bit carry select adder have lesser power dissipation at every frequency in comparison to conventional CMOS.

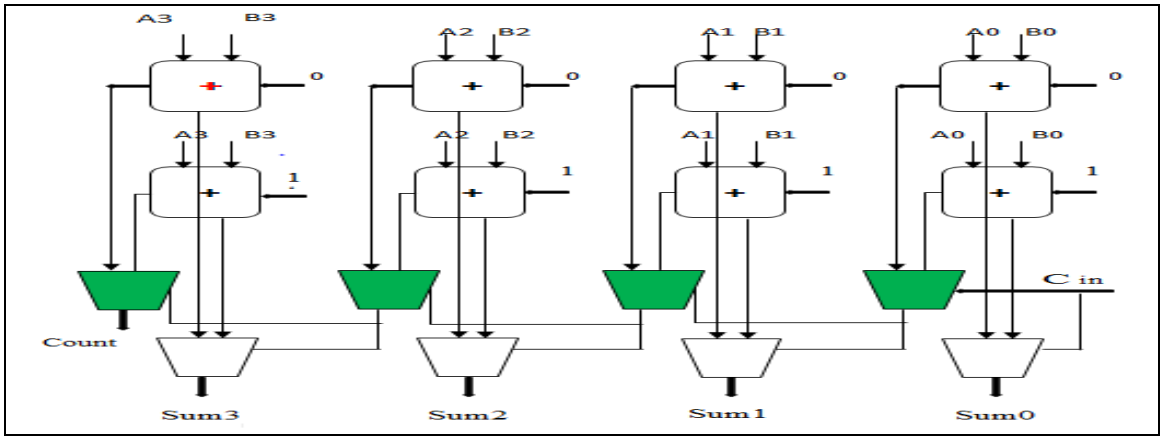

Figure 4 _bit carry select Adder

V. Simulation Results And Discussion

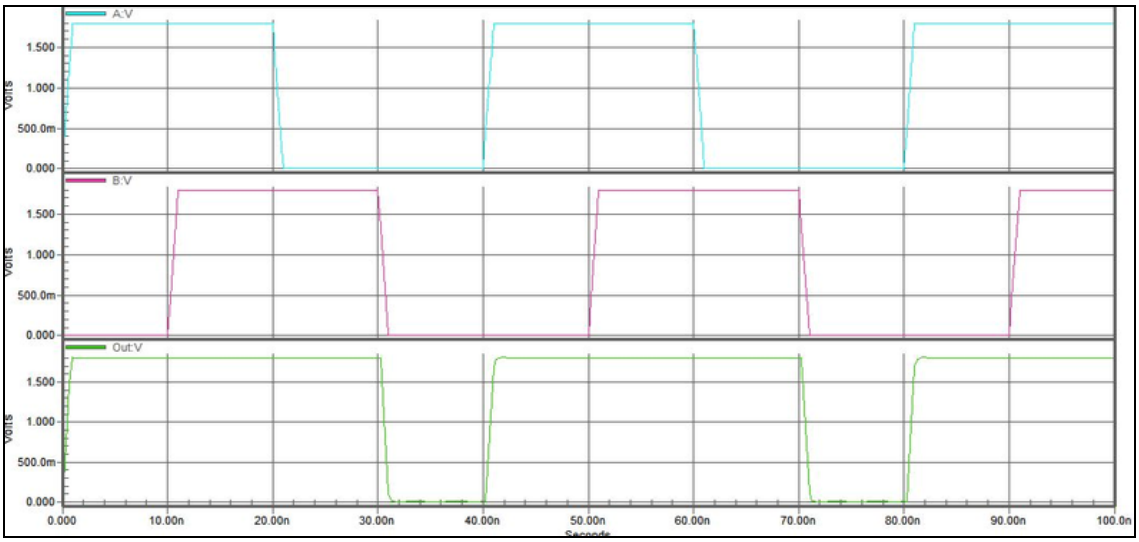

Figure 5.1 Xor Gate designed using transmission gate Output

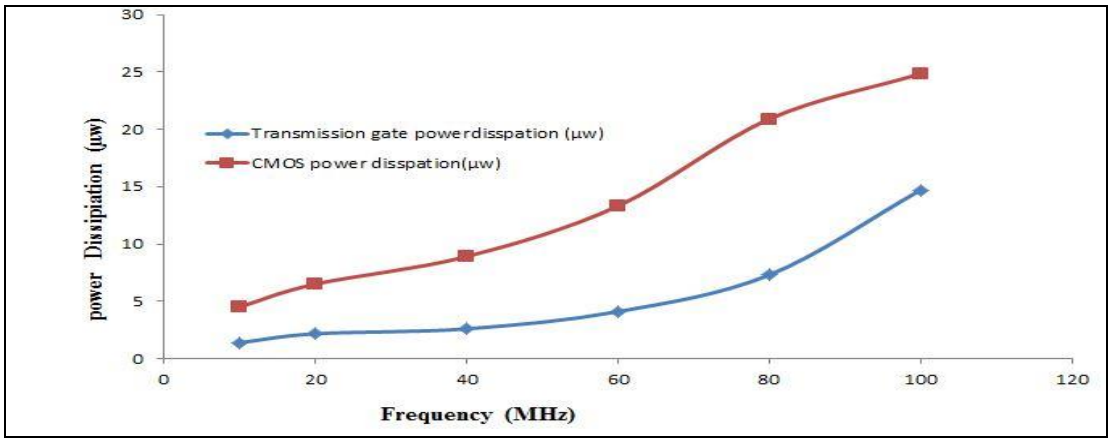

Figure 5.2 Xor Gate designed using transmission gate Frequency versuse powerdissipation

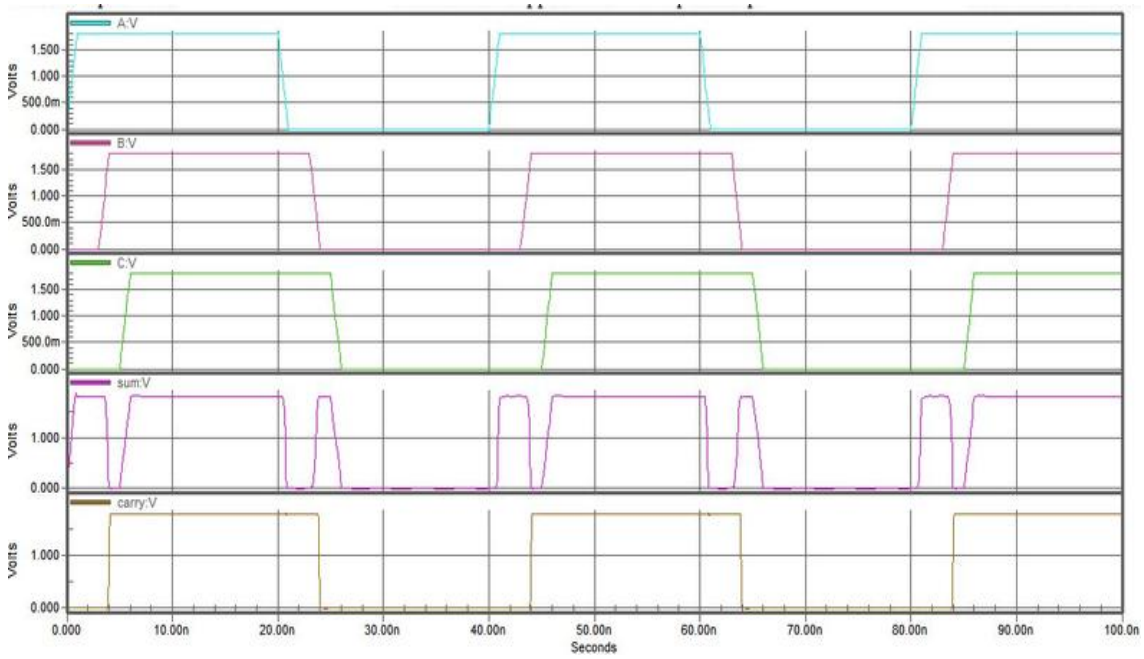

Figure 5.3 1_bit full adder using transmission gate output

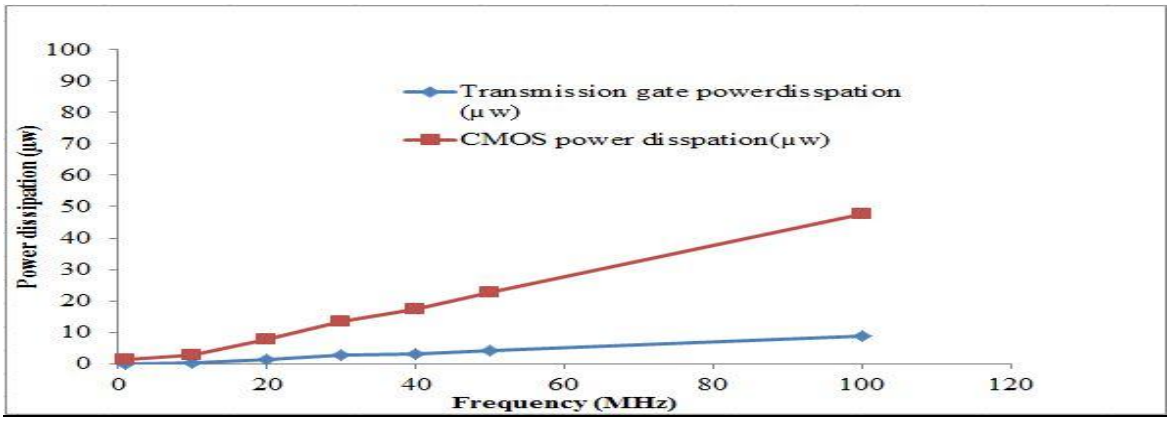

Figure 5.4 1_bit full adder using transmission gate Frequency versus powerdission

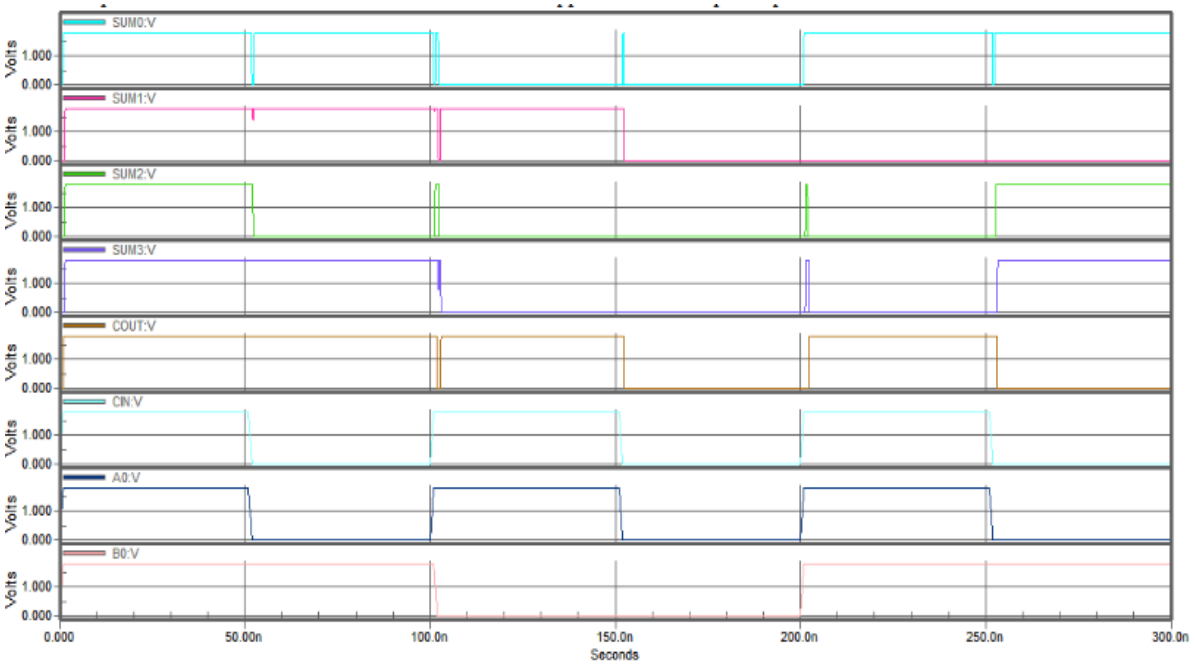

Figure 5.5 4_bit Carry select adder using transmission gate Output

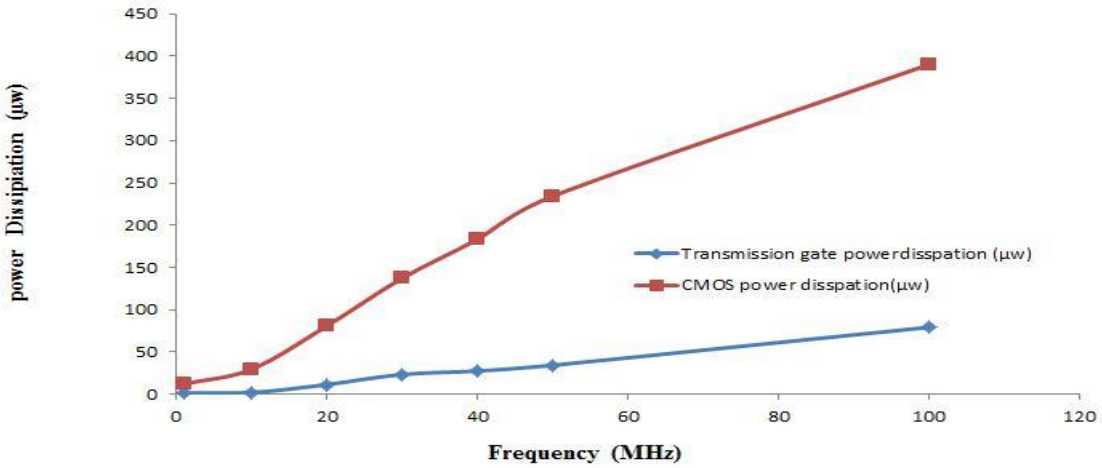

Figure 5.6 4_bit carry select adder using transmission gate Frequency versuse powerdissipation

VI. Main Conclusion

From the Simulation Result ,the Transmission Gate based XOR , 1_bit full Adder and 4_bit Carry select Adder have got Powerful validation & wide acceptance for low power digital circuits at average frequency. The comparison of the transmission gate based circuit with CMOS has proved that power consumption of the Transmission gate based circuits is far less as compared to CMOS based techniques. The Transmission gate based XOR , 1_bit carry select adder and 4_bit carry select adder dissipate minimally as only 19 % & 33% power of the total power of a static CMOS based logic circuit.so that it is clear cut indication that transmission gate based circuits is very promising and power efficient technique especially for low power digital circuits

References

[1]. Chandrakasan, A.,Brodersen,"Low Power Digital Design",Kluwer Academic Publishers, R., 1995.
[2]. Low power cmos VLSI circuit design Kaushik Roy,sharatc.prasad copy right @2000 by john Wiley Sons Inc
[3]. AtulKumarMaury & Gagnesh Kumar, Energy Efficient Adiabatic Logic for Low Power VLSI Applications, 2011 International Conference on Communication Systems and Network Technologies.
[4]. Shipraupadhay,R.AMishra,RKNagari,andSPSingh,DiodefreeAdiabaticlogiccircuits,hindawanipublishedcorporationsISRNElectronicsVolume2013,ArticleID 673601.
[5]. O. J. Bedrij, "Carry-Select Adder", IRE Transactions one Electronic Computers, pp. 340–346, June 1962.
[6]. Arvind Kumar, Anil Kumar Goyal, Study of Various Full Adders using Tanner EDA Tool. IJCST Vol. 3, Iss ue 1, Jan. - March 2012
[7]. N. Waste and K. Eshraghian, Principle of CMOS VLSI Design: System Prospective, 2nd New York: Addison – Wesley, 1993.
[8]. W. C. Athas, L. J. Svensson, J. G. Koller, "Low- power digital systems based on Adiabatic, switching principles" IEEE Trans. On VLSI systems, 2(4), Dec. 1994, pp: 398-407.