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Comparative Analysis of Multiplier in Quaternary logic

Shweta Hajare[1], Dr.P.K.Dakhole[2]
[1](*Research scholar:Dept. of Electronics Engg ,Yeshwantrao Chavan College of Engg Nagpur, India)*
[2](*Professor:Dept. of Electronics Engg Yeshwantrao Chavan College of Engg Nagpur, India)*

Abstract : *Multiple Valued Logic (MVL) has some important benefits such as increased data density, increased computational ability, reduced dynamic power dissipation Therefore with the help of Multiple Valued Logic (MVL) we have designed two quaternary multiplier architecture. The partial products in the multiplier are designed with quaternary voltage mode circuits. Each multiplier architecture is designed with two methods. The performance of two quaternary multiplier architecture is then compared based on Energy delay product (EDP) & Power delay product (PDP) . Comparison of these multiplier is done based on the analysis for power delay & area*

Keywords - *Multiple Valued Logic (MVL)* **,** *Quaternary logic, NMIN, NMAX*

I. Introduction

In many practical application such as digital signal Processing, arithmetic processor, FIR filter multiplier plays important roll. In case of digital system performance is generally evaluated by the performance of the multiplier . Many researchers with advances in technology, have tried to design multipliers which offer high speed, low power consumption, regularity of layout. Arithmetic processors constitute another important example, where multiple-valued data representation provides additional conceptual and implementational flexibility. Alternatively, MV, for multiple-valued view, presents the system as multiple-valued or as having multiple-valued segments, which in turn (internally) may have binary parts. Researchers in VLSI design, mainly concentrate on area, speed and power dissipation. The type of high speed multipliers are Booth multiplier, Parallel multiplier, Braun multiplier. In the conventional multiplier, the number of partial products to be added are determined by the number of bits the multiplier or multiplicand being used. As the number of bits in the multiplicand or the multiplier increase, the longer time it takes to produce the product. Digital multiplication is the process where two binary numbers, the multiplier and the multiplicand are combined into the result forming a series of bit shift and bit additions. There are different types of multipliers available depending upon the application in which they are used. Conventional array multiplier is based on regular full adder in which multiplication is obtained by partial product method. In a digital system an array multiplier involves the parallel multiplication, which is done in the following three steps:

1. Generation of partial product (PP) bits.
2. The accumulation of partial product (PP) bits into two rows.
3. The computation of final product using Full adder .

Partial product bits of the multiplicand and multiplier are produced by PP (partial product) generation . PP reduction is used to compress the partial product bits to two. In Multiplication product of two bits produces an output which is twice that of the original bit. For reduction of area cost it is needed to truncate the partial product bits to the required precision .This paper is organized as first part consist of basic circuit of quaternary logic which are used to design multiplier. Second part is based on the designing of multiplier architecture. Third part is based on the analysis of multiplier architecture & conclusion.

II. Background

In recent years, Multiple-valued Logic (MVL) circuits have been attracting researchers in VLSI technology, the reason behind the fact that some synonymous with many-valued logic (MVL) is the study of theory and application of logics, where the classical truth values ”true” and ”false” are replaced by infinitely many values. There are mainly two kinds of MVL circuits based on MOS technology, namely the current mode MVL circuits and the voltage-mode MVL circuits. A quaternary (radix-4) logic system allows for the use of relatively simple encoding/decoding circuits to be employed for interfacing to binary logic since radix $4=2^2$. In quaternary -valued logic signals easily interface with the binary world they may be decoded directly into their two-binary-digit equivalent with MVL .Many logical and arithmetic functions have been efficiently implemented with fewer operations, gates, transistors, signal lines, etc are required. In binary logic {1,2}, the conversion from binary to binary coded decimal or the inverse, could be done easily since we behave only with

simple numbering set {0,1}. In higher valued logic [3,4,5] such as ternary {0,1,2}, quaternary {0,1,2,3} and quinary {0,1,2,3,4}, the matter of conversion becomes different and done in a very difficult way . The base radix for the work is Quaternary logic (radix-4-valued) quaternary logic offers all the benefits of MVL such as reduced area due to signal routing reduction along with the important advantage of being able to easily interface with traditional binary logic circuits.[2][3]

III. Quaternary Circuit Design

This circuit is a CMOS circuit operates with four voltage levels corresponding to 0V and other three power supply lines of 1V, 2V and 3V.

3.1 NMIN gate

In quaternary logic, binary NAND gate is replaced by NMIN gate & AND gate is replace by MIN gate [4][12]. The MIN operation sets the output of the MIN circuit to be the lowest value of inputs. MIN gate is equal to AND gate in binary. NMIN gate is not of MIN gate. In binary AND gate, minimum of two inputs of the gate are chosen at the output. NAND gate is not of AND gate. Similarly in quaternary logic gates minimum of two inputs are chosen for MIN gate. NMIN circuit is combination of the inverter and a common binary AND circuit.

3.2 NMAX/MAX Gate

In quaternary logic, binary NOR gate is replaced by NMAX gate & OR gate is replaced by MAX gate [4][12]. NMAX gate is not of MAX gate. The MAX operation sets the output of the MAX circuit to be the largest value of inputs. OR gate in binary is equal to MAX gate in quaternary. NMAX gate is not of MAX gate circuit. The MAX gate is a circuit of multiple inputs and sets the output in the higher value of all entries. NMAX circuit is combination of the inverter and a common binary OR circuit.MAX circuit is by adding one inverter at the output of NMAX gate .

IV. Quaternary Multiplier Architecture

Basic multiplication can be realized by the shift add algorithm by generating partial products and adding successive properly shifted partial products. Thus multiplication is proportional to the number of partial products to be added [1]. In all multiplier circuits, two types of adder cells are present. They are half adder and full adder. Output of the multiplier is shown in Table 1.The high speed techniques is essential for the adder to work in high speed, implementing the adder in any one of the way. Delay of the circuit depends on the number of inversion levels. Circuit size depends on the number of transistors in the circuit. Multiplication is the one of the most important function carried by ALU. To carry out mathematical high speed operations, most advanced digital systems incorporate a parallel multiplication unit . Multipliers are used in arithmetic logic unit in case of microprocessor. A digital signal processing system requires multipliers to implement algorithms such as convolution and filtering. For the design of multipliers three important criteria are the chip area, speed of computation and power dissipation.

4.1 Quaternary Serial Multiplier

Serial multiplication is the process of computation of the partial product and summing the partial product together. Serial multiplier are simple in architecture because both the operand enter serially. Quaternary ripple carry adder based multiplier consist of multiplicand SISO shift register, multiplier SISO shift register, product SISO shift register, single digit multiplier, an array of HA cells configured in a carry ripple organization . The speed of operation of serial multiplier is slow because of operand entering serially. In Quaternary ripple carry adder based multiplier the partial product accumulation operation is serial, because after *n* iterations final product is available where *n* is the maximum number of digits in each operand. In Quaternary ripple carry adder based multiplier after each clock cycle multiplier digit is multiplied with multiplicand value with the help of single digit multiplier ,the result of this multiplication is then added to the partial product, the partial product is then stored in partial product register, partial product shift register shift the partial product after every clock cycle. Quaternary RCA multiplier structure is then implemented with carry look-ahead adder as shown in Fig 1 .Then comparative analysis of Quaternary ripple carry adder based multiplier & quaternary carry look-ahead multiplier is done based on power & area as shown in fig.4 & fig. 5

Table I. Truth Table Of Quaternary Multiplier

C	B	A	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	0	2	0	2
0	0	3	0	3
0	1	0	0	1
0	1	1	0	1
0	1	2	0	2
0	1	3	0	3
0	2	0	0	0
0	2	1	0	2
0	2	2	1	0
0	2	3	1	2
0	3	0	0	0
0	3	1	0	3
0	3	2	1	2
0	3	3	2	1
1	0	0	0	1
1	0	1	0	1
1	0	2	0	1
1	0	3	0	1
1	1	0	0	1
1	1	1	0	2
1	1	2	0	3
1	1	3	1	0

C	B	A	CARRY	SUM
1	2	0	0	1
1	2	1	0	3
1	2	2	1	1
1	2	3	1	2
1	3	0	0	1
1	3	1	1	0
1	3	2	1	3
1	3	3	2	2
2	0	0	0	2
2	0	1	0	2
2	0	2	0	2
2	0	3	0	2
2	1	0	0	2
2	1	1	0	3
2	1	2	1	0
2	1	3	1	1
2	2	0	0	2
2	2	1	1	0
2	2	2	1	2
2	2	3	2	0
2	3	0	0	2
2	3	1	1	2
2	3	2	2	0
2	3	3	2	3

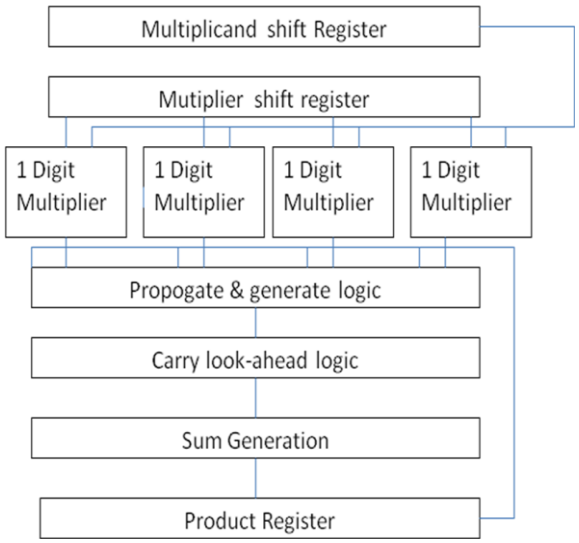

Figure 1: Design of Quaternary CLA multiplier

4.2 Quaternary Combinational Array Multiplier

In quaternary Combinational array multiplier partial products are generated simultaneously. In quaternary Combinational array multiplier each partial product bit of the multiplication can be computed in parallel. In combinational array multiplier , the array consist of structure of quaternary Half adder & quaternary full adder as shown in Fig 2. Similar to the combinational array we have designed quaternary Braun multiplier as shown in Fig. 3 . Comparative analysis of power & area of Quaternary parallel & Braun multiplier are shown in Fig. 6 & Fig 7. The power delay product (PDP) is calculated by (1) which is the product of average power dissipation and propagation delays. The PDP of serial & parallel multiplier is then compared. The Energy Delay Product (EDP) of the multiplier circuit is measured by (2)

PDP=Power *time (1)

EDP = Average Power Dissipation * (Delay) ^{2} (2)

Fig. 9 & Fig. 10 shows power delay product (PDP) and Energy Delay Product (EDP) of quaternary combinational & serial multiplier .

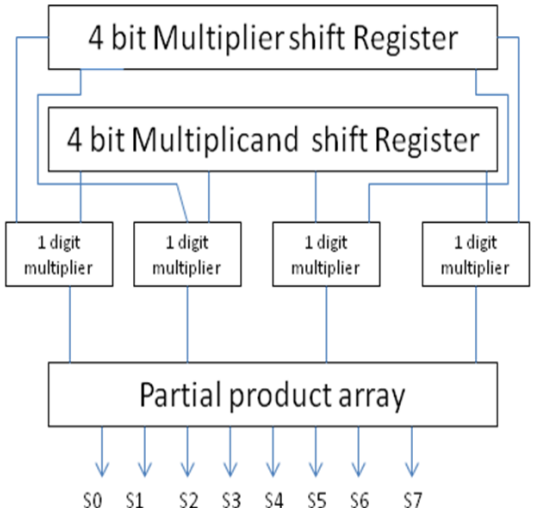

Figure 2: 4 bit Combinational array Multiplier

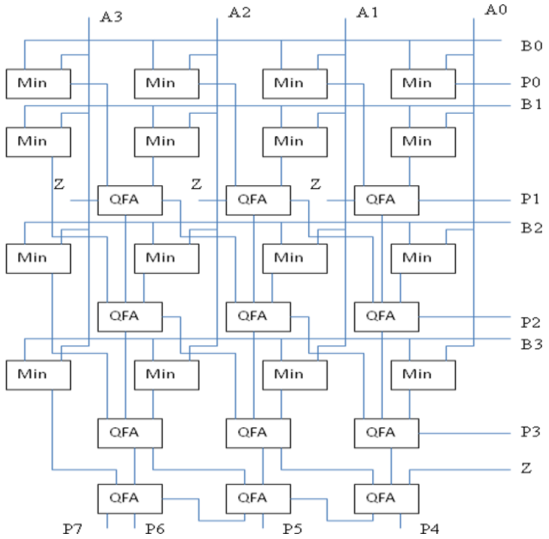

Figure 3: Quaternary Braun Multiplier

V. Result & Conclusion

In this paper we have proposed design of various quaternary multiplier architecture. Simulation of the proposed circuits is carried out for 180nm technology using Tanner EDA tool. Here we proposed comparison of quaternary multiplier in terms of power, area. The analysis result shows that area required for quaternary multiplier is more than area required for binary multiplier, the quaternary multiplier circuits have decreased dynamic power dissipation characteristics and improved timing performance when compared to binary circuits with equivalent word sizes as shown in Fig. 8. In the case of the serial multiplication circuits, an average of 20% more transistors are required for the quaternary implementation. However, the parallel multiplier circuits resulted in a decrease of 14%, 24%, and 33% in transistors respectively for the increasing operand word sizes. Here we have compared binary equivalents for operand word sizes of 8, 16, and 32quaternary digits. The corresponding binary circuits are synthesized using tanner EDA tool for 16, 32, and 64 bit operand word sizes for power dissipation, area. From PDP and EDP graph as shown on Fig. 9 & Fig.10 it is concluded that as compared to serial multiplier quaternary parallel multiplier is fast in speed performance and full-swing This type of multiplier can be used for the design of ALU.

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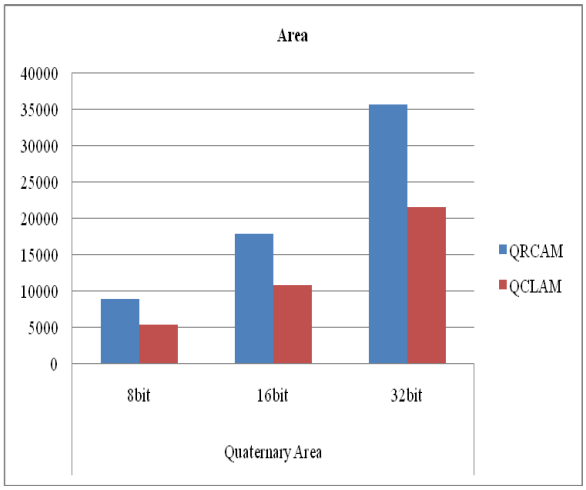

Figure 4: Comparative analysis of area of ` Quaternary serial & Quaternary CLA multiplier

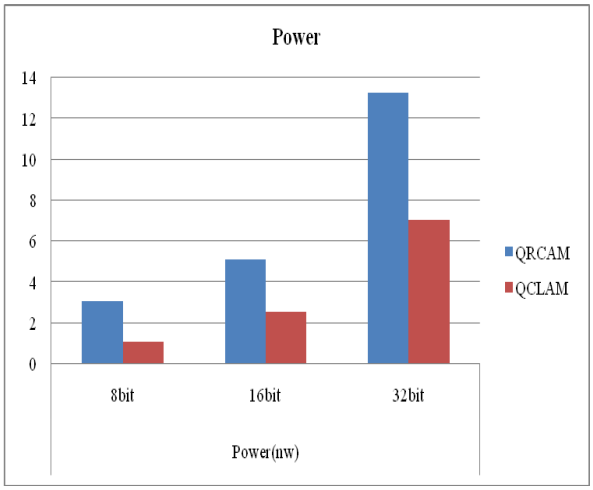

Figure 5: Comparative analysis of power of Quaternary serial & Quaternary CLA multiplier

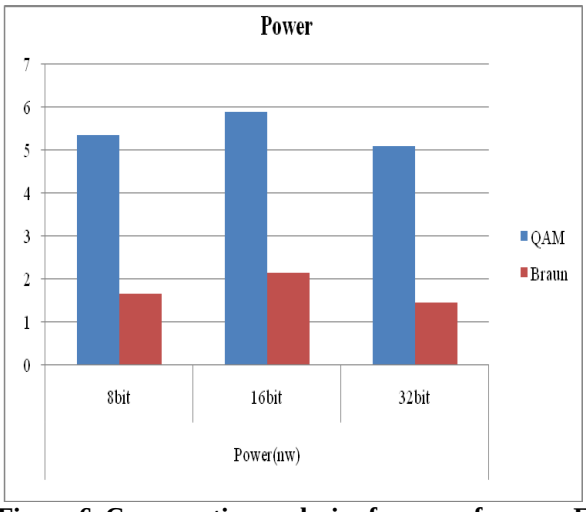

Figure 6. Comparative analysis of power of combinational array multiplier & Braun multiplier

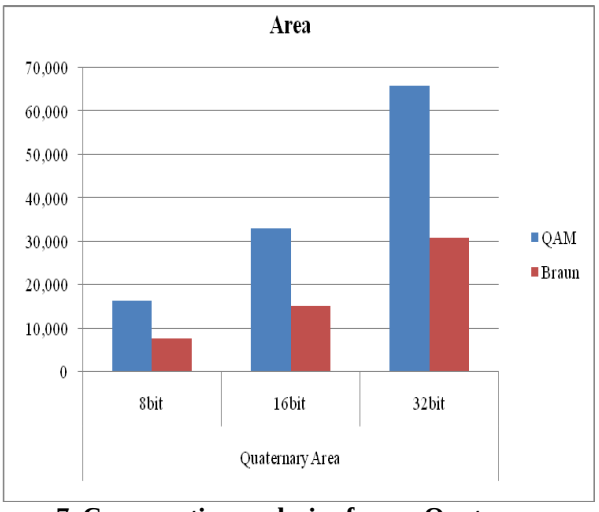

Figure 7. Comparative analysis of area Quaternary of Quaternary combinational array multiplier & Braun multiplier

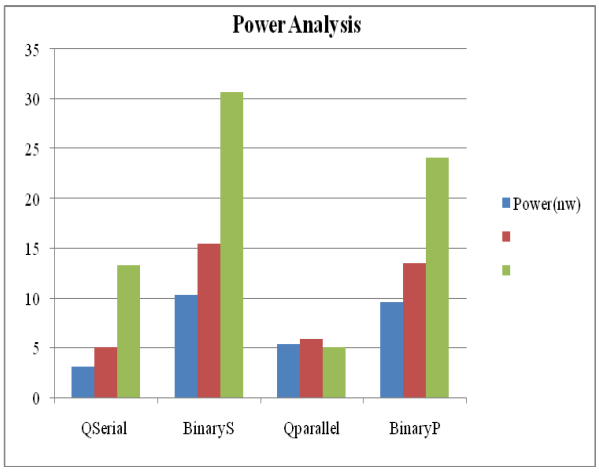

Figure 8. Comparative analysis of Quaternary Serial & binary Serial Qcombinational array multiplier & binary parallel multiplier

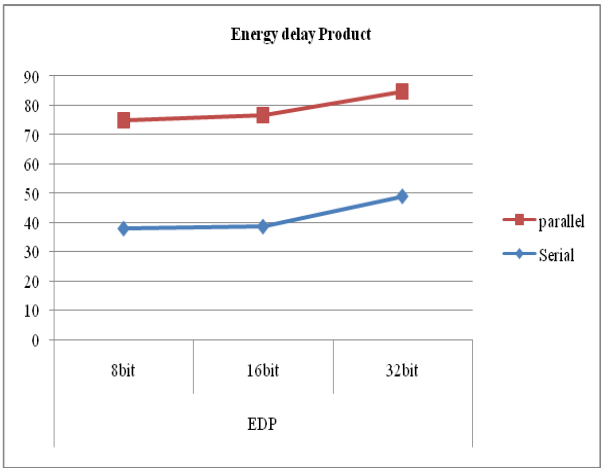

Figure 9. Comparative analysis of Quaternary combinational array multiplier &Q Serial multiplier

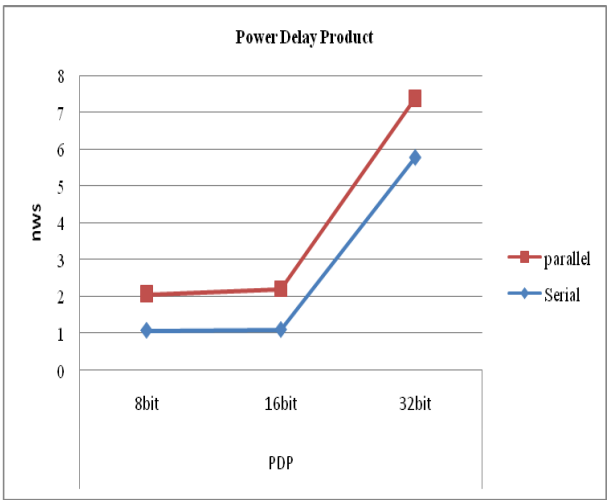

Figure 10. Comparative analysis of Quaternary Serial & Quaternary combinational array multiplier multiplier

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