A Modern Approach for Low Power Dynamic Double Tail Comparator

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Abstract- *Dynamic comparators are widely used in the design of high speed analog to digital converters (ADCs).Clocked comparators are often called dynamic comparators. Dynamic double tail comparators are compared in terms of their power, speed and delay. The accuracy of comparators, which is defined by its power consumption and speed, is of keen interest in achieving over all higher performance of ADCs. In the domain of signal processing with low power VLSI, the role of ADC system is essential. Many high speed ADCs, such as flash ADCs, require high speed, low power comparators with small chip area. The dynamic comparator is based on bipolar CMOS technology. This is the combination of Bipolar and CMOS technology. The Bipolar CMOS circuit offers high speed, high gain and low output resistance, which are excellent properties for high-frequency analog amplifiers and CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates.*

Keywords- *ADC (Analog to Digital converter), CMOS (Complementary Metal Oxide Semiconductor), Flash ADC, Dynamic double tail comparator, Bipolar CMOS.*

I. Introduction

The comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them. Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications such as on-chip high frequency signal testing, data links, sense amplifiers and analog-to-digital converters. On-chip testing of high frequency pseudo random binary sequences (PRBS) requires a high speed comparator at the electrical interface stage.

A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor.

In many applications comparator speed, power dissipation and transistor count are more important. If comparator speed is a priority, the regenerative stage could be designed to start its operation from midway between power supply and ground. Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to digital converters (ADCs), Memory sense amplifiers (SAs) and data receivers. High speed comparators in ultra-deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially, when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. The general trend in CMOS technology is to make the devices smaller and smaller to increase the density and speed of digital circuits. Reduced power supply voltage is normally not an advantage for analog design and a low supply voltage may require some special circuit techniques.

The input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise. The pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain to source resistance due to the continuous technology scaling. The organization of the paper is as follows. In Section II, related works are presented. Section III presents the details of dynamic double tail comparator. Experimental results are reported in Section IV, the conclusions are drawn and the possible future works are described in Section V.

II. Bipolar Sizing Cmos

The proposed design of CMOS comparator based on Low voltage bipolar sizing CMOS technique. We focus to design architecture of CMOS comparator using Low voltage bipolar sizing CMOS technique. That means proposed design of the Comparator design is based on bipolar CMOS technology. This is the

combination of Bipolar and CMOS technology. The Bipolar CMOS circuit offers high speed, high gain, and low output resistance, which are excellent properties for high-frequency analog amplifiers, and CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates. Two voltage/Sources are applied to the designed architecture that compares both inputs and result is the higher source as output. Finally our proposed system provides the reduced delay time and results in low power consumption.

III. CMOS Comparator

CMOS circuits are constructed in such a way that, all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. The input to the A/D converter is a voltage, A/D converters may be designed for voltages from 0 to 10v, from -5 to +5v, etc., but they almost always take a voltage input. In any event, the input is an analog voltage signal for most cases. The output of the A/D converter is a binary signal, and that binary signal encodes the analog input voltage. So, the output is some sort of digital number. A comparator can be used as a simple one-bit A/D converter.
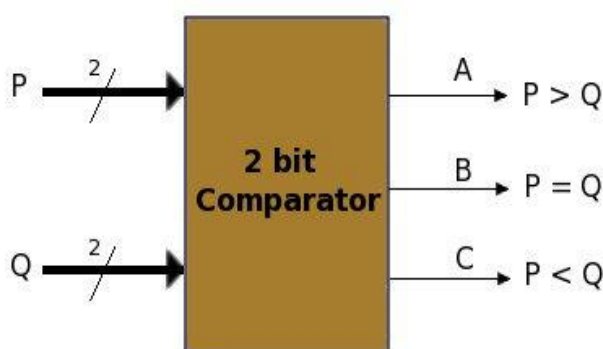
Figure 1: Simple diagram of comparator
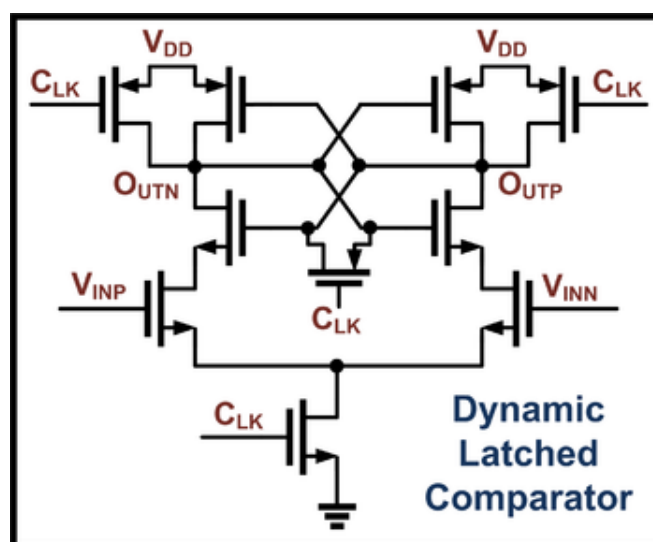
Figure 2: A low power CMOS comparator

A CMOS double tail dynamic comparator was designed from the figure 2. CMOS is a methodology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication.
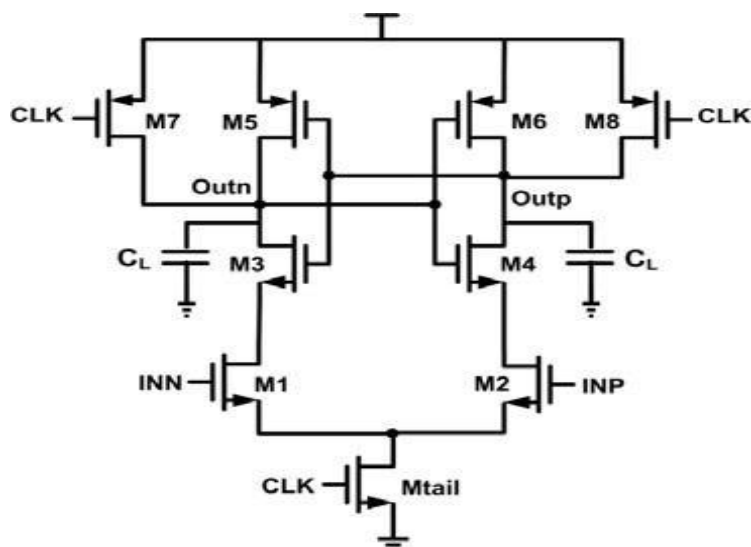
Figure 3: schematic diagram of dynamic comparator

The operation of the comparator is as follows. During the reset phase when CLK = 0 and M tail is off, reset transistors (M7– M8) pull both output nodes Out n and Out p to VDD to define a start condition and to have a valid logical level during reset. After when CLK = VDD, transistors M7 and M8 are off, and M tail is on. Output voltages (Out p, Out n), which had been pre- charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Out p discharges faster than Out n, hence when Out p (discharged by transistor $M2$ drain current), falls down to VDD–|Vthp| before Out n (discharged by transistor $M1$ drain current), the corresponding PMOS transistor ($M5$) will turn on initiating the latch regeneration caused by back-to-back inverters and M4, M6). Thus, Out n pulls to VDD and Out p discharges to ground. If VINP < VINN, the circuits works vice versa.
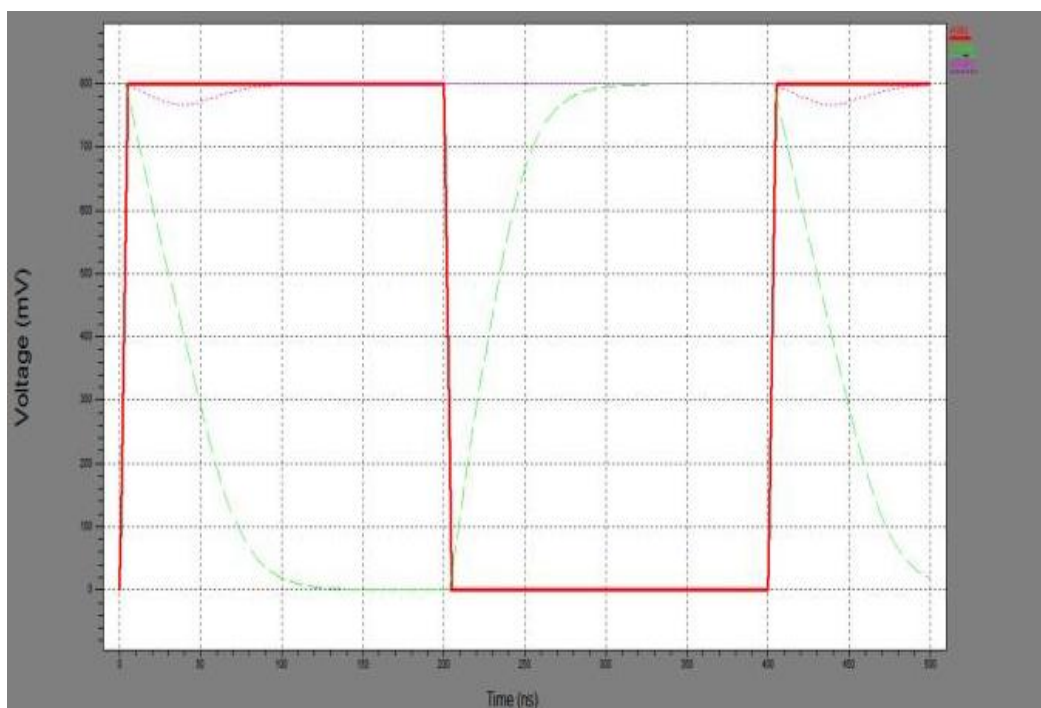

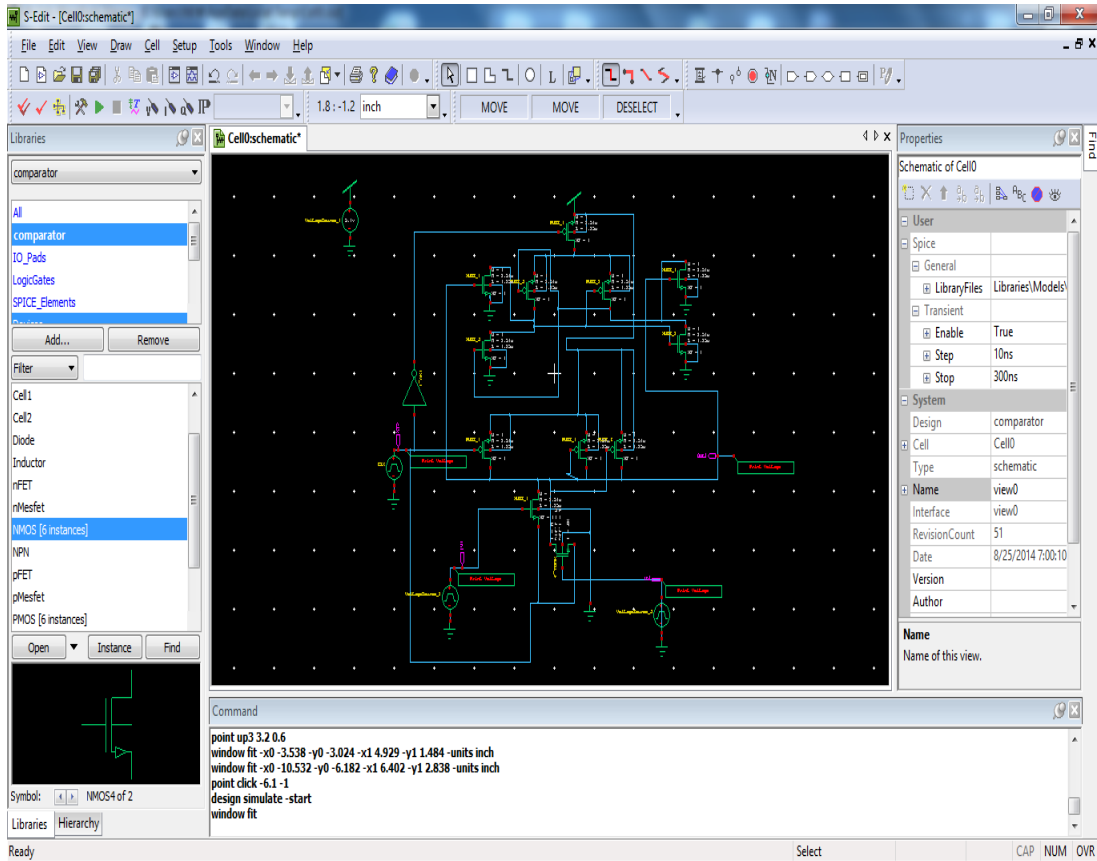**Figure 4:** Transient simulation of dynamic comparator

Figure 5: schematic diagram of dynamic double tail comparator
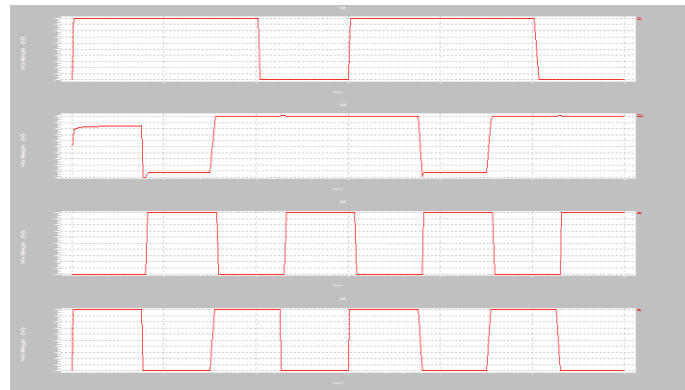
IV. Simulation Results

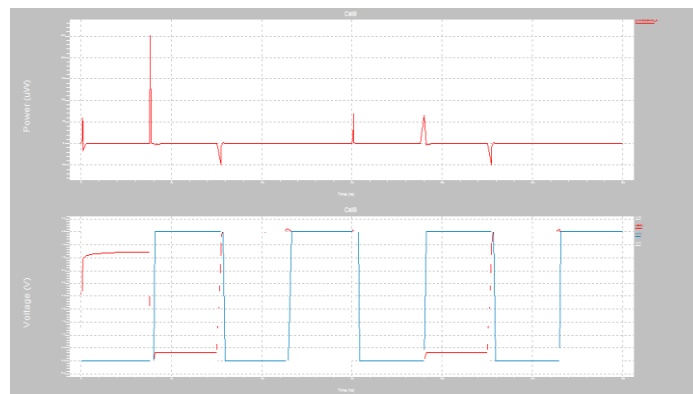
Figure 6: Comparator Result

Figure 7: Power measurement

V.   Conclusion

The proposed work designed with Bipolar CMOS technology, In the existing design they proposed the conventional Double tail comparator that was designed for reduced power consumption and also it concentrates in some other factors, such as delay, area, noise. The proposed design provides promising result than existing system. This work concentrated on reduction of power and also area efficiency, by reducing number of transistors. We have reduced number transistors from 16 to 12 and thus the area also reduced. Thus from the overall parameters we have achieved better performance than the existing design of comparator. For this design of proposals designed in CMOS design methodology and we have used Tanner EDA 13.0 as simulation tool to show the performance analysis of this Implementation.

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