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Design of Ternary D Flip-Flop Using Neuron MOSFET

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Abstract: *In this paper, we have designed D flip-flop using NAND gates. The gates are ternary NAND gates, which are constructed using Neuron MOS transistors. According to D Flip-Flop operation, output will follow the input which is given in the form of ternary logic as 0, 1, 2. A considerable reduction in the number of transistor count is achieved using this new configuration. The circuit simulation is done using T-spice and waveforms are checked using W-edit. The circuit is design using transistor length L=0.18u.*
Keywords: *D flip-flop, Floating-gate, Neuron MOS, Ternary logic, TNAND.*

I. Introduction

Conventional digital logic consists of Binary Logic which is used for computation in today's world. Digital equipments designed based on binary logic system are easy to implement, low cost and consume less power. But over the years, its usage will meet saturation. This is where systems having radix greater than 2(binary system)comes into picture. These systems are known as Multi-valued logic (MVL) system. The advantages and disadvantages of MVL systems are mentioned in [8]. The important advantages of MVL systems are that more number of information can be sent over channels and number of interconnections on chip can be reduced. In a typical VLSI circuit, about 70% of the on-chip area is consumed by interconnections and remaining for devices [9]. Thus reduction of interconnections is becoming one the important factor while designing the chip. There are several disadvantages of MVL systems than binary logic system, but with proper optimization of design we can try to overcome such disadvantages.

This paper demonstrates ternary D flip-flop using neuron MOS transistor. Considerable reduction in transistor count is achieved by using neuron MOS transistors. In Section II information of neuron MOS transistor is given, section III ternary logic, section IV Ternary NAND gate implementation, section V ternary D flip-flop implementation, section VI simulation results of ternary NAND gate and ternary D flip-flop and lastly section VII conclusions of the proposed work.

II. Neuron Mos Transistor

The proposed work uses neuron MOS transistor for implementation. The neuron MOS transistor is also known as multiple input floating gate (MIFG) transistor or floating gate MOSFET (FGMOS) [3]. In [1-2] a functional MOS transistor is proposed which behaves more cleverly than a mere switching device. The device has a floating gate and the potential on it is determined by the control gates. The control gates are coupled with floating gate through capacitors. The device is called "Neuron MOS transistor", because it is analogues to biological neurons, in which the transistor turns on when the weighted sum of all the input signals exceeds a certain threshold value. With neuron MOS transistors they have developed various applications such as variable threshold voltage transistor, a single-gate D/A converter and Soft-Hardware logic circuit. The technologies developed for floating gate EPROM's and EEPROM's are directly transferable to implement the neuron MOS in VLSI circuits [1-3].

The neuron-MOS transistor's basic construction is shown in Fig. 1(a) [1-2].It is an n- channel MOS transistor having a gate electrode which is electrically floating. There are n control gates which are coupled through capacitors to the floating gate. The terminal voltages and various capacitive coupling coefficients are defined in Fig. 1(b), where ϕ_F is floating gate potential, $V_1, V_2, \ldots V_n$ are input signal voltages, $C_1, C_2, \ldots, C_n$ are capacitive coupling coefficients between floating gate and each of the input, C_0 is the capacitive coefficient between floating gate and substrate, and $Q_0, Q_1, Q_2, \ldots, Q_n$ are the charges in each of the capacitors. A symbol representing the device is shown in Fig. 1(c).The equations for floating gate potential charges on input gates and floating gate are determined in [2] are as follows.

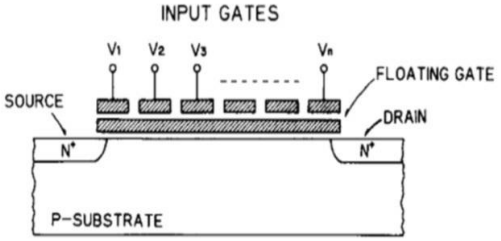

Fig. 1(a) Basic structure of neuron MOS transistor [1-2]

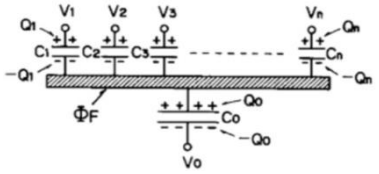

Fig. 1(b) Relationship among terminal voltages and capacitance coupling coefficients [1-2]

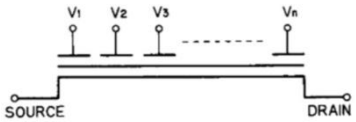

Fig. 1(c) Symbol representing the device [1-2]

Let QF denote the net charge in the floating gate, which is calculated as

$$Q_F = Q_0 + \sum_{i=1}^{n}(-Q_i) = \sum_{i=0}^{n} C_i(\phi_F - V_i)$$
$$= \phi_F \sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i \qquad (1)$$

It is assumed that no charge injection occurs during de- vice operation. Then QF is equal to the initial charge in the floating gate, which is assumed to be zero at the moment for simplicity. Such assumptions do not prevent generality of the analysis in the following, as is discussed later in this section. All voltages are measured with respect to the ground, and the substrate and source are both grounded; namely, $V_s = V_0 = 0$. Here V_s and V_0 denote the source and substrate potentials, respectively. Then (1) reduces to

$$\phi_F = \frac{C_1 V_1 + C_2 V_2 + \ldots . C_n V_n}{C_{TOT}} \qquad (2)$$

where

$$C_{TOT} = \sum_{i=0}^{n} C_i$$

One of the most important features of this functional device is clearly expressed in (2), which states that the floating-gate potential ϕ_F is determined as a linear sum of all input signals weighted by the capacitive coupling coefficients. The voltage signals are directly added at the gate level without any power dissipation.

A number of input gates are interacting with the floating gate via different capacitive coupling coefficients and the potential of the floating gate controls the formation of the channel underneath the gate oxide, i.e., the "on" and "off" of the MOS transistor. The value of ϕ_F is uniquely determined by (2) provided that all capacitive coupling coefficients are not changing during device operation. Among all C_i's, only C_0 can vary depending on theoperating condition of the transistor. However, it can be reasonably well approximated by the gate oxide capacitance when the device is on and the channel is formed, the case of interest in the study of de- vice operation. As long as the channel is formed, the value of C_0 does not vary appreciably and can be regarded as a constant. Here we would like to introduce a parameter Υ which is defined as

$$\Upsilon = \frac{C_1 + C_2 + \ldots . C_n}{C_{TOT}} = \frac{C_{TOT} - C_0}{C_{TOT}} \qquad (3)$$

ΥV_{DD} represents the maximum floating-gate voltage obtained as all input gates are at V_{DD}. Since the value is the voltage gain of the floating gate as a result of its capacitive coupling to all of the input gates, Υ is called the floating-gate gain factor, one of thekey design parameters of the device and circuits.

Let V_{TH}^* be the threshold voltage of the transistor as seen from the floating gate. Then the transistor tums on at the condition of $\phi_F > V_{TH}^*$, namely

$$\frac{C_1 V_1 + C_2 V_2 + \ldots . C_n V_n}{C_{TOT}} > V_{TH}^* \qquad (4)$$

This relationship presents the other important feature of the device, the threshold operation. When the linear weighted sum of all input signals exceeds a certain threshold value V_{TH}^*, the transistor turns on. The behavior of the transistor very well resembles that of a biological neuron [2].

III. Ternary Logic

Ternary logic has three switching values and it has it has radix 3. The logics are interpreted as low, intermediate and high, which can be represented by 0, 1, 2 or -1, 0, 1 logic levels. 0, 1, 2 logics are called as unbalanced ternary whereas -1, 0, 1 logics are called as balanced ternary [10]. The advantages and disadvantages of ternary logic is given in [8]. The comparison is made between balanced ternary and unbalanced ternary which is given in [10] and based on requirements it can be chosen. It is nicely proven in [10] the efficiency of system having radix e=2.71828. Hence ternary logic system (radix =3)is better than binary system (radix = 2). The feasibility of ternary logic digital systems has been demonstrated in [6]. Ternary digital algebra, ternary codes, minimization of ternary expressions by manipulating algebraic expressions like in boolean algebra or ternary maps ortabulation method is explained in [6-7]. In [5], ternary storage elements, ternary flip-flops such as PZN, D type, T type, ternary counters, ternary RAM, ternary ROM are realized using COS/MOS integrated circuits. Here we will use which is required for our proposed work.

IV. Ternary Nand Gate

We have considered ternary logic as (0,1,2). For the construction of D flip-flop using Ternary NAND gates (TNAND) we have proposed TNAND gates using neuron MOS transistors. The expression for TNAND is given as [5]

$$\text{TAND: } A \wedge B = \min(A, B) \qquad (5)$$

$$\text{TNAND: } \overline{A \wedge B} = 2 - [\min(A, B)] \qquad (6)$$

The truth table of TNAND gate is given in Table I.

Table I: Truth Table of Ternary NAND Gate

Inputs		Outputs		
A	B	PTNAND	NTNAND	STNAND
0	0	2	2	2
0	1	2	2	2
0	2	2	2	2
1	0	2	2	2
1	1	2	0	1
1	2	2	0	1
2	0	2	2	2
2	1	2	0	1
2	2	0	0	0

In Table I, PTNAND is Positive Ternary NAND, NTNAND is negative ternary NAND and STNAND is standard ternary NAND. PTNAND = 0 when all the inputs are high (here it is logic 2), else PTNAND = 2. NTNAND = 2 when any one input is high, else NTNAND = 0. STNAND = 2 – [min (A, B)] from eq. (6). Interestingly,

$$\text{STNAND} = \frac{\text{PTNAND} + \text{NTNAND}}{2} \quad (7)$$

The schematic diagram of ternary NAND gate is shown in Fig.2. TNAND gate is two input NAND gate. PTNAND and NTNAND gates require only 3 transistors each. The series connected pull down network uses only one n-type neuron MOS, which has two inputs. In conventional ternary CMOS or CNTFET circuits, the pull down network which is connected in series will require 2 transistors. So in all, 4 transistors each are required for NTNAND and PTNAND realization in CMOS or CNTFET circuits. Thus for two input TNAND gate we have saved one transistor each in PTNAND and NTNAND, and two transistors in STNAND. The simulation results of TNAND are shown in Fig. 4.

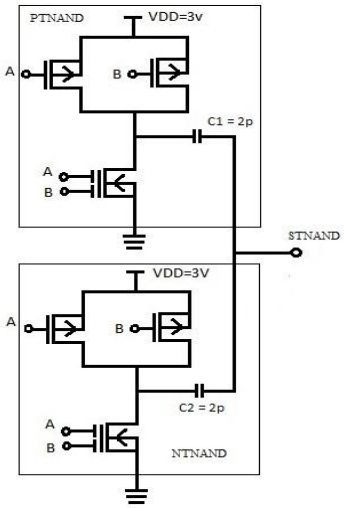

Fig. 2 Schematic of ternary NAND gate using neuron MOSFET

V. Ternary D Flip-Flop Using Tnand Gates

We have proposed ternary D flip-flop using TNAND gate, it is shown in Fig. 3. As per D flip-flop functionality output follows the input.The simulation results of ternary D flip flop is shown in Fig. 5.We have connected one TNAND gate as inverter at output Q, which act as a load. The topmost wave in Fig. 5 denotes wave of load. Starting from top to bottom waveforms are denoted at terminals load, $\overline{Q}$, Q,Clk, Din.

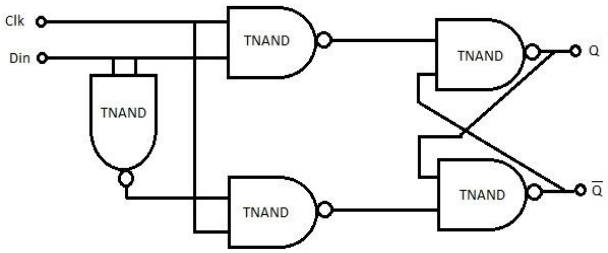

Fig. 3 Schematic of Ternary D flip-flop using TNAND gates.

VI. Simulation Results

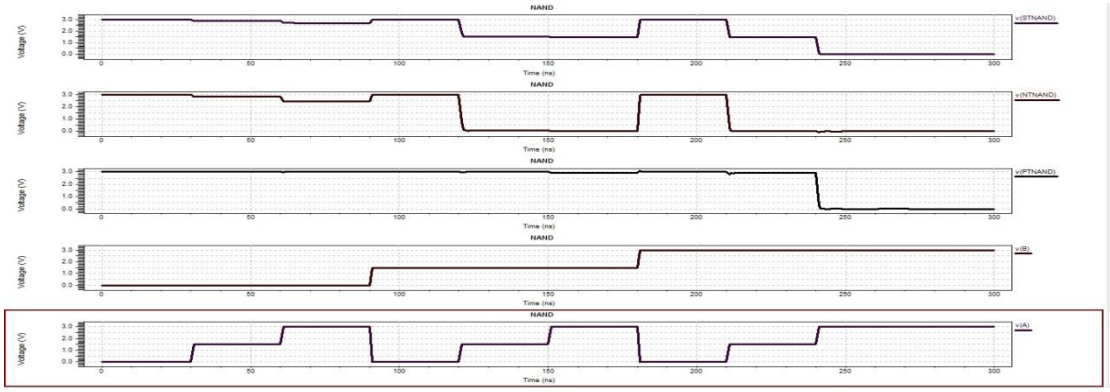

Fig. 4 Simulation results of TNAND gate.

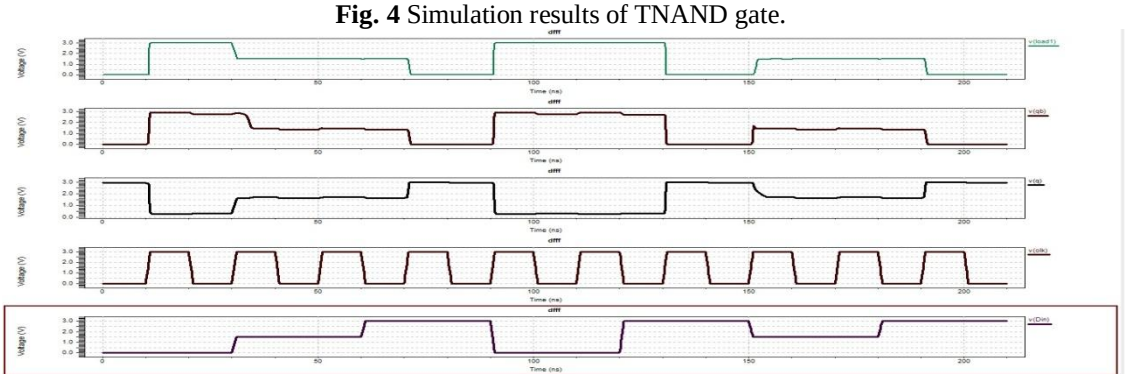

Fig. 5 Waveform of Ternary D flip-flop using TNAND gates.

VII. Conclusions

A ternary D flip-flop using TNAND gate is presented. The TNAND gates are realized using neuron MOS transistors. The output of ternary D flip-flop makes transition at positive edge of the clock. The number of transistors required for the implementation of ternary D flip-flop is 30, whereas for conventional CMOS or CNTFET circuit requires 40 transistors. Thus there is reduction of ten transistors in our proposed work. We have used T-spice and W-edit for circuit simulation. We have used L=0.18u, W_n =5u and L = 0.18u, W_p= 20u as the dimensions of n-type and p-type neuron MOS transistors respectively. The rise time and fall time of the circuit are mentioned in Table II. The circuit can drive a load as demonstrated. The load is TNAND gate as inverter. The proposed circuit can be used for implementation of counters. We have made an attempt to make TNAND gate as universal ternary gate, which can implement any ternary logic.

Table II: Rise Time and Fall Time of Ternary D Flip-Flop

Rise Time		Fall Time	
0 to 1	0.782 ns	1 to 0	0.118 ns
1 to 2	0.309 ns	2 to 1	0.128 ns
0 to 2	40.96 ns	2 to 0	0.270 ns

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