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VLSI Implementation of Area Efficient Fast Parallel Fir Digital Filters Based On Fast Fir Algorithm

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Abstract: *This paper proposes new parallel fir structures to reduce the hardware complexity of higher order Finite Impulse Response (FIR) filter with symmetric coefficients based on Fast FIR Algorithms (FFAs). The objective is to design an area-efficient Fast Parallel Finite-Impulse Response (FIR) filter structure which constraint that the filter taps must be a multiple of 2 or 3. In this brief discussed for three parallel FIR Filter implementation based on recursively using proposed 2 parallel FIR Structure. It exploits the inherent nature of Symmetric co-efficient reducing the number of Multipliers in further. The parallel FIR filter structure based on proposed FFA techniques has been implemented based on Modified carry save adder (MCSA) for further enhancement. The reduction in hardware complexity is achieved by eliminating the bulky multiplier with an adder namely MCSA. Overall, the proposed parallel FIR structures can lead to significant hardware savings for symmetric coefficients from the existing FFA parallel FIR structures, particularly when the length of the filter is very large.*

Keywords: *Symmetric Filter; Polyphase decomposed Fast Finite Impulse Response (FIR) Algorithm (FFA); Common Sub expression Elimination (CSE) ; Level Constrained Common Sub expression Elimination (LCCSE) Parallel FIR symmetric convolution; Very Large Scale Integration (VLSI); FFA technique.*

I. Introduction

The vital area of research in VLSI System Design is the area-efficient high-speed data path logic systems. Digital Filters are one of the most widely used fundamental devices in DSP systems, ranging from explosive growth in multimedia signal processing to wireless mobile communications. FIR filters are used in high frequency applications, like as multimedia signal processing, whereas some other applications require high throughput with a low-power circuit such as Multiple Input Multiple Output (MIMO) systems used in cellular wireless communications. A higher order digital filter is used video ghost canceller for broadcast television, it reducing the effect of multipath signal echoes. So higher order digital filter is unavoidable.

Area complexity is optimized by reducing bulky multipliers from (2N - N/L) to L x N using the FFA technique. The Iterated Short Convolution (ISC) based linear convolution structure is transposed to obtain a new hardware efficient. i.e., Small-sized filtering structures recursively used to constructed large filters in [6]-[10].

This paper is organized as follows. A brief introduction of existing FFAs is shown in Section II. In Section III, the proposed new parallel FIR filter structures are presented. Section IV investigates the complexity analysis of an existing with proposed structures. In Section V, the description of hardware implementation and the experimental results are shown. Finally, section VII describes the conclusions and future work.

I. Fast FIR Algorithm (FFA)

In general the output of an n-tap FIR filter which can be expressed as in (1)

$$y(n) = \sum_{i=0}^{N-1} h(i).\, x(n-i), \quad n = 0,1,2,\ldots\ldots,\infty \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ \mathbf{(1)}$$

where the input {x(n)} is an infinite-length input sequence of the length N FIR filter coefficients. Then, the traditional L-Parallel FIR filter can be expressed from polyphase decomposition as in [3].

$$\sum_{i=0}^{L-1} Y_p(z^L).\, z^{-p} = \sum_{q=0}^{L-1} X_q(z^L)z^{-q} \ \sum_{r=0}^{L-1} H_r(z^{-L})z^{-r} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\mathbf{(2)}$$

Where $X_q = \sum^{\infty} z^{-k}\, x\,(L_k+q)$, $H_r = \sum^{(N/L)-1} z^{-k} X(L_k+r)$, $Y_p = \sum^{\infty} z^{-k} X(L_k+p)$ for p,q,r = 0,1,2,……..L-1.

k=0 k=0 k=0

From the above equation shows that the traditional FIR filter will require L^2 Subfilter blocks of length N/L for its implementation.

(1).Existing 2x2 FFA (Level of parallelism, L = 2):

By using equation (2) a two parallel FIR filter can be described as,

$Y_0 + z^{-1}Y_1 = (H_0 + z^{-1} H_1) (X_0 + z^{-1} X_1) = H_0X_0 + z^{-1}(H_0X_1 + H_1X_0) + z^{-2}X_1H_1$ **……………...... (3)**

After simplifying this can be,

$Y_0 = H_0X_0 + z^{-2} X_1H_1 , Y_1 = H_0X_1 + X_0H_1$ **……………..… (4)**

Equation (3) and (4) shows the traditional two-parallel filter structure, which will require four length-N/2 FIR sub filter blocks, two post processing adders, and totally 2N multipliers and (2 N - 2) adders.
However, (4) can be written as,

$Y_0 = H_0X_0 + z^{-2} X_1H_1$

$Y_1 = (H_0 + H_1) (X_0 + X_1) – H_0X_0 – H_1X_1$ **……………..… (5)**

This above equation (5) will take three FIR sub filter blocks of length N/2, one preprocessing and three post processing adders, and 3N/2 multipliers and 3(N/2 - 1) +4 adders, which reduces approximately one forth over the traditional two-parallel filter hardware cost from the equation (4). The Two-parallel (L=2) FIR filter implementation using obtained from (5) is shown in Fig.1.

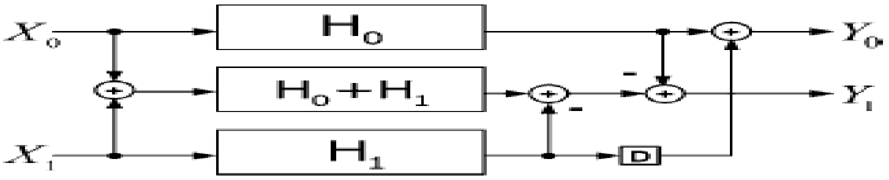


Fig. 1: Existing FFA for Two-parallel FIR filter implementation

(2).Existing 3x3 FFA (Level of parallelism, L = 3):

By the similar approach, a three- Parallel FIR filter using FFA can be described as,

$Y_0 = H_0X_0 - z^{-3} X_2H_2 + z^{-3} [(H_0 + H_1) (X_0 + X_1) – H_1X_1]$

$Y_1 = [(H_0 + H_1) (X_0 + X_1) – H_1X_1] – (H_0X_0 - z^{-3} X_2H_2)$

$\mathbf{Y_2} = \mathbf{[}(H_0 + H_1+H\mathbf{)(}X_0+X_1+X_2\mathbf{)]}–[(H_0 + H_1)(X_0 + X_1) –H_1X_1] –[(H_1 + H_2)(X_1+X_2) –H_1X_1]$ **……………… (6)**

This above equation (5) will take six length N/3FIR sub filter blocks, three preprocessing and seven post processing adders, and N multipliers and 2N + 4 adders, which further reduces approximately one third over the traditional three-parallel filter hardware cost from the equation(6). The Three-parallel (L=3) FIR filter implementation using obtained from (6) is shown in Fig.2

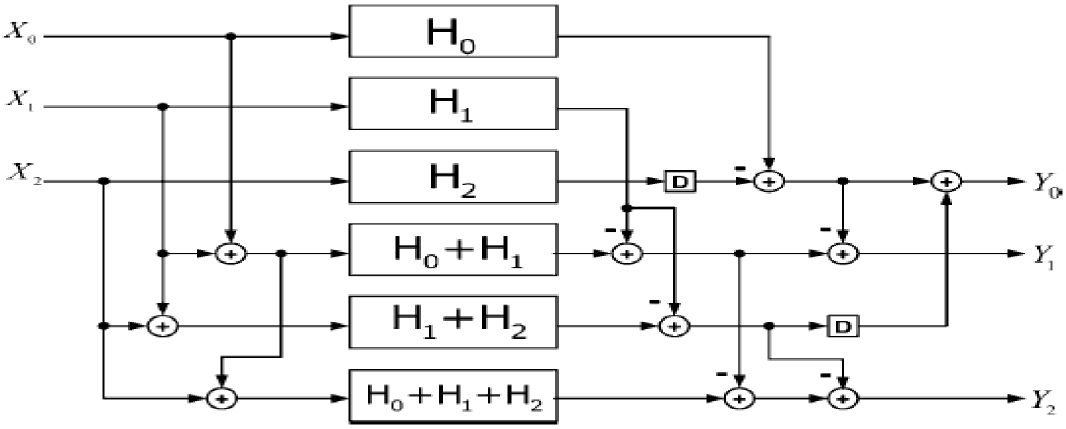


Fig. 2: Existing FFA for Three-parallel FIR filter implementation

II. Proposed New parallel structures Based on Fast FIR Algorithm

The Main idea behind the proposed structure is based on Fast FIR Algorithm which utilizes the symmetric co-efficient, manipulating the poly phase decomposition to earn as many sub filter blocks as possible. The sub filter blocks containing symmetric coefficients, so the required number of multiplications is reduced to half in a single Sub filter block. It can be recursively used for the whole taps.

(1).Proposed 2x2 FFA (Level of parallelism, L = 2):

From (4), a two – parallel FIR Filter can also be written as,

$Y_0 = \{ 1/2 [(H0 + H_1) (X_0 + X_1) + (H0 – H_1) (X_0 – X_1)] – H_1 X_1\} + z^{-2} H_1 X1$
$Y_1 = 1/2[(H0 + H_1) (X0 – X_1) – (H0 – H_1) (X_0 – X_1)]$ …………………….. **(7)**

This above equation (7) comes to a set of even symmetric coefficients, which can earn one more sub filter block containing symmetric coefficients than (5), from the existing FFA parallel FIR Filter. The Proposed Two-parallel (L=2) FIR filter implementation using obtained from (7) is shown in Fig.3.

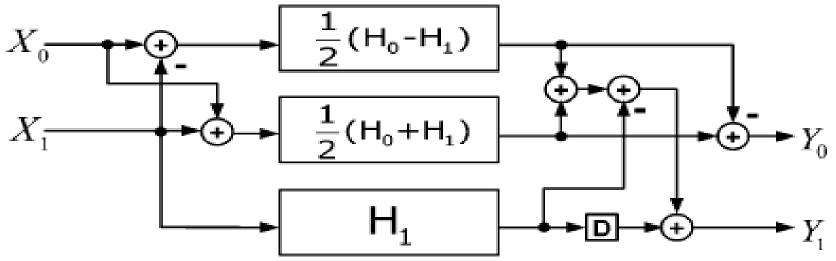


Fig. 3: Proposed FFA for Two-parallel FIR filter

For an example Consider a 16 – tap FIR Filter with a set of symmetric coefficients applying to the proposed two-Parallel FIR filter as follows,

{ h(0),h(1),h(2),h(3),h(4),h(5),h(6),h(7),
h(8),h(9),h(10),h(11),h(12),h(13),h(14),h(15)**}**
where h(0) = h(15), h(1) = h(14), h(2) = h(13), h(3) = h(12), h(4) = h(11), h(5) = h(10), h(6) = h(9), h(7) = h(8), applying to the proposed two parallel FIR Filter structure, and the top two sub filter blocks will be as,

$\mathbf{H_0 \pm H_1 = \{}$ h(0) ± h(1), h(2) ± h(3), h(4) ± h(5), h(6) ± h(7), h(8) ± h(9), h(10) ± h(11), h(12) ± h(13), h(14) ± h(15) }

Where ,h(0) ± h(1) = ± h(14) ± h(15) ,h(2) ± h(3) = ± h(12) ± h(13), h(4) ± h(5) = ± h(10) ± h(11) , h(6) ± h(7) = ± h(8) ± h(9) …………..……….….. **(8)**

From this example, the proposed two parallel FIR Filter structure having two sub filter blocks out of three. i.e., $\mathbf{H_0 + H_1}$ and $\mathbf{H_0 - H_1}$ these two sub filter blocks are with symmetric coefficients now, as per equation (8). The sub filter block is realized in fig.4.

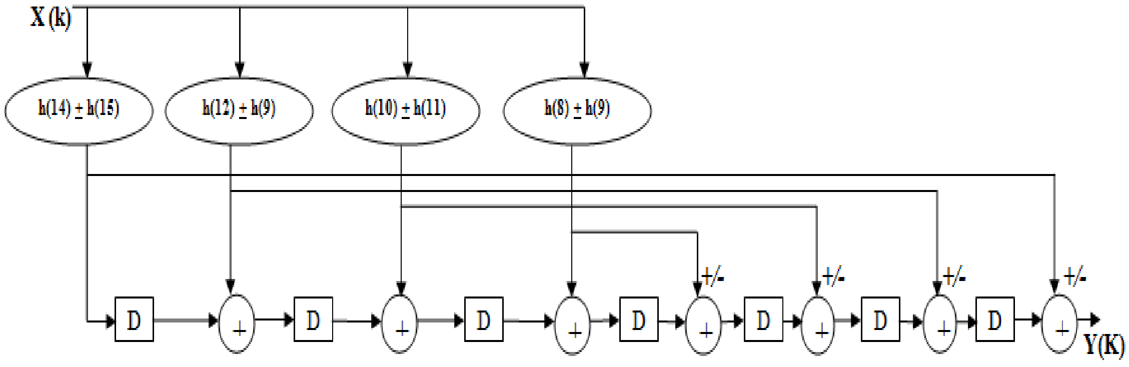


Fig. 4: Sub filter implementation with symmetric coefficients

(2).Proposed 3x3 FFA (Level of parallelism, L = 3):

By the similar approach of (7), a three-parallel FIR Filter can also be expressed by recursively using the proposed 2x2 FFA.

$$Y_0 = \frac{1}{2}[(H0 + H_1)(X_0 + X_1) + (H0 - H_1)(X_0 - X_1)] - H_1 X_1 + z^{-3}\{(H_0+H_1+H_2)(X_0 + X_1 + X_2)$$
$$- (H0 + H_1)(X_0 + X_1) - \frac{1}{2}[(H0 + H_1)(X_0 + X_1) + (H0 - H_1)(X_0 - X_1)] - H_1 X1\}$$
$$Y_1 = \frac{1}{2}[(H0 + H_1)(X_0 + X_1) - (H0 - H_1)(X_0 - X_1)] + z^{-3}\{(H_0+H_2)(X_0 + X_2) - (H0 - H_2)(X_0 - X_2) -$$
$$\frac{1}{2}[(H_0+H_1)(X_0 + X_1) + (H0 - H_1)(X_0 - X_1)] - H_1 X_1\}$$
$$Y_2 = \frac{1}{2}\{[(H0 + H_2)(X_0 + X_2) - (H0 - H_2)(X_0 - X_2)]\} + H_1 X_1 \quad \text{..........................} \quad \textbf{(9)}$$

This above equation (9) comes to a set of even symmetric coefficients, which can earn four sub filter blocks containing symmetric coefficients from the total of six sub filter blocks in the existing 3x3 parallel FFA Structure, The Proposed Three-parallel (L=3) FIR filter implementation using obtained from (9) is shown in Fig.5.

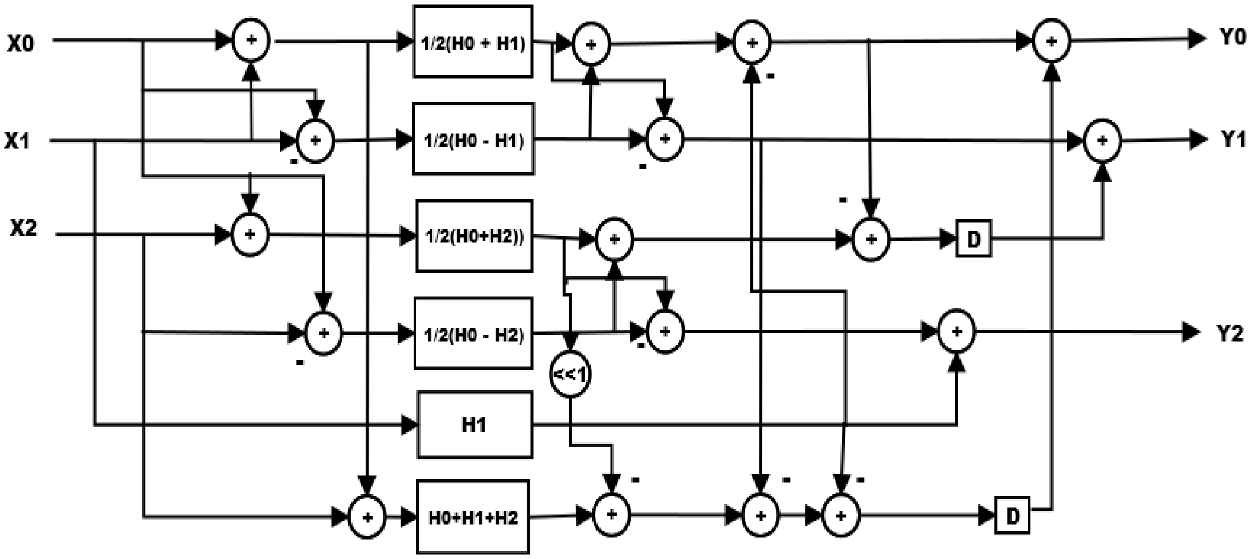


Fig. 5: Proposed FFA for Three-parallel FIR filter

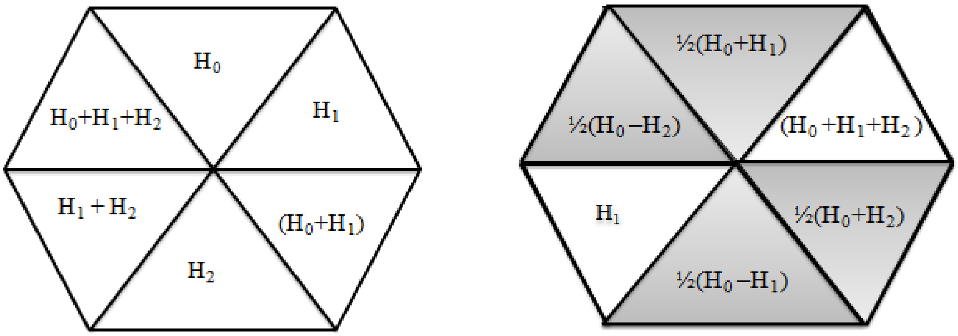


Fig. 6: Comparison of Sub filter blocks between existing FFA and the Proposed FFA for Three-parallel FIR filter Structures

From the above figure 6. The shadow region in the proposed FFA stands for symmetric coefficients. Therefore, for an N –tap three –parallel FIR Filter, the

Proposed structure can earn N/3 multipliers from the existing FFA structure. However, this proposed three-parallel FIR structure also brings on overhead of seven additional adders in both preprocessing and post processing adders.

(3).Proposed Cascading FFA (Based on Symmetric coefficients)

The larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures. The proposed parallel Cascading FFA structure enables the reuse of multipliers in parts of the sub-filter blocks but it also brings more adder cost in preprocessing and post processing blocks. When cascading the proposed FFA parallel FIR structures for larger parallel block factor L, the increase of adders can become larger. Due to this other than applying the proposed FFA structure to all decomposed sub filter block blocks, the existing FFA structures which have more compact operations in pre processing and post processing blocks are employed for those sub-filter blocks that contain no symmetric coefficients.

Whereas the proposed FIR filters structures are still applied to the rest of sub-filter blocks with symmetric coefficients. Figure 7 shows an illustration of comparison of sub filter blocks between existing and proposed FFA four – parallel FIR Filter Structures using Cascaded FFA. The shadow region in the proposed FFA stands for symmetric coefficients.

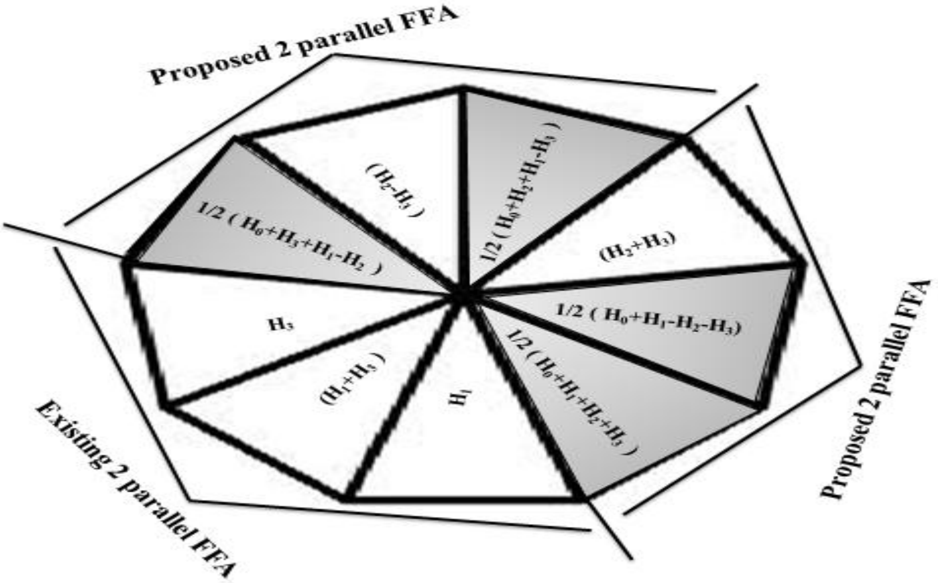

Proposed 2 parallel FFA
(H$_2$-H$_3$)
1/2 (H$_0$+H$_2$+H$_1$-H$_3$)
1/2 (H$_0$+H$_3$+H$_1$-H$_2$)
(H$_2$+H$_3$)
1/2 (H$_0$+H$_1$-H$_2$-H$_3$)
H$_3$
(H$_1$+H$_3$)
H$_1$
1/2 (H$_0$+H$_1$+H$_2$+H$_3$)
Existing 2 parallel FFA
Proposed 2 parallel FFA

Fig. 7 (a): Sub filter Section of Proposed FFA for Proposed Four-parallel FIR filter using Cascading approach

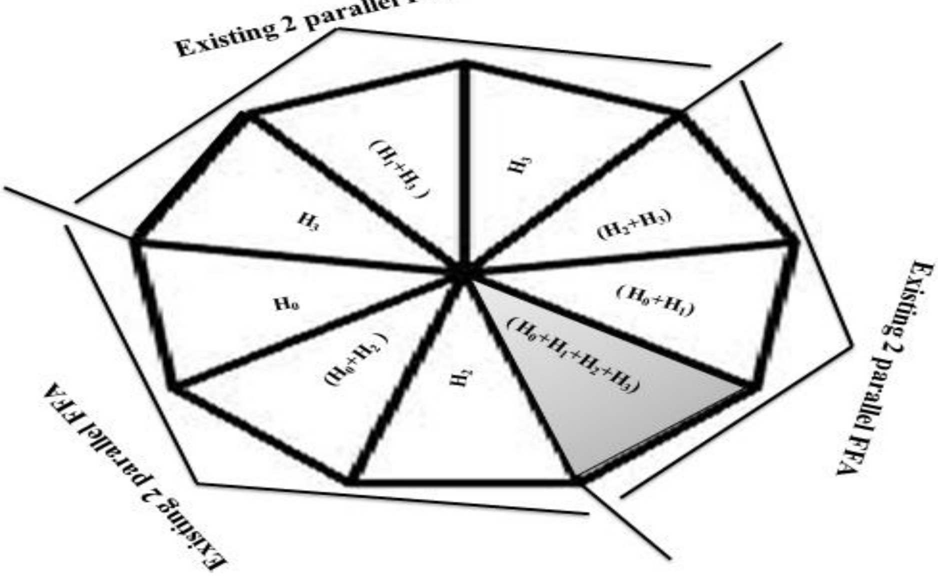


Fig. 7 (b): Sub filter Section of existing FFA for Four-parallel FIR filter using Cascading approach

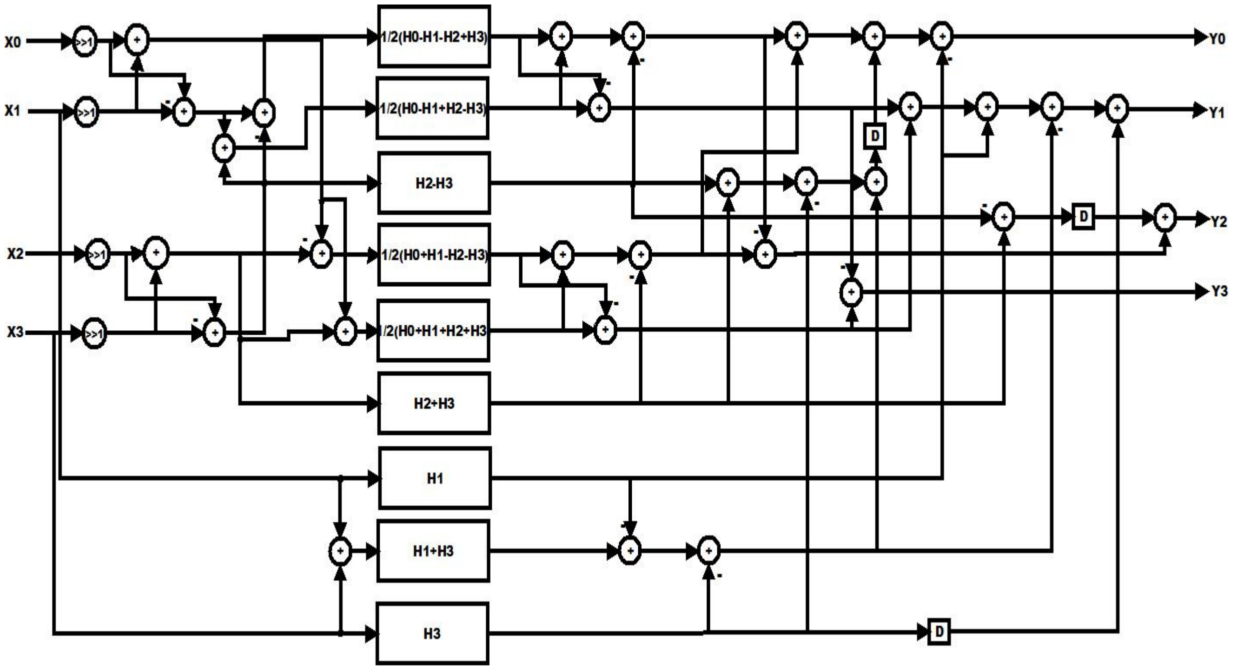


Fig. 8: Proposed FFA for Four-parallel FIR filter

(4).Proposed Canonical Sign Digit Representation (for Constant Symmetric coefficients multiplication)

The canonical signed digit (CSD) representation is one of the existing signed digit (SD) representations with unique features which make it useful in certain DSP applications focusing on low-power, efficient-area and high-speed arithmetic.

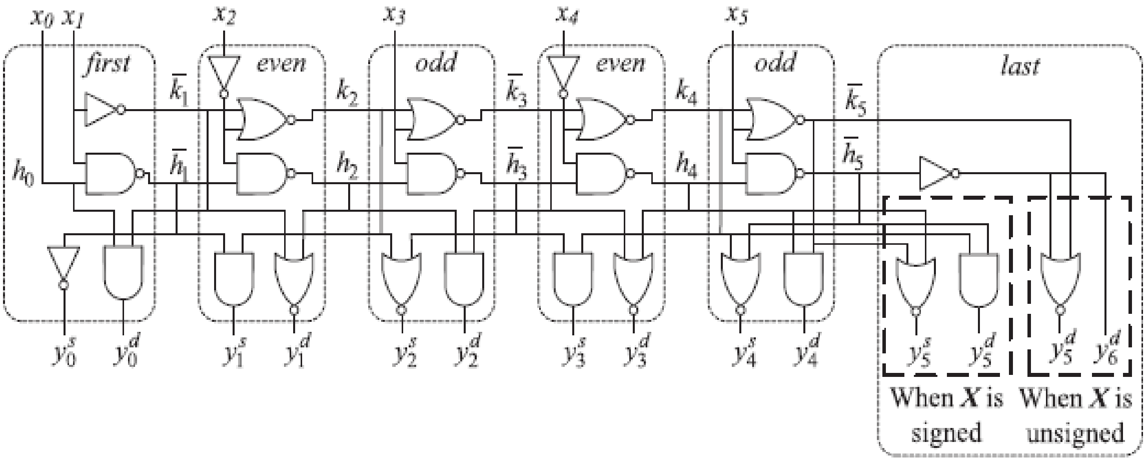


Fig.9: Hardware Architecture of Binary to CSD Conversion

The CSD code is alternary number system with the digit set{ $\bar{1}$ 0 1},where $\bar{1}$ stands for 1.Given a constant, the corresponding CSD representation is unique and has two main properties:(1)the number of nonzero digits is minimal ,and (2) no two consecutive digits are both non zero, that is, two non zero digits are not adjacent. The first property implies a minimal Hamming weight, which leads to a reduction in the number of additions in arithmetic operations. The second property provides its uniqueness characteristic.

For a constant CSD representation has proven to be useful for the design and implementation of digital filters such as the area-efficient program-mable FIR digital filter architecture in Chebyshev FIR filter can be design with some constrains in terms of hardware and frequency domain. Figure. 7 Shown the proposed CSD conversion from its equivalent binary number. An efficient implementation for CSD conversion is shown in Fig.8. The fast implementation of a CSD recoding is based on the binary associative property. This is developed for their prefix adders.

(5). Design of Multiplier and Adder Blocks

Finite-impulse response (FIR) digital filters are widely employed in digital signal processing due to their stability and linear-phase property. The FIR filter consists of many constant multiplications, in past have decomposed the multiplications into simple operations such as addition, subtraction and shift and have tried to share as many partial sums as possible to reduce the hardware complexity. As shown in Figure 8, all coefficients are considered as a whole to design all the Constant multiplications into a hardware block called a multiplier block.

There are two metrics that are important in the design and comparison of digital FIR filters. The first one is the adder cost, which is the number of adders required to implement a given set of filter coefficients, and the second is the adder step, which is the number of adders passing through the critical path. Many algorithms have been proposed to reduce the adder cost and adder step, which can be categorized into two groups: 1) dependence-graph and 2) common sub expression elimination (CSE) algorithms. Since the FIR filter consists of many constant multiplications, earlier works have decomposed the multiplications into simple operations such as addition, subtraction and shift and have tried to share the partial sums as many as possible in order to reduce the hardware complexity.

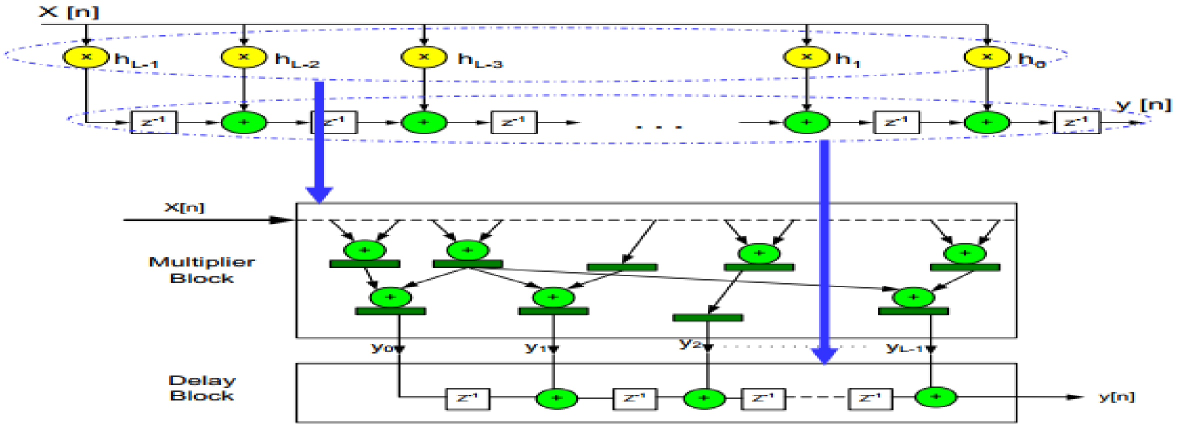


Fig.8: Replacing Constant Multiplication by Multiplier

Block in Sub filter Block of symmetric Convolution

Example 1: Let Coefficient Set As {3, 13,219,221}
Consider X=1001, h0=11,
X*h0 = 1001 * 11
1 0 0 1 -------- X
1 0 0 1 0 --------- X<<1 (+)
X*h0= X + X << 1

Multiplier Block is being replaced by Multiplier. The Multiplier block is simply nothing but only Adders. So the Add/Shift Implementation is consists of only Adders and Shifts.

3*X = 0011 * X = X + X << 1
13*X = 1101 * X= X + X << 2 + X << 3
219 * X = 1101 1011 * X= X+X << 1+X << 3 + X << 4 + X << 6 + X << 7
221 * X = 1101 1101 * X = X+ X << 2 + X << 3 + X << 4 + X<< 6 +X <<7

In the above coefficient set {3, 13,219,221} can be implemented using Add/Shift Implementation. By using Add/Shift Implementation 3*X is expressed in terms of X+X<<1.

III. Complexity analysis of an existing with proposed structures:

Whenever the L–parallel FIR filter comes with a set of symmetric coefficients of length N, the number of required Multipliers for the proposed parallel FIR filter structures is given by,
Case 1:

When $\frac{N}{\prod_{i=1}^{r} L_i}$ is even, $M = \frac{N}{\prod_{i=1}^{r} L_i}\left(\prod_{i=1}^{r} M_i - \frac{S}{2}\right)$ …………………………. (10)

Case 2:

When $\frac{N}{\prod_{i=1}^{r} L_i}$ is odd, $M = \frac{N}{\prod_{i=1}^{r} L_i}\prod_{i=1}^{r} M_i - \frac{S}{2}\left(\frac{N}{\prod_{i=1}^{r} L_i} - 1\right)$ ………………….…. (11)

Where, L_i is the small parallel block size such as (2x2) or (3x3) FFA. r is the number of FFAs used. M_r is the number of sub filter blocks used from i-th FFA. Where, S is the number of sub filter blocks containing symmetric coefficients. The number of the required adders in sub filter section can be given by,

$$A_{Sub} = \prod_{i=1}^{r} M_i\left(\frac{N}{\prod_{i=1}^{r} L_i} - 1\right) \quad \text{……………….…… (12)}$$

A Comparison between the proposed and the existing FFA structures for even symmetric coefficients with different length under different level of parallelism is summarized in Table I.

Table I .Comparison of Proposed and the existing FFA Structures with different length and different level of parallelism

L	Filter Length	Structure	M	R.M	Required Adders		I.A
					Sub.	Pre/ Post.	
2	16-tap	FFA	22	6	24	4	2
		Proposed	16			6	
	72-tap	FFA	90	18	105	4	
		Proposed	72			6	
	596-tap	FFA	740	164	931	4	
		Proposed	596			6	
3	16-tap	FFA	32	8	42	10	7
		Proposed	24			17	
	72-tap	FFA	120	24	138	10	
		Proposed	96			17	
	596-tap	FFA	986	206	1256	10	
		Proposed	780			17	
4	16-tap	FFA	61	9	58	20	11
		Proposed	52			31	
	72-tap	FFA	153	27	153	20	
		Proposed	126			31	
	596-tap	FFA	1512	256	1347	20	
		Proposed	1256			31	

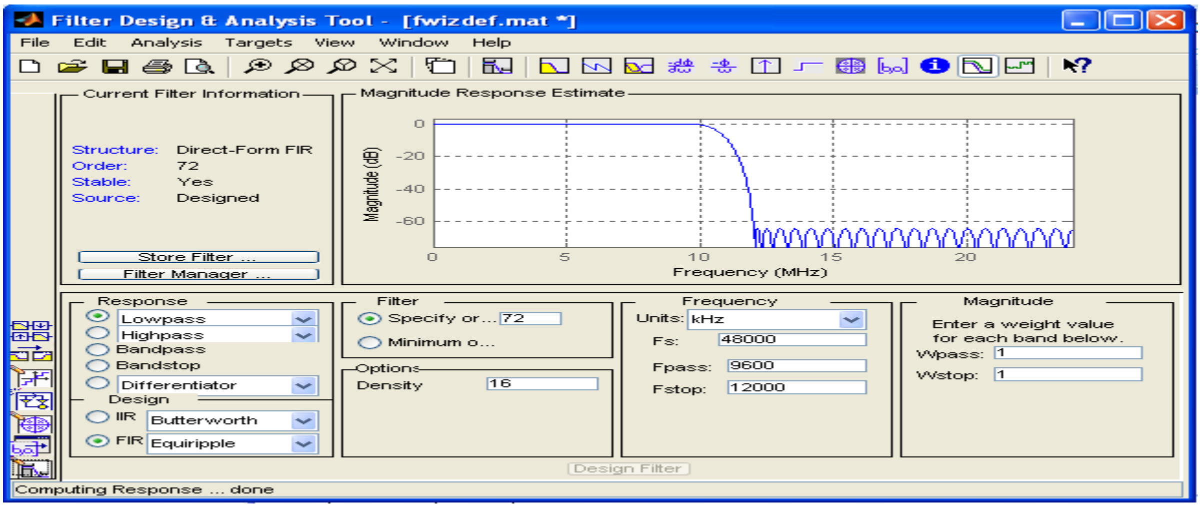
Where, M- Number of Required Multipliers, R.M. Reduced Multipliers, Sub- Number of Required Adders in Sub filters Section, Pre/Post – Number of Required Adders in Pre/Post Processing Blocks, I.A – Number of Increased Adders.

IV. Implementation and Experimental Results:

The proposed FFA structures and the existing FFA structures are implemented in VHDL with filter length of 16 and 72, word length of 8-bit and 16-bit, respectively. Two sets of Ideal Low pass FIR filter symmetric coefficients of length 16 and 72 are generated by MATLAB using Remez Exchange algorithm.The sub filters are based on Canonical Sign digit (CSD) structure and Reconfigurable Carry Save adder (RCSA) introduced in [7] are used. Figures 8,9,10 and 11 shows the output results of an 16 tap FIR filter implemented in VHDL Language on Xilinx FPGA SPARTAN 3E kit.

The implementation of Remez Linear phase FIR filter of order 72 is done for the specifications characterizing an Equiripple FIR design method for a low pass response type and filter structure is Direct form symmetric FIR.

Experimental Results:


Filter Design & Analysis Tool - [fwizdef.mat *]
File Edit Analysis Targets View Window Help
Current Filter Information
Magnitude Response Estimate
Magnitude (dB)
0
-20
-40
-60
0
5
10
15
20
Frequency (MHz)
Store Filter ...
Filter Manager ...
Design Filter

Structure: Direct-Form FIR
Order: 72
Stable: Yes
Source: Designed

Response
● Lowpass
○ Highpass
○ Bandpass
○ Bandstop
○ Differentiator
Design
○ IIR Butterworth
● FIR Equiripple

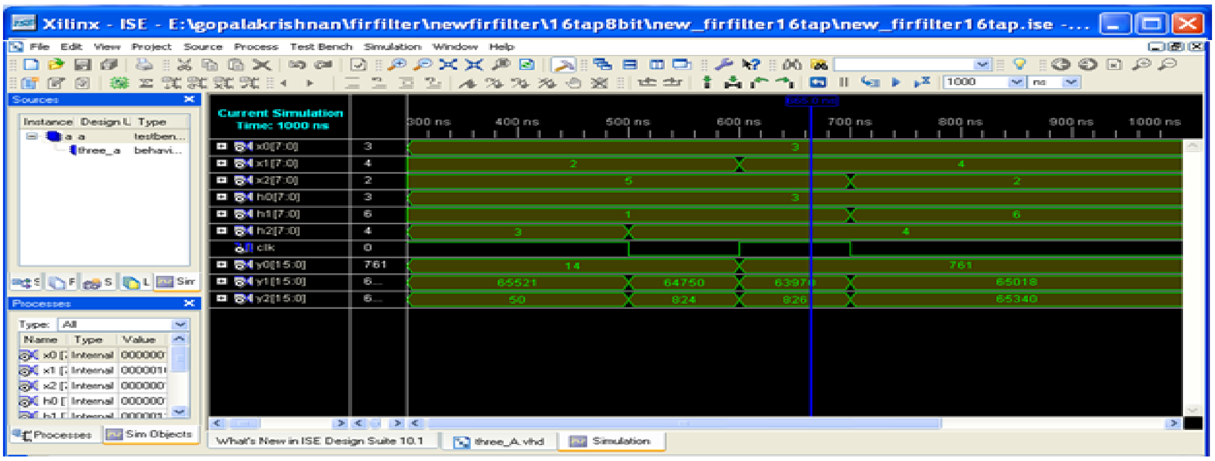
Filter
● Specify order: 72
○ Minimum order
Options
Density 16

Frequency
Units: kHz
Fs: 48000
Fpass: 9600
Fstop: 12000

Magnitude
Enter a weight value for each band below.
Wpass: 1
Wstop: 1

Computing Response ... done

Fig.10: Magnitude Response of Linear Phase Fir Filter of Order 72 with Symmetry Co-Efficients



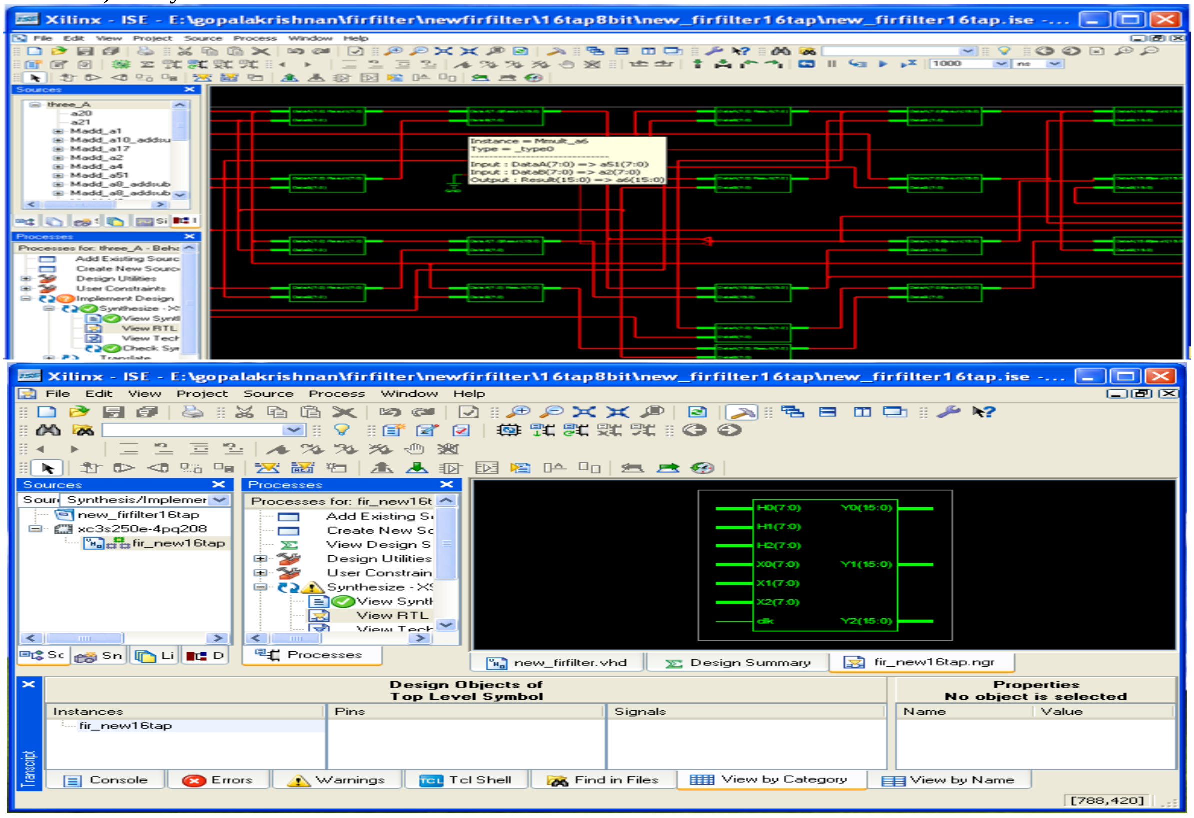
x0[7:0]	3	3
x1[7:0]	4	2, 4
x2[7:0]	2	5, 2
h0[7:0]	3	3
h1[7:0]	6	1, 6
h2[7:0]	4	3, 4
clk	0	
y0[15:0]	761	14, 761
y1[15:0]	6...	65521, 64750, 63970, 65018
y2[15:0]	6...	50, 824, 826, 65340

Fig.9.Output Wave form of proposed three - Parallel 72 tap FIR Filter. (8 bit)

This above results shows the proposed 3X3 parallel linear phase fir filter of order 72 with symmetric co-efficient in terms of Area, Power and critical path delay. Area can be calculated with the help of number of gates used in Field Programmable Gate Arrays. Also the power utilization is measured with the help of Xilinx 9.2i under the various power consumption levels like static, dynamic and leakage power consumption. Power consumption is depends on area utilized. i.e., number of gates to be used. As the above both simulation and synthesis results clearly shows, the circuit complexity in terms of area, power and delay of 72 order Linear phase proposed parallel FIR Digital Filters as listed below in Table II, and also comparison of various sub-filter methods of proposed for linear phase fir filter structures under the different level of parallelism. Validated the proposed techniques on Spartan 3E device where the significant area is observed and power reductions in both Common Sub expressions elimination (CSE) and Level Constrained Common Sub expression Elimination (LCCSE) techniques. Comparing the Proposed methods in sub-filter sections with conventional methods,

1. Using proposed LCCSE algorithm
   - a) Power consumption 68.768% reduced
   - b) Area 75.506% reduced
   - c) Delay 30.95% reduced
2. Using CSE algorithm

a) Power consumption 24.354% reduced
b) Area 36.433% reduced
c) Delay 20.4% reduced



Instance = Mmult_a6
Type = _type0

Input : DataA(7:0) => a51(7:0)
Input : DataB(7:0) => a2(7:0)
Output : Result(15:0) => a6(15:0)

Fig.10. RTL Schematic View of proposed three- parallel 72 tap FIR Filter (8bit).

Parameter	Conventional Parallel FIR Filter	Existing FFA Structure	Proposed FFA Structure
Slices	412	243	180
Flip Flops	305	192	171
4input LUTs	503	407	263
Delay(ns)	46.011	19.2385	15.725
Power(mW)	10.3478	12.1451	11.7805

Table II. Synthesis Result of 16 tap three- parallel Proposed Fir filter (8 bit)

V. Conclusion & Future Work

The new parallel FIR filter structures has proposed, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3.(i.e., Even length based). Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The proposed new structure exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. Since multipliers outweigh adders in hardware cost, it is profitable to exchange multipliers with adders. Consequently, the larger the length of FIR filters is, the more the proposed structures can save from the existing FFA structures, with respect to the hardware cost. The new parallel FIR structures consisting of advantages in both polyphase decompositions dealing with symmetric convolutions comparatively better than the existing FFA structures in terms of hardware consumption.

The proposed new parallel FFA Structures For FIR filters are an area efficient. Since, approximately 40% of the area is saved with this technique as compared to conventional and existing FFA FIR filter design. Area efficiency and high speed is achieved with new parallel FFA technique at very slight cost of power consumption for large tap FIR filter. Since, Parallel FIR filters are an area efficient and contained less delay, so these filters can be used in various applications such as pulse shaping FIR filter in WCDMA system, software design radio and signal processing system for high speed. In future this work can be extended for designing Odd length based FIR filters with less hardware complexity.

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