

Power Optimized Multiplexer Based 1 Bit Full Adder Cell Using .18 μm CMOS Technology

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Abstract: *In this paper, a multiplexer based 1 bit full adder cell using 10 transistors is reported (MBFA-10T). In addition to higher speed , low power and reduced transition activity, this design has no direct power supply connections, results in reduced consumption of short circuit current. The design was implemented using Cadence Virtuoso tools in 180-nm CMOS technology. Performance parameters like layout area, power delay product(PDP), transistor count, average power and delay were compared with the existing logic design styles like static CMOS logic, pass transistor logic(TFA-16T, 14 T) , transmission gate logic and so on. The intensive simulation shows improved operation speeds and power savings compare to the conventional design styles. For 1.8-V supply at 180-nm CMOS technology, the average power consumption (3.9230 μW) ,delay (196.8ps) ,the power delay product (PDP) (0.772fJ) and lay out area(175.79 μm^2) was found to be extremely low, when compared with other potential design styles.*

Keywords: *Multiplexer, full adder ,Very large scale integration(VLSI), low power, Complementary metal oxide semiconductor(CMOS).*

I. Introduction

Arithmetic operations such as addition , subtraction, multiplication, comparisons are all commonly used in VLSI based design of microprocessors and system components in portable consumer electronics[1]-[3]. The demand for small area low power microelectronics has increased and remain as a key focus of research over the decade. Full adders, being the basic building cell of all arithmetic operations influence the overall performance of the entire system. The system overall performance can be significantly influenced by enhancing the performance of the full adders[4].

Several logic style approaches have been practiced in the past for the design of full adder cell. Each design styles has got its on advantages and disadvantages. A wide range of classical full adder designs using dynamic and logic styles have been observed in literature, see Fig.1. One of such design is the conventional static CMOS structure Fig. 1(a) with pull-up and pull down transistors which provides full output voltage swing and also efficient driving capabilities[5]. Due to the low mobility characteristics pull-up pMOS block compared to pull down nMOS , CMOS design has got its own drawback. The large input capacitances also results in the speed degradation of static CMOS circuit. Some other full adder implementations uses more than one logic styles, hence they are referred as hybrid logic styles. Some examples are 14-T adder, 16-T full adder, 10-T Hybrid full adder(10-HFA),16-T low power hybrid full adder (LPHFA) [5]-[10]. These designs uses different logic styles , and concentrated more on the reduction of number of transistors in the adder modules. This is mostly achieved by making use of low power logic styles like simple pass transistor, transmission gate logic etc[8]. In doing so the researchers often trade off other important requirements such as power consumption due to the short circuit current, layout complexity, reduced transition activity etc.

In this paper, we propose a power optimized multiplexer based full adder cell, named MBFA-10T, which uses five identical multiplexers and uses 10 transistors in total. The proposed design (MBFA-10T) is compared with different logic styles including 28-transistor static CMOS adder, 14-T adder, 16-T full adder, 10-T Hybrid full adder(10-HFA),16-T low power hybrid full adder(LPHFA) as shown in fig.1.The rest of the paper is organized as following. In section II the design of new adder is proposed. In Section III, we present the simulation results. The Section IV concludes the paper.

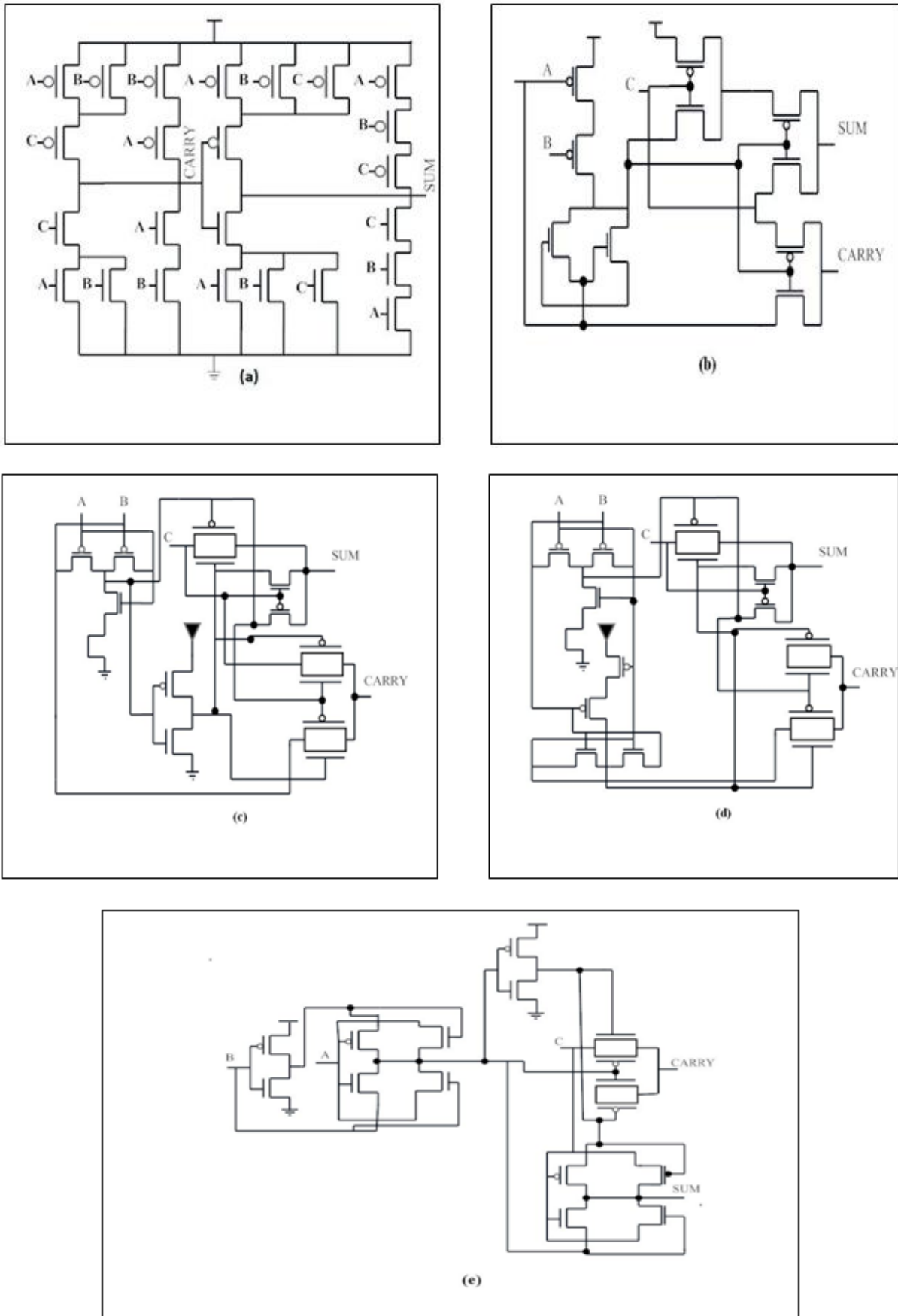


Fig. 1. Full adder cells of different logic styles a)Static CMOS b)10-T c)14-T d)16-T e) Hybrid full adder(HFA 16-T)

II. Proposed 1 Bit Multiplexer Based Full Adder

A 1-bit full adder architecture based upon five identical multiplexer gates is shown in Fig. 2(a). If each of the multiplexer gates are substituted by a two transistor circuit Fig. 2(b) it gives us the new MBFA-10T full adder, which requires a total of 10 transistors to realize the newly derived Boolean function of full adder as shown,

$$SUM = (A \oplus C)\bar{B} + (\overline{A \oplus C})B$$

$$CARRY = (A \oplus C)B + (\overline{A \oplus C})A$$

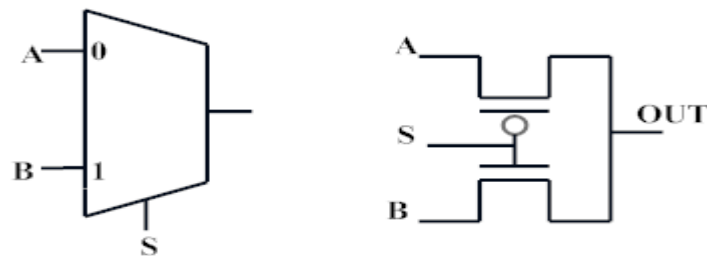
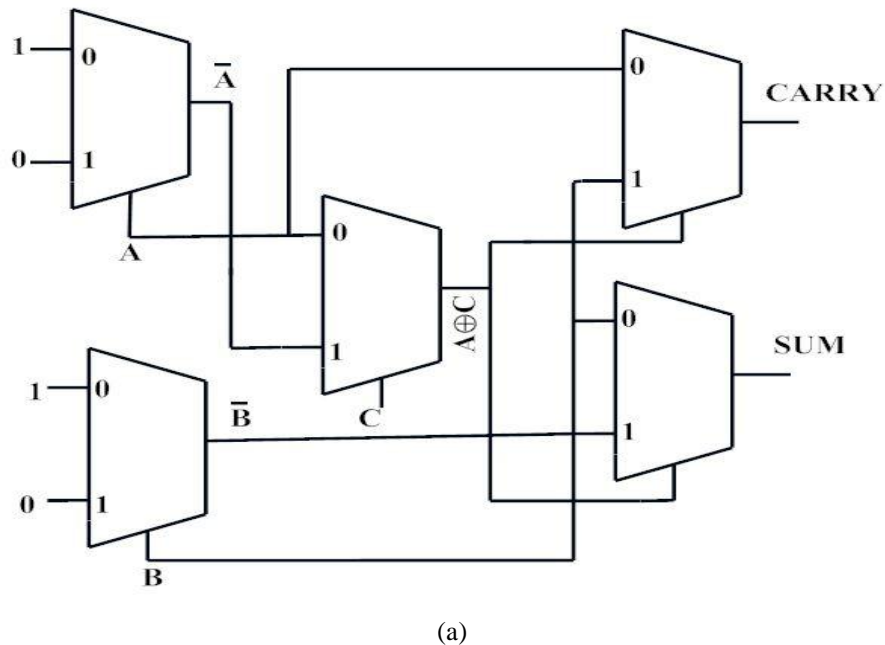


Fig. 2 (a) Architecture (b) 2-T multiplexer model

Examining the full adder's truth table in Table 1, it can be seen that the sum output is equal to $(A \oplus C)$ when $B=0$, and its equal to $(\overline{A \oplus C})$ when $B=1$. Thus a multiplexer can be used to obtain the expression keeping B as the select signal. Following, the same criteria can be employed for designing carry part of the full adder when $B=1$. it corresponds to $(A \oplus C)$ and also when $A=1$ its equal to $(\overline{A \oplus C})$.

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table-1 Full adder truth table: A, B and C are inputs; Sum and Carry are output

The new multiplexer based 1 bit full adder cell has 10 transistors. The three major components of power consumptions in digital CMOS VLSI circuits are i) Switching power ii) Short circuit power iii) Static power. Switching power is mostly consumed in the charging and discharging of the capacitances during the switching action of transistors. Short circuit power occurs due to the short circuit current flowing from the supply to the ground during the switching action of the transistors. Static power consumed due to the leakage effects of the static current while the circuit is in stable state. The first two power components are referred as dynamic components that contribute much to the total power consumption.

As the proposed design MBFA-10T adder cell does not have any direct connections to the supply(VDD) and the ground, the power consumption due to the short circuit component can be reduced to a greater extent. Accordingly the proposed full adder design consume less power than the standard adder cell implementations discussed earlier. The power optimized multiplexer based full adder cell design is shown in Fig. 3. The analytical reasoning's are made by circuit simulations in the following section.

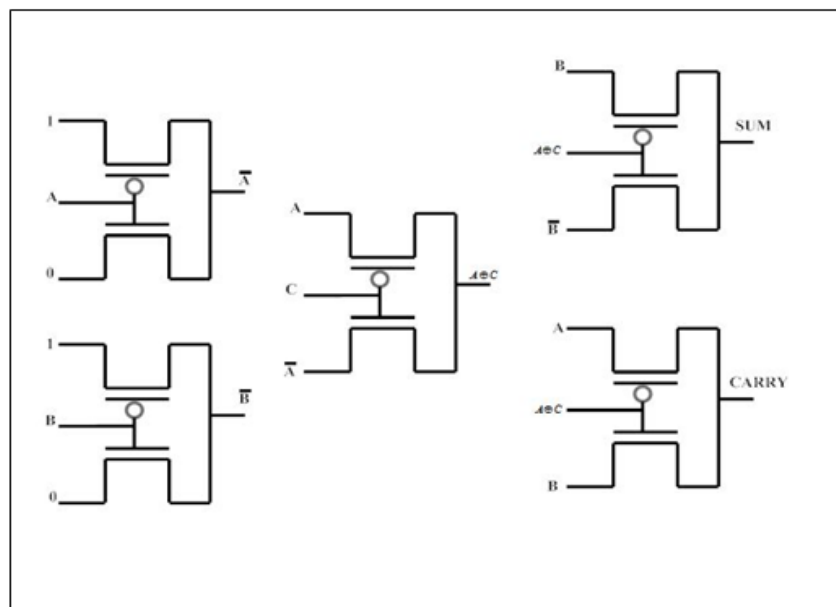


Fig. 3. The new MBFA-10T adder

III. Results And Analysis

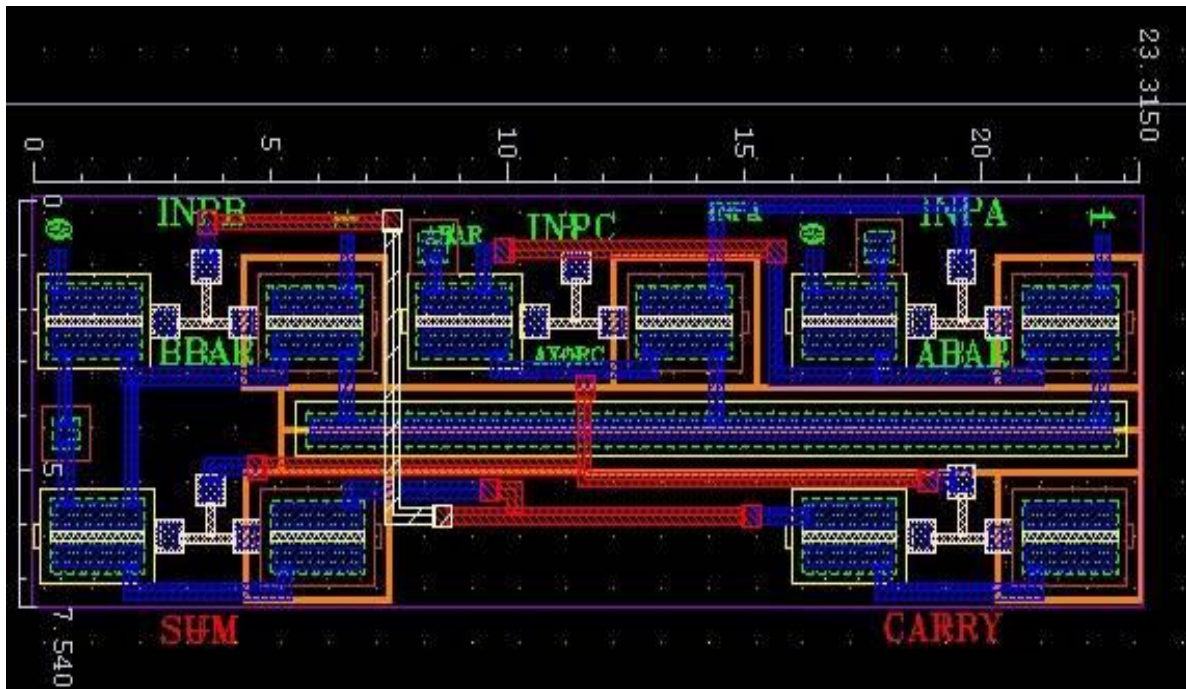
The simulation and analysis of the proposed full adder was carried out using Cadence Virtuoso tools in 180-nm technology with supply voltage 1.8V ,and compared with other potential design styles mentioned in[.]. With an aim to optimize the power and delay of the circuit , the energy consumption parameter power delay product (PDP) has been reduced to a great extend in the proposed design.

The average power consumed by the proposed full adder (MBFA-10T) is significantly less than that of the other potential adder designs. The use of less number of transistors (10-T) also helps in faster transition and reduced power consumption. The detailed comparison of the proposed full adder design with other adder designs is represented in Table 2.

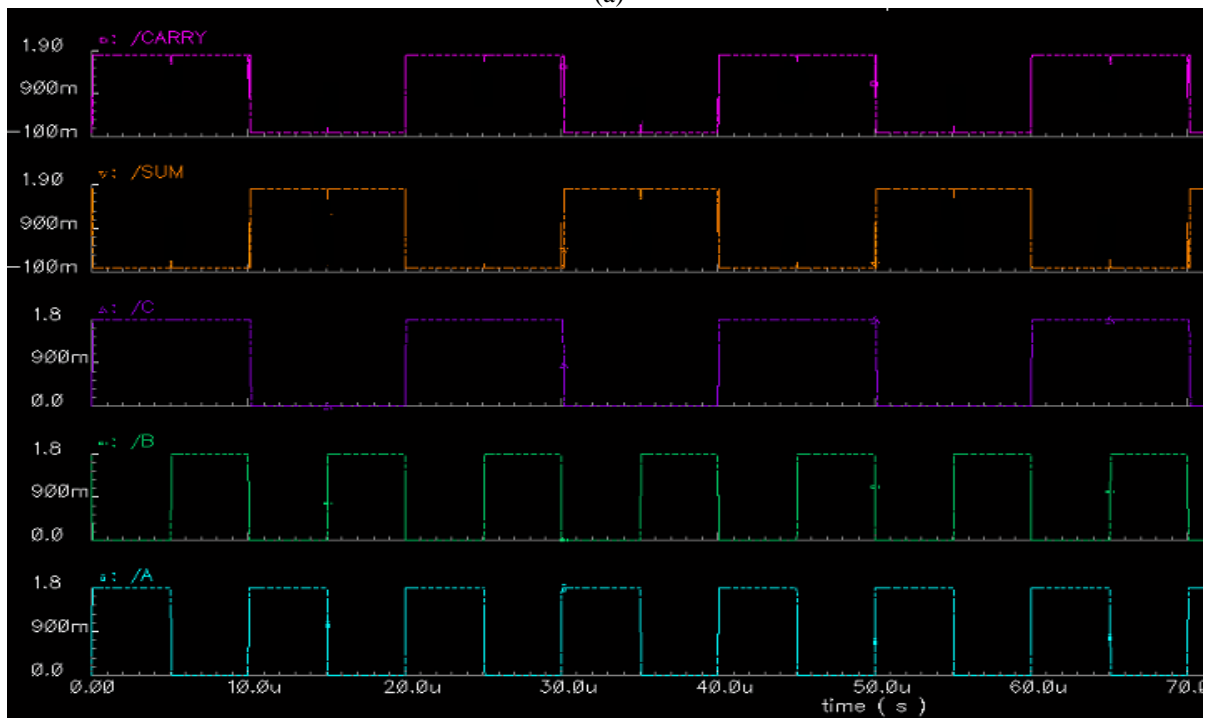
Design	Average Power (μW)	Delay (pS)	PDP ($\mu\text{W} \cdot \text{pS}$) (fJ)	Layout Area (μm^2)	Transistor Count	References
Static CMOS 28-T	6.1293	290.6	1.781	345.68	28	[5]
10-T Full adder	13.5682	130.59	1.771	190.56	10	[9]
14-T Full adder	12.2321	299.65	3.665	210.69	14	[8]
16-T Full adder	12.4341	205.9	2.560	254.56	16	[10]
Hybrid adder 16T	4.1524	223.4	0.927	218.02	16	[7]
Proposed adder	3.9230	196.8	0.772	175.79	10	

Table-2. Performance Analysis of various full adder cells at 0.18 μm CMOS process technology at 1.8V.

From the analysis , it is clear that the power consumption of the proposed multiplexer based adder cell is decreased by 35.99% , 71.06%, 67.9%, 68.44% and 5% over static CMOS adder, 14-T adder, 16-T full adder, 10-T Hybrid full adder(10-HFA) and 16-T low power hybrid full adder(LPHFA) respectively. Power delay product (PDP) of the MBFA-10T adder is reduced by 49.1%, 7.7%, 16.5%, 30.94% and 24 % as against the conventional 26T CMOS adder, 14-T adder, 16-T full adder, 10-HFA and 16-T (LPHFA) respectively.. The decrease in the transistor number eventually results in the optimized utilization of the cell area. The area in 180-nm technology is 175.76 μm^2 . Fig. 4(a) shows the layout of the proposed full adder. The simulation waveform obtained from Cadence Virtuoso tool is shown in Fig. 4(b).



(a)



(b)

Fig.4 (a) Layout of the multiplexer based full adder(MBFA) in 180-nm technology (b)Transient Response waveforms of Proposed Adder Cell (MBFA)

IV. Conclusion

In this paper , a power optimized multiplexer based 1- bit full adder (MBFA-10T) is introduced, which is built using 5 identical multiplexers and transistor count of 10. This full adder shows significant charge recycling capabilities and has very low short circuit current hence it is power optimized. Cadence EDA tool simulations have been performed to compare MBFA-10T and five other potential adder design styles., including 28-transistor static CMOS, 14-T full adder, 16-T full adder, 10-T Hybrid full adder(10-HFA) and 16-T low power hybrid full adder . Simulation results shows MBFA-10T is 49% speedier and consumes 26% less power than all other tested potential adders. Therefore, MBFA-10T is suitable for low power high speed VLSI systems.

References

- [1]. Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full Adders for Energy Efficient Arithmetic Applications," *IEEE Tran. on VLSI Systems*, Vol 19, No. 4, pp. 718-721, April 2011.
- [2]. N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, A System Perspective*. Reading, MA: Addison-Wesley.
- [3]. Y. Jiang, Al-Sheraidah. A, Y. Wang, Sha. E, and J. G. Chung, "A novel multiplexer-based low-power full adder," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 51, pp.345–348, July 2004.
- [4]. S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1320, Dec. 2006.
- [5]. C. Chang, J. Gu, and M. Zhang, "A review of 0.18-umfull adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.
- [6]. A. M. Shams, T. K. Darwish, and M. Bayoumi, "Performance analysis of low-power1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.
- [7]. P.Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, A. Dandapat, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit," *IEEE Trans Very Large Scale Integration (VLSI) Systems*, Volume: PP, September 2014.
- [8]. M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in *Proc. IEEE Workshop Signal Processing Systems*, Oct. 1999, pp. 713–722..
- [9]. H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10transistor full adders using novel XOR-XNOR gates," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 1, pp. 25–30, Jan. 2002..
- [10]. N. Zhuang and H. Hu, "A new design of the CMOS full adder," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 840–844, May 1992.