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Effects of Scaling on MOS Device Performance

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Abstract:*This paper presents effects on MOS transistor performance due to scaling of its dimensions. Scaling theory deals with the change in the device characteristics with the decrease in the dimensions of a MOS transistor. MOS transistors are continuously scaled down due to the desire for high density and high functionality VLSI chips. The driving forces behind these developments are increasing the demand for portable systems requiring high throughput and high integration capacity. Effects of scaling on the performance characteristics of a MOS device are analyzed in this paper.*

Keywords: *Scaling, constant field scaling, constant voltage scaling, threshold voltage, scaling factor*.

I. Introduction

Scaling of a MOS transistor is concerned with reducing the dimension of the device. The size of a MOS transistor is reduced by a factor of 0.7 in each technology generation [1]. Scaling results in the decrease of the dimensions of a MOS device, and thus increases the device density and functional capacity of the chip. More number of smaller MOS transistors is packed into a smaller chip area, and thus increases the device density and functional capacity of the chip. The cost of a VLSI chip depends upon the number of chips that can be produced per wafer. Smaller MOS transistors reduce the chip area, and thus allow more chips per wafer. This reduces the overall fabrication cost of the chip. MOSFET capacitances are also reduced, which in turn reduces the output switching time and switching power dissipation [1]. Despite some of the advantages, scaling of MOS device presents a series of challenges to device design. The electrical characteristics of a MOS transistor change with the reduction in the device dimensions. Further reducing the size of MOS transistors is restricted due to difficulties in device fabrication process and need for low voltages. Lowering the supply voltage reduces the switching speed of a MOS transistor. So, in order to maintain the same switching speed, its threshold voltage should be reduced at the same rate as the supply voltage is reduced. However, low threshold voltage MOS transistor results in increasing the subthreshold leakage power dissipation [2-3]. Thus, the relationship between power dissipation and switching speed is critical in obtaining optimal scaled MOS device. The internal MOS transistor characteristic is changed with the reduction in the dimension of MOS device, and thus the current flow characteristics also changes [4-5]. MOSFET characteristics degrade with the reduction in its physical dimension. Main characteristics are threshold voltage and subthreshold swing. Threshold voltage decreases and subthreshold swing increases because of two-dimensional (2-D) electrostatic charge sharing between the gate and the source-drain regions [6-7]. Consequently, the on-to-off current ratio is reduced substantially, which results in a significant increase in standby power and compromised overall performance [7]. Weaker electrical performance due to scaling of MOS transistor further necessitate for new initiatives in improving the performance of the device.

II. Mosfet Scaling

Fig. 1 shows the scaling of a MOS transistor by a scaling factor (S >1). Before scaling, the channel length and the channel width of the MOS transistor are W and L respectively. After scaling by a factor S, the dimensions of the scaled MOS device are W'=W/S and L'=L/S. The channel area of the MOS transistor before scaling is A=WL, whereas the channel area of the MOS transistor after scaling is A'= W'L'=A/S^2. Hence after scaling, the channel area of a MOS device reduces significantly. Two different scaling options are employed for scaling the MOS device. These different options are: constant field scaling and constant voltage scaling [8]. Both types of scaling methods have different effects on the performance characteristics of the MOS device.

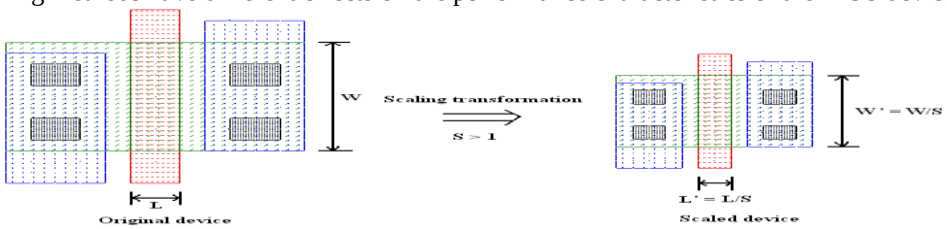

Fig.1 MOSFET Scaling

2.1 Constant Field Scaling

Fig. 2 shows constant field scaling in an nMOS transistor. In this scaling method [8], physical dimensions of a MOS transistor are scaled down by a scaling factor (S >1). Table 1 shows the MOS physical dimensions, potentials, and doping densities in constant field scaling. All terminal potentials and the threshold voltage of the MOS transistor are also scaled down by the same scaling factor (S). The doping densities (N_A and N_D) are increased by a factor S to maintain the charge densities and electric field relations.

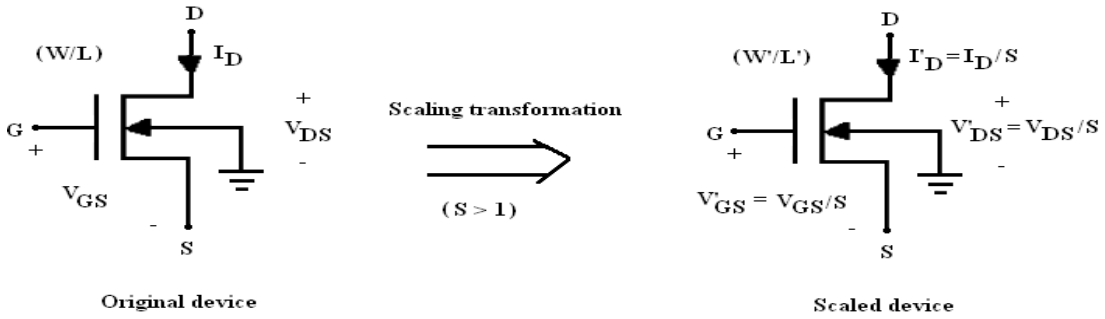

Fig. 2 Constant field scaling in a MOSFET

Table 1: MOS physical dimensions, potentials, and doping densities in constant field scaling [8]

Quantity	Symbol	Before Scaling	After Scaling
Channel length	L	L	L'= L/S
Channel width	W	W	W'= W/S
Channel area	A	A	A'= A/S
Gate oxide thickness	t_{ox}	t_{ox}	$t'_{ox}= t_{ox}/S$
Junction depth	x_j	x_j	$x'_j = x_j/S$
Supply voltage	V_{DD}	V_{DD}	$V'_{DD} = V_{DD}/S$
Gate to source voltage	V_{GS}	V_{GS}	$V'_{GS} = V_{GS}/S$
Drain to source voltage	V_{DS}	V_{DS}	$V'_{DS} = V_{DS}/S$
Substrate to source voltage	V_{BS}	V_{BS}	$V'_{BS} = V_{BS}/S$
Threshold voltage	V_{TH}	V_{TH}	$V'_{TH} = V_{TH}/S$
Doping densities	N_A N_D	N_A N_D	$N'_A = S. N_A$ $N'_D = S. N_D$

2.1.1 Effects Of Constant Field Scaling On Mos Device Performance

The effects of constant field scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (1) – (6).

$$\text{Gate oxide capacitance per unit area, } C'_{ox} = \varepsilon_{ox}/t'_{ox} = S.\ \varepsilon_{ox}/t_{ox} = S.\ C_{ox} \quad (1)$$

$$\text{Transconductance, } k'_n = \mu_n.C'_{ox}.W'/L' = S.\ k_n \quad (2)$$

$$\text{Drain current, } I'_D(\text{lin}) = k'_n/2.\ [2.(V'_{GS}-V'_{TH}).V'_{DS} - V'^2_{DS}]$$
$$= S.\ k_n/2.\ 1/S^2.[2.(V_{GS}-V_{TH}).V_{DS} - V^2_{DS}]$$
$$\text{Hence, } I'_D(\text{lin}) = I_D(\text{lin})/S \quad (3)$$

$$I'_D(\text{sat}) = k'_n/2.\ (V'_{GS}-V'_{TH})^2$$
$$= S.\ k_n/2.\ 1/S^2.\ (V_{GS}-V_{TH})^2$$
$$\text{Hence, } I'_D(\text{sat}) = I_D(\text{Sat})/S \quad (4)$$
$$\text{Power dissipation, } P' = I'_D\ .\ V'_{DS}$$
$$= 1/S^2.\ I_D\ .\ V_{DS}$$
$$\text{Hence, } P' = P/S^2 \quad (5)$$

$$\text{Power dissipation density, } P'_d = P'/(W'.\ L') = P_d \quad (6)$$

2.2 Constant Voltage Scaling

Fig. 3 shows constant voltage scaling in an nMOS transistor. In this scaling method [8], physical dimensions of a MOS transistor are reduced by a scaling factor (S>1). Table 2 shows the MOS physical dimensions, potentials, and doping densities in constant voltage scaling. The supply voltage, terminal voltages,

and the threshold voltage in a MOS transistor remain unchanged in this scaling method. The doping densities (N_A and N_D) are increased by a factor of S^2 in order to maintain the charge densities and electric field relations.

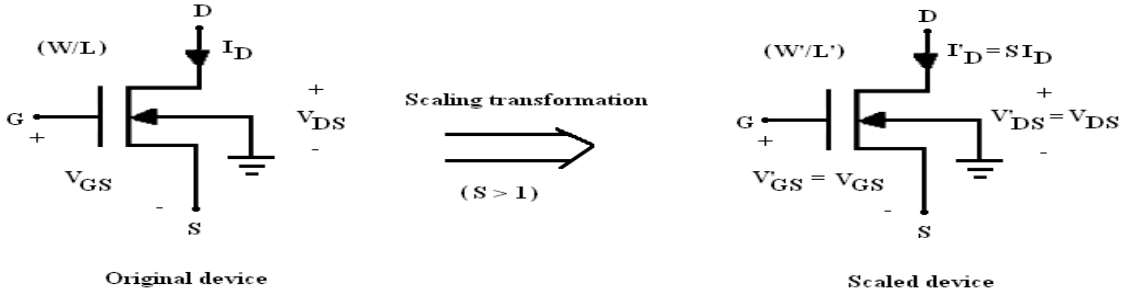

Fig. 3 Constant voltage scaling in a MOSFET

Table 2: MOS physical dimensions, potentials, and doping densities in constant voltage scaling [8]

Quantity	Symbol	Before Scaling	After Scaling
Channel length	L	L	L'= L/S
Channel width	W	W	W'= W/S
Channel area	A	A	A'= A/S
Gate oxide thickness	t_{ox}	t_{ox}	$t'_{ox}= t_{ox}/S$
Junction depth	x_j	x_j	$x'_j = x_j/S$
Supply voltage	V_{DD}	V_{DD}	$V'_{DD} = V_{DD}$
Gate to source voltage	V_{GS}	V_{GS}	$V'_{GS} = V_{GS}$
Drain to source voltage	V_{DS}	V_{DS}	$V'_{DS} = V_{DS}$
Substrate to source voltage	V_{BS}	V_{BS}	$V'_{BS} = V_{BS}$
Threshold voltage	V_{TH}	V_{TH}	$V'_{TH} = V_{TH}$
Doping densities	N_A N_D	N_A N_D	$N'_A = S^2.N_A$ $N'_D = S^2.N_D$

2.2.1 Effects Of Constant Voltage Scaling On Mos Device Performance

The effects of constant voltage scaling on MOS device performance such as gate oxide capacitance per unit area, transconductance, drain current, power dissipation, and power dissipation density are shown from equations (7) – (12).

$$\text{Gate oxide capacitance per unit area, } C'_{ox} = \varepsilon_{ox}/t'_{ox} = S.\ \varepsilon_{ox}/t_{ox} = S.\ C_{ox} \tag{7}$$

$$\text{Transconductance, } k'_n = \mu_n.C'_{ox}.W'/L' = S.\ k_n \tag{8}$$

$$\begin{aligned}\text{Drain current, } I'_D(\text{lin}) &= k'_n/2.\ [2.(V'_{GS}-V'_{TH}).V'_{DS} - V'^2_{DS}] \\ &= S.\ k_n/2.\ [2.(V_{GS}-V_{TH}).V_{DS} - V^2_{DS}] \\ \text{Hence, } I'_D(\text{lin}) &= S.\ I_D(\text{lin})\end{aligned} \tag{9}$$

$$\begin{aligned}I'_D(\text{sat}) &= k'_n/2.\ (V'_{GS}-V'_{TH})^2 \\ &= S.\ k_n/2.\ (V_{GS}-V_{TH})^2 \\ \text{Hence, } I'_D(\text{sat}) &= S.\ I_D(\text{Sat})\end{aligned} \tag{10}$$

$$\begin{aligned}\text{Power dissipation, } P' &= I'_D\ .\ V'_{DS} \\ &= S.\ I_D\ .\ V_{DS} \\ \text{Hence, } P' &= S.\ P\end{aligned} \tag{11}$$

$$\text{Power dissipation density, } P'_d = P'/(W'.\ L') = S^3.\ P_d \tag{12}$$

III. Performance Analysis

Constant voltage scaling may be preferred over constant field scaling in many cases because the scaling of voltages may not be very practical in many cases. The peripheral and interface circuitry may require certain voltage levels for all input and output voltages, which in turn would necessitate multiple power supply voltages and complicated level shifter arrangements [9]. However, it is observed that by using constant voltage scaling in a MOS transistor, the drain current and power dissipation increases by a factor of S, while power dissipation density increases by a factor of S^3. This large increase in power dissipation density may cause serious reliability problems for the scaled transistor, such as electromigration, hot carrier degradation, oxide breakdown, and electrical over stress [9]. In constant voltage scaling, the performance enhancement results primarily from the improvement of the drain current. In constant field scaling, the drain current and power dissipation decrease by

S and S^2 respectively, while power dissipation density remains unchanged. In this scaling, a much higher off-state leakage is observed due to the scaling down of the threshold voltage.

IV. Conclusion

Reducing the device dimensions allows higher density and higher logic integration. As the device dimensions are systematically reduced through constant field scaling or constant voltage scaling, various physical limitations become increasingly more prominent, and ultimately restrict the amount of feasible scaling for some device dimensions. In constant field scaling, power dissipation decreases by S^2, while in constant voltage scaling, drain current increases by S. Hence, constant field scaling can be used in low power applications, while constant voltage scaling can be used in high switching speed applications. The appropriate scaling approach in a MOSFET may be used depending upon the applications.

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