High Speed, Low Offset, Low Power, Fully Dynamic Cmos Latched Comparator

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Abstract: *An improved design of CMOS dynamic latch comparator with dual input dual output with a simple design of three stages is represented. The basic disadvantages of latch type comparators are overcome by producing an edge triggered comparison. The circuit is designed for a resolution of 300nV and the power consumption is reduced to 450uW. It is designed for 1.8V DC supply voltage and 1 MHz clock frequency for PVT variations. The simulation of the comparator is done in Cadence® Virtuoso Analog Design Environment using 180nm technology. The error quotient is reduced less than 5% by adding a buffer stage. The delay is brought down to 5nS. The active area appreciably is reduced. Layout of the proposed comparator has been simulated in Cadence® Virtuoso Layout XL Design Environment. DRC and LVS have been verified.*

I. Introduction

A comparator is an electronic device, which is widely used in the design of analog to digital converters and mixed signal systems. Basically, a comparator is a device, which compares two signals(voltages) and produces the digital output based on the comparison made [1]. The sampled input signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. Comparators are used in several applications such as sensor circuits and analog to digital converters. The comparator basically consists of three blocks i.e., the preamplifier stage, the latch stage and the output buffer stage[3]. The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolate the input of the comparator from switching noise coming from latch stage. The latch stage is used to determine which of the input signals is larger and amplifies their difference. The output buffer amplifies the information from latch and out-puts a digital signal. The preamplifier based latch comparator, which combines a pre-amplifier at the input stage is used to obtain high speed and low power dissipation[2]. It also helps in obtaining high resolution and eliminates common mode noise in signal as well as reference. Due to these factors, the preamplifier based latch comparator is the best choice for high speed ADC's. In this paper, we present a new dynamic preamplifier based latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. Even though numbers of transistors in the proposed comparator are more but overall area and the power consumption is small when compared to conventional dynamic latched comparators. Figure 1 shows the block diagram of pre-amplifier based latch comparator.
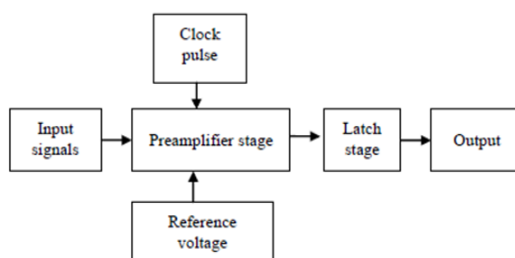
II. Block Diagram

Fig (1) Block diagram of preamplifier based latch comparator.

III. Basic operation

The comparator is a decision-making circuit. If the +, v+ input of the comparator is at a greater potential than the -, v- , input, the output of the comparator is a logic 1, whereas if the + input is at a potential less than the - input, the output of the comparator is at a logic 0[4].
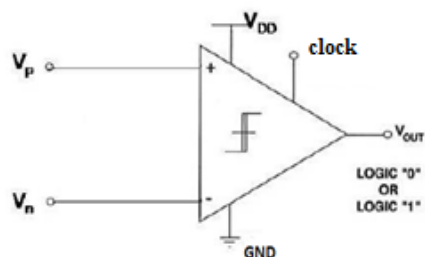
Fig (2) Schematic symbol and basic operation

IV.   Previous study

Latch type sense amplifiers are used to read the contents of the different kinds of A/D converters , data receivers , memory and on-chip transistors since they yield fast decision due to positive feedback. Using this sense amplifiers in low-voltage CMOS technologies is difficult because stack of the four transistors requires large voltage headroom. Also speed and offset of this amplifier is very much dependent on the common mode voltage of the input because of which it is difficult to use this amplifier in ADC's where large common mode ranges are used. Conventional latch type Comparator has high DC power consumption and adjustable threshold voltage.This comparator shows a high offset voltage and its high offset voltage dependency on a different common mode voltage, therefore it is only suitable for low resolution comparison.Strong dependency on speed and offset with a different common-mode input voltageand problem in low power supply voltage operation due to its structure can be overcome by using proposed architecture. The architecture is also prone to error in case of device mismatch which are overcome in the following proposed architecture.
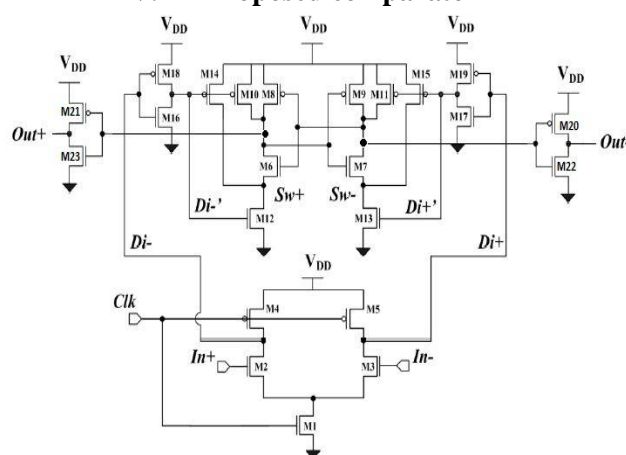
V.   Proposed comparator

Fig (3): circuit diagram.

The proposed comparator provides faster operation in addition to the advantages of those comparators such as reduced clock load, less kickback noise and removal of the timing requirement between Clk and complimented clk over a wide common-mode and supply voltage range(0.6V to 1.6V). The overall area is small. It is because of widths of transistors are optimized without compromising the speed and performance of the comparator. The table1 shows the transistor lengths and widths of proposed comparator.

Table 1:

Transistors	Aspect ratio(W/L)
M1	0.2880
M2,M3	0.8916
M4,M5	0.7320
M6,M7, M12,M13, M16,M17, M22,M23	1.3333
M18,M19, M20,M21	3.8888
M8,M9, M10,M11, M14,M15	2.9444

VI.   Working principle

For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistor M4 and M5 are turned on and they charge Di nodes' capacitance to VDD, which turn both NMOS transistor M16 and M17 of the inverter pair on and Di' nodes discharge to ground.Sequentially, PMOS transistor M10, M11, M14 and M15 are turned on and they make Outnodes and SW nodes to be charged to VDD while both NMOS transistors M12 and M13 are being off. During the evaluation (decision-making) phase (Clk=VDD), each Di node capacitance is discharged from VDD to ground in a different time rate proportionally to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between Di+ and Di- node. Once either Di+ or Di- node voltage drops down below around VDD−|Vtp|, the inverter pairs M18/M16 and M19/M17 invert each Dinode signal into the regenerated Di' node signal. Then the regenerated and different phasedDi' node voltages are amplified again and relayed to the output-latch stage by transistor M10−M13. As the regenerated each Di' node voltage is rising from 0V to VDDwith a different time interval, transistor M12 and M13 turn on one after another and the final amplification is made between SW nodes before the regeneration process. Once either of SWnode voltages falls below around VDD−Vtn, the output latch stage starts to regenerate the small voltage difference at Outnodes into a full-scale digital level. Once both the Di nodes are discharged the S-R latch gets the input as high on both ends this complication is eliminated by M14 and M15. The output inverters provide a sufficient segregation between the digital levels thus reducing the output ripple from the previous SR latch stage.

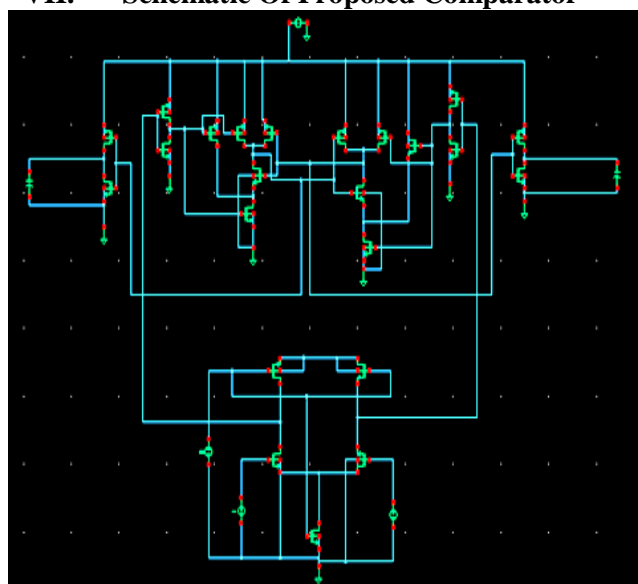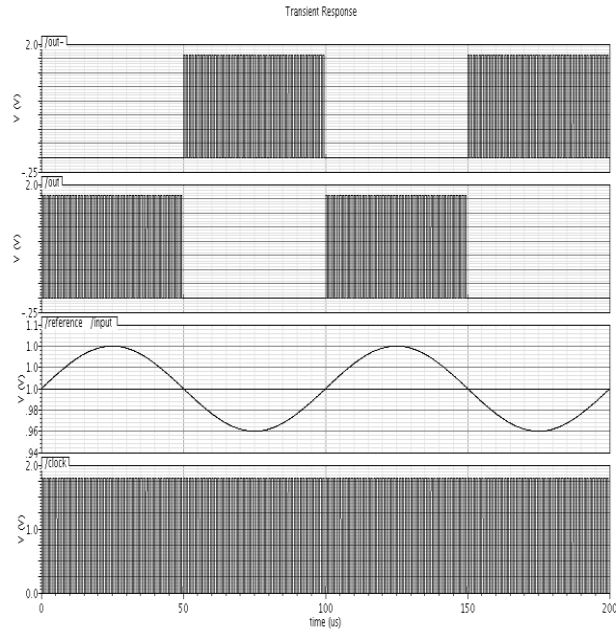## VII.   Schematic Of Proposed Comparator

Fig (4): schematic diagram.

VIII.   Simulation results:

Table 2:

Parameters	Desired value	Achieved value
Delay	5ns	4.78ns
Power consumption	500uw	431.2uW
Resolution	10mV	278nV
Type	Dynamic	Dynamic

Fig(5):Transient output of the proposed architecture

The following figure shows the transient response where in which if the given input(sinusoidal signal) goes above the reference, the output terminal reproduces the clock input. Else, the output remains at zero(gnd). the case is reversed in case of complimented output terminal.
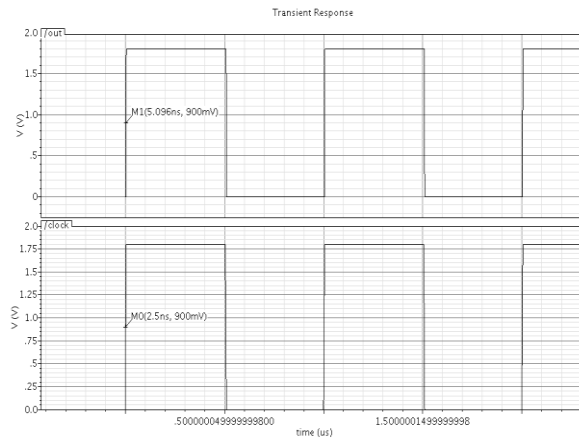

Fig(6): Delay calculation

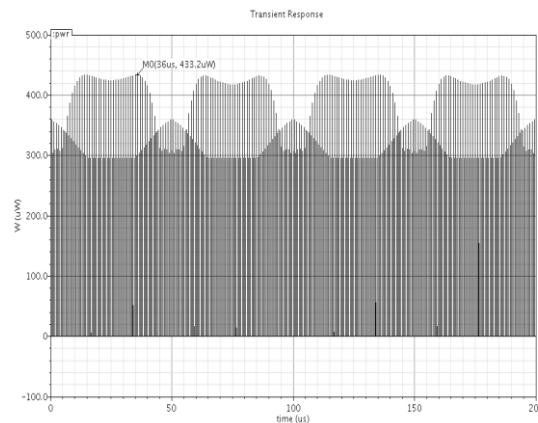The following figure shows the midpoint delay calculation at 27ºC. in typical C-mos environment.

Fig (7): Dynamic power consumption

The following figure shows the dynamic power consumption of the comparator. the static power consumption is obtained to be 390uW. And the dynamic power consumption is found to be around 450uW.
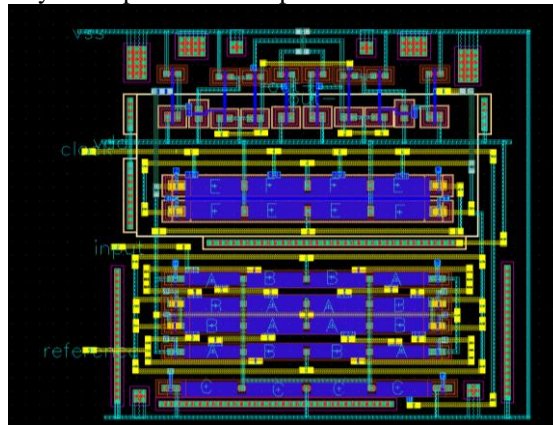

Fig (8): Layout of the proposed comparator

This following figure shows the typical, optimised layout structure for the proposed comparator.

IX.   Conclusions:

To justify the performance of the proposed comparator , the circuit was simulated in Cadence® virtuoso analog design environment. Technology used is 180nm technology with VDD=1.8V as supply voltage. The layout and schematic diagrams have been given in figures. Table 2 shows the result summary before post layout simulation. We can also infer that from Table 2, the speed is improved by a large amount. From Table 2, we can say that the power dissipation of proposed comparator, after post layout simulation is 450uW but it is still less than an optimum range. But in other aspects, it is still better than that of permissible limit.

The circuit was designed using 180nm technology with VDD=1.8V,$C_{load} = 100fF$,$f_{clk} = 1MHz$ Temp=25ºC common mode voltage $V_{com} = 0.6 \text{ to } 1.6\,V$, and simulated with Cadence® Virtuoso Analog Design Environment.

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