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"Power and Temperature Analysis of 12T CMOS SRAM Designed With Short Channel Devices"

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Abstract: *This paper focuses mainly on dynamic power dissipations at different temperature for both read and write operations of 12T SRAM. In the proposed 12T structure virtual vdd concept is employed because of this leakage current will reduce. Hence reduction in leakage current causes reduction in dynamic power. Power dissipation of the proposed SRAM cell have been determined and compared to those of some other existing memory cells. Proposed cell is a short channel BSIM4 model. It is observed that power dissipation of 12T SRAM for read operation at 40̊ is 44.7nw and for write operation it is 38.79nw. The proposed SRAM cell dissipates less power. Simulation has been done in Tanner-13 EDA tool for 50nm.*
Keywords: *BSIM4 model, Dynamic power, Low power SRAM, Virtual vdd.*

I. Introduction

Low power is the main issue in SRAM design. Many techniques have been employed to fulfill these requirement such as supply voltage scaling, mutli threshold CMOS (MTCMOS) etc. [1] have proposed 12T SRAM using charge recycling technique. In this paper total power dissipation at different temperature is calculated and compared with existing RAM cells. It is observed that Power consumption of 12T SRAM is very less compared to other SRAM cells. Static noise margin at different pull up ratio is also calculated and compared those with previous SRAM cells. Microwind 3.1 is used for schematic and layout purpose. According to [2] separate static and dynamic power and power delay product of 12T SRAM is calculated and compared with previous existing cells. Charge recycling technique is used for ckt. operation which is nothing but applying a transmission gate between virtual supply and ground. Microwind 3.1 is used for schematic and layout purpose.

According to[4], voltage scaling is most powerful power reduction technique. In this author suggested that using large cells results in increase in total SRAM area, hence attention must be paid for a low vdd min through increased area. Balancing cell size i.e redundancy or ECC(error correction coding) helpful for minimizing total SRAM area. Main technique to reduce the vdd min is the redundancy technique. Column redundancy implementation using shift redundancy is developed. In this technique, if any cell in a column fails next column replaces the failed column and next column replaced with the column next to it and so on. Finally author suggested that redundancy, ECC, appropriate cell sizing yield optimized SRAM design with minimum area which will reduce vdd min. This method is for 6T SRAM same method is applicable for other SRAM cells[4].

In this paper 12T SRAM short channel BSIM4 model is proposed. In this model virtual vdd concept has been employed, in which vdd is given to the circuit. only when it is needed and during hold time no vdd is given to the circuit. due to this concept leakage current will be reduced. Existing SRAM cells has single ended output but in proposed SRAM cell has single ended output with transmission logic. Transmission logic will give output as only high logic level and low logic level because of this leakage current will reduce which will eventually reduce the overall power consumption.

II. Basic Sram Cell Design

A. 6T Working (Read):

- Precharge both bitlines high
- Then turn on wordline
- One of the two bitlines will be pulled down by the cell
- Ex: A = 0, A_b = 1
  - bit discharges, bit_b stays high
  - But A bumps up slightly
- Read stability
  - A must not flip

N1 >> N2

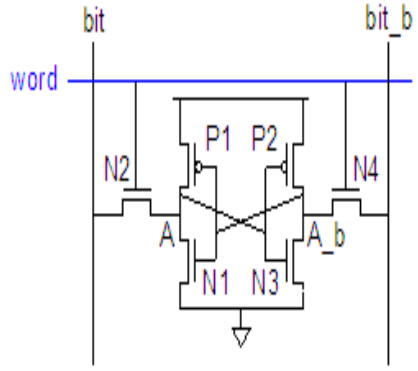

Fig.1

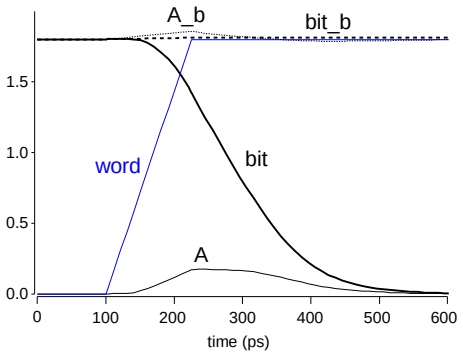

Fig.2

B. 6T Working (Write):

- Drive one bitline high, the other low
- Then turn on wordline
- Bitlines overpower cell with new value
- Ex: A = 0, A_b = 1, bit = 1, bit_b = 0
  - Force A_b low, then A rises high
- Writability
  - Must overpower feedback inverter
  - N2 >> P1

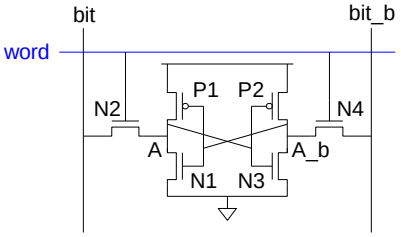

Fig.3

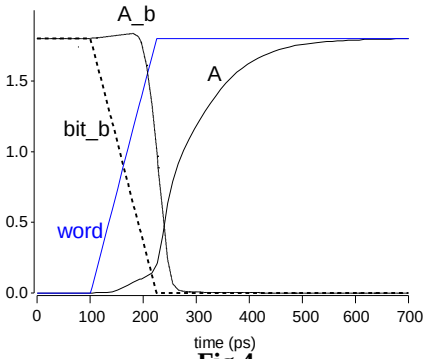

Fig.4

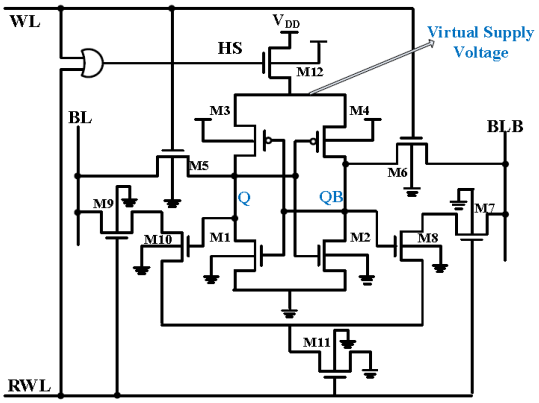

Fig.5 Proposed 12 T SRAM cell.

The proposed SRAM cell is demonstrated in Fig 5.This structure consist of ten transistors which six main transistors are same as conventional 6T. The four additional transistors respect with 6T are used to separating the read and write path of cell. The cell is single ended structure which does the read operation from one side of cell. Using separated path for read and write operation increases the control over the array of the cell in the catch design by simultaneous read and write operations which is in contrast with shared access path as conventional 6T cell. Circuit functionality modes are; Write, read and hold mode. The state of the control signals for choosing between these modes is archived in Table 1. The WWL and RWL are independent signals

and Hold Signal (HS) is produced by them (see Fig 5). Both write and read modes are called active mode. For choosing between active and idle (hold) mode, M12 transistor is used on the top place which separates virtual supply voltage from supply voltage rail. This transistor acts as a power gating transistor. In active mode the M12 transistor should be in ON mode by producing zero in HS signal (HS=0). After that the write and read operation can be done. The characteristic of cell in different modes is discussed in below parts.

Cell modes	WWL	RWL	HS=(WWL) R (RWL)
Read	0	1	1
Write	1	0	1
Hold	0	0	0

Table 1. States of control signal.

Write Operation:

The write paths proposed architecture consist of two transistors (M5 and M6). In write mode, these transistors activate with WWL signal and write the value of BL and BLB on the storage nodes. The write operation can be performed at supply voltages as lower voltage. Inability of access transistors to change the cell's value in write operation is called write failure.

Read Operation:

The read operation is done only from QB storage node. In this mode RWL signal becomes one and Bl and BBL pre-charge to one. When cell saves the one, (Q=1 and QB=0) the M10 becomes ON and reads the Q node by passing the current through M8 and M9. On the other case, when zero is saved in cell (Q=0 and QB=1) the M8 becomes ON and BLB line discharges thorough M7 and M1.

III. Circuit Designs And Simulations

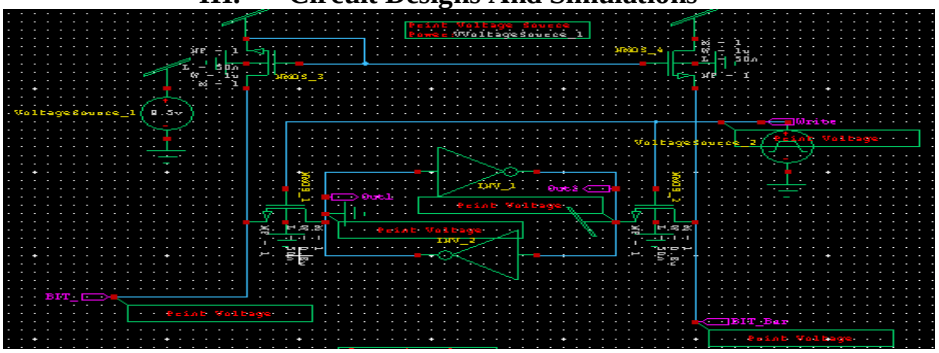

Fig.6 Design of 6t SRAM for read operation

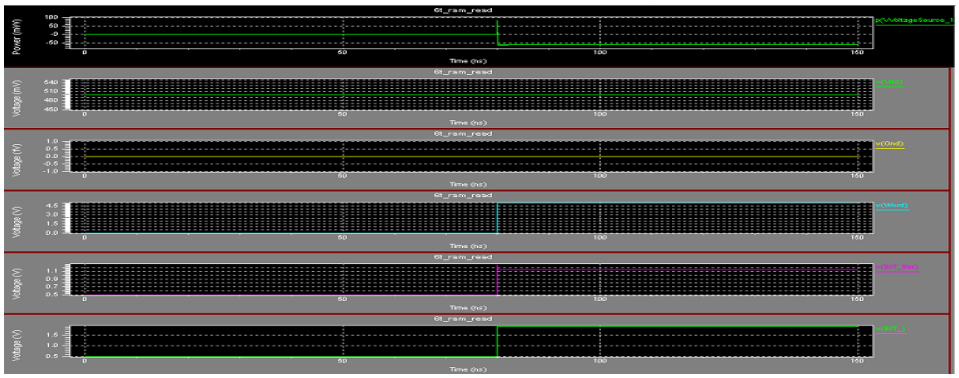

Fig.7 Simulation result of 6T read

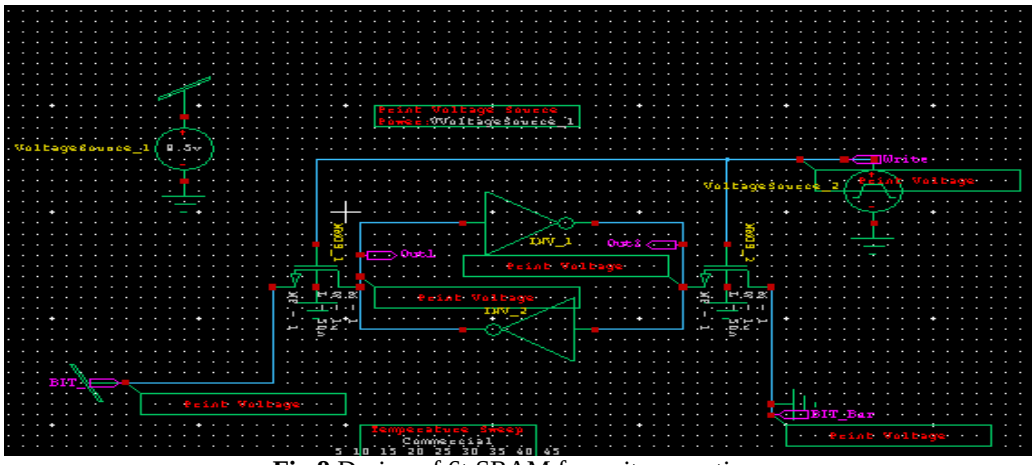

Fig.8 Design of 6t SRAM for write operation.

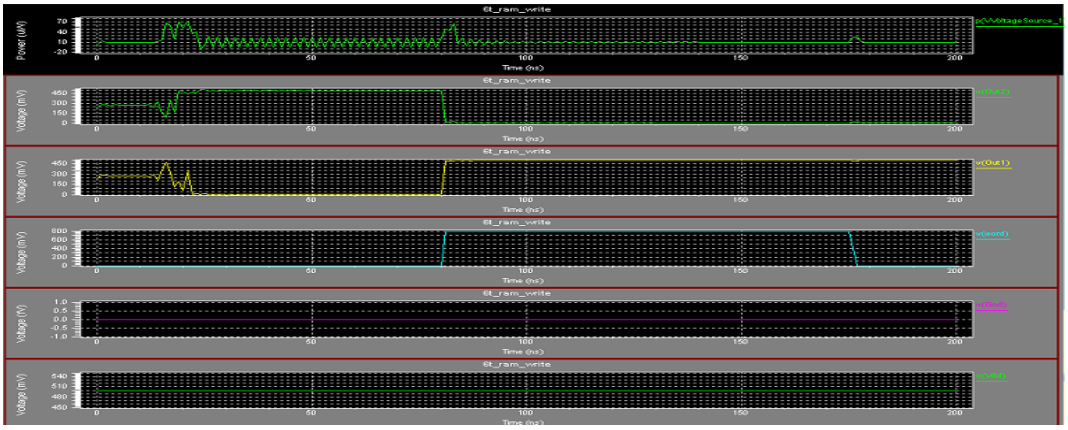

Fig.9 Simulation result of 6T write

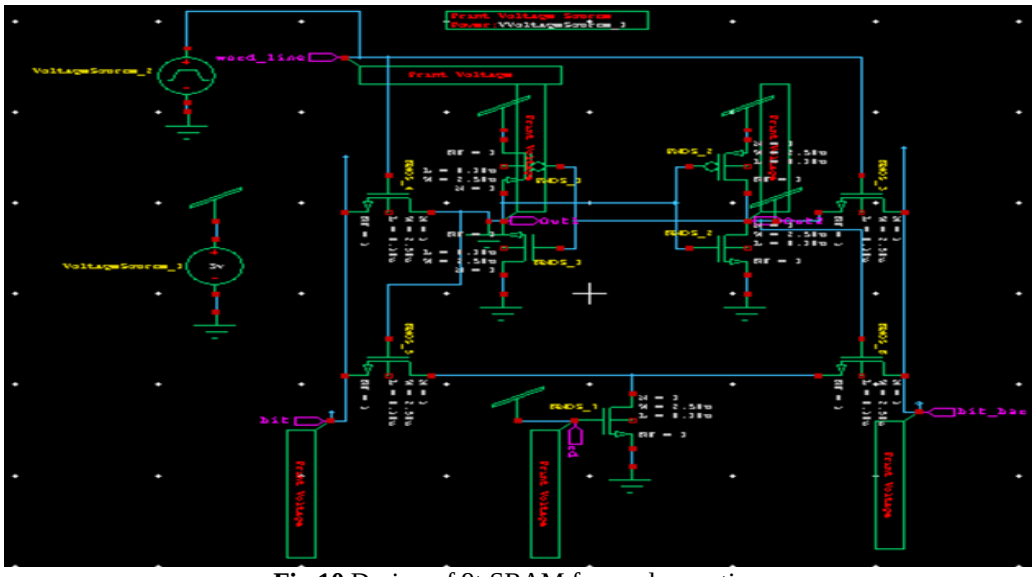

Fig.10 Design of 9t SRAM for read operation

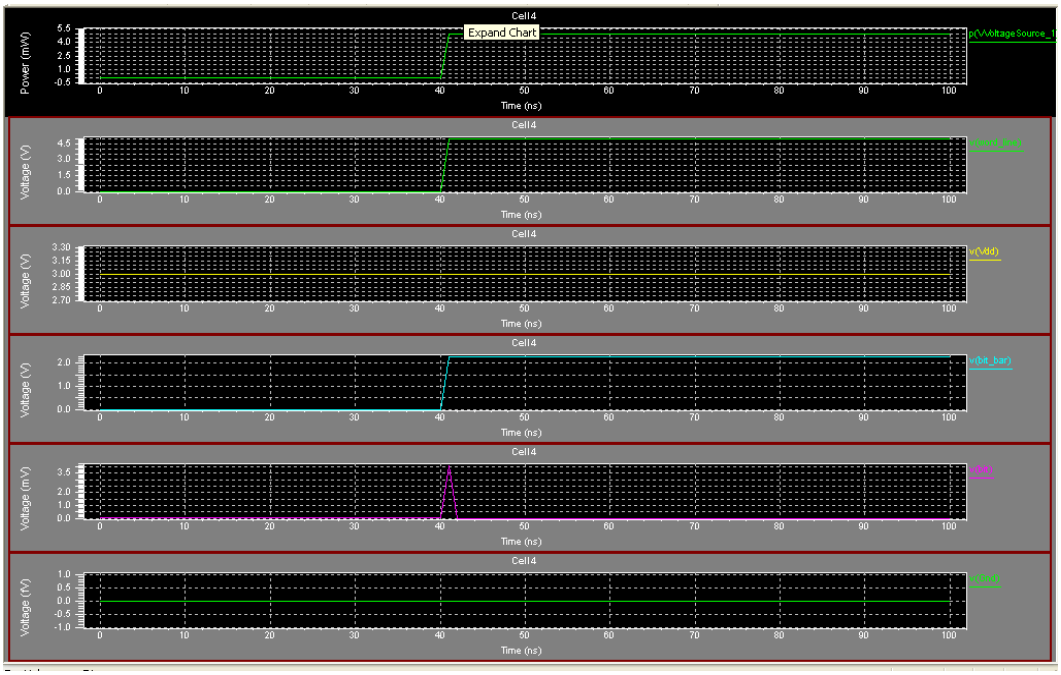

Fig.11 Simulation of 9t SRAM for read operation.

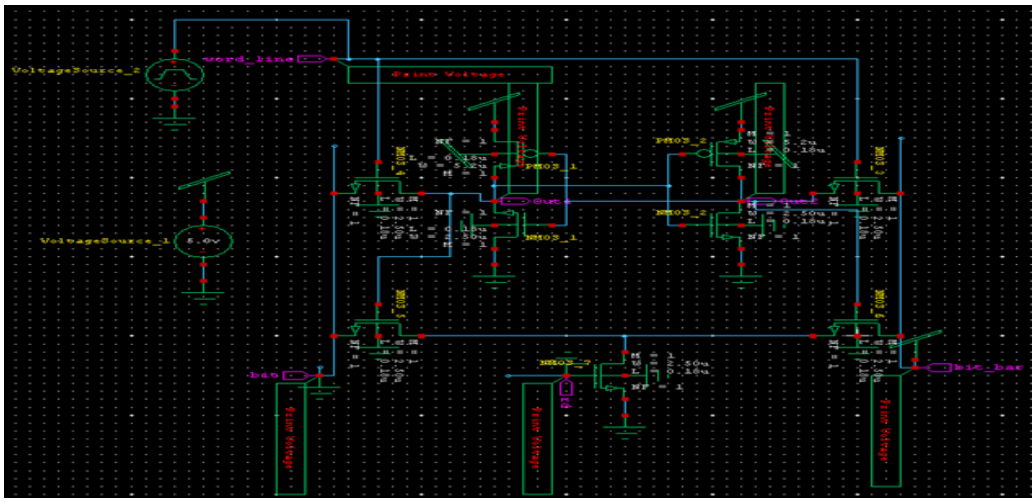

Fig.12 Design of 9t SRAM for write operation

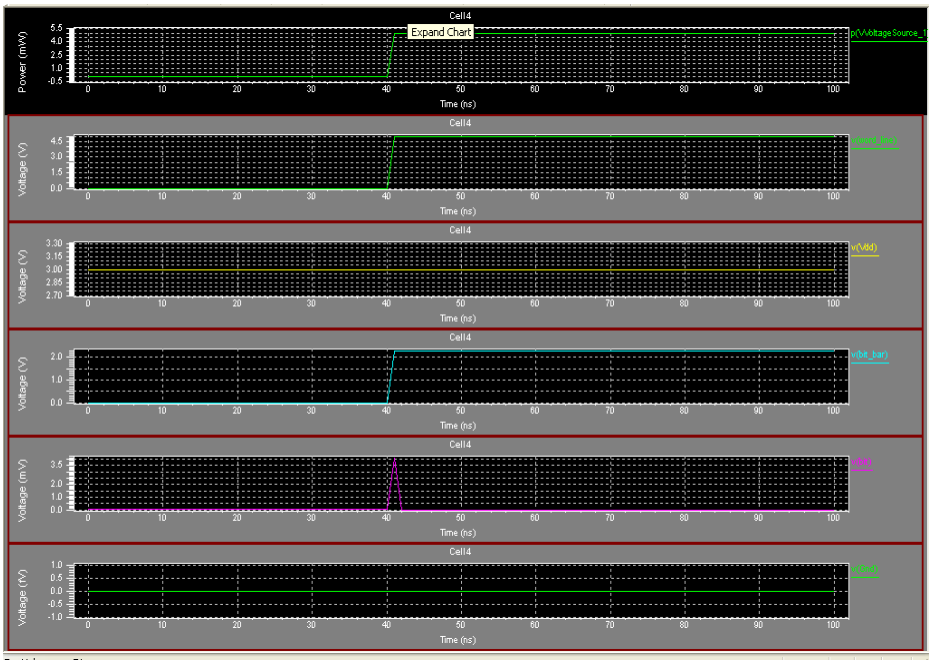

Fig.13 Simulation of 9t SRAM for write operation

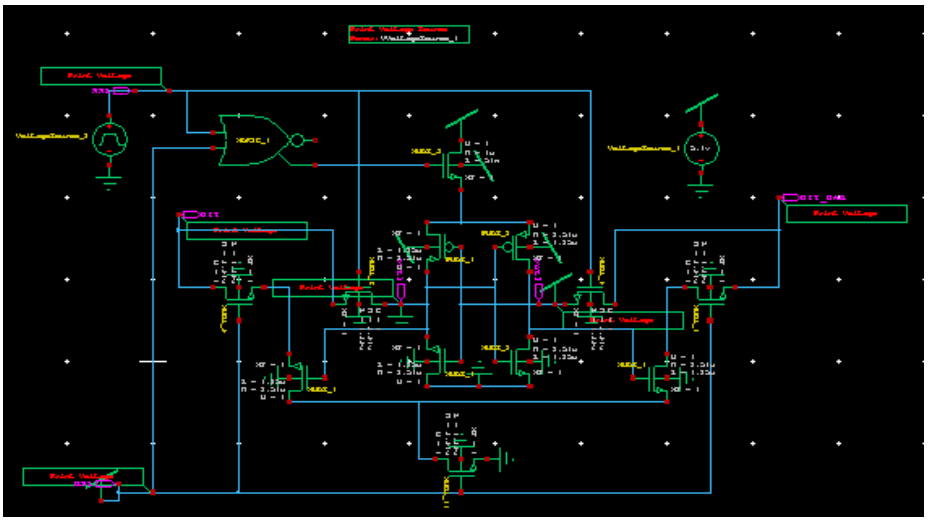

Fig.14 Design of 12t SRAM for read operation

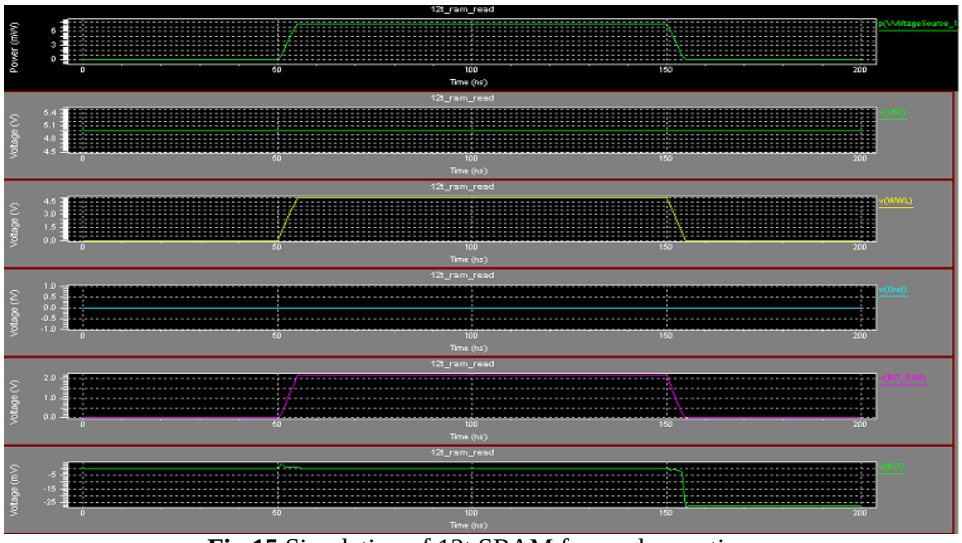

Fig.15 Simulation of 12t SRAM for read operation.

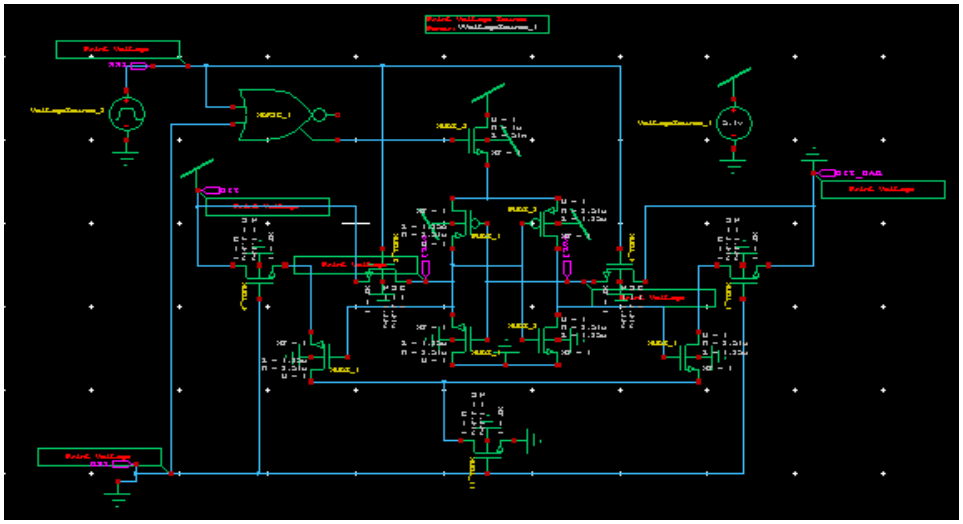

Fig.16 Design of 12t SRAM for write operation.

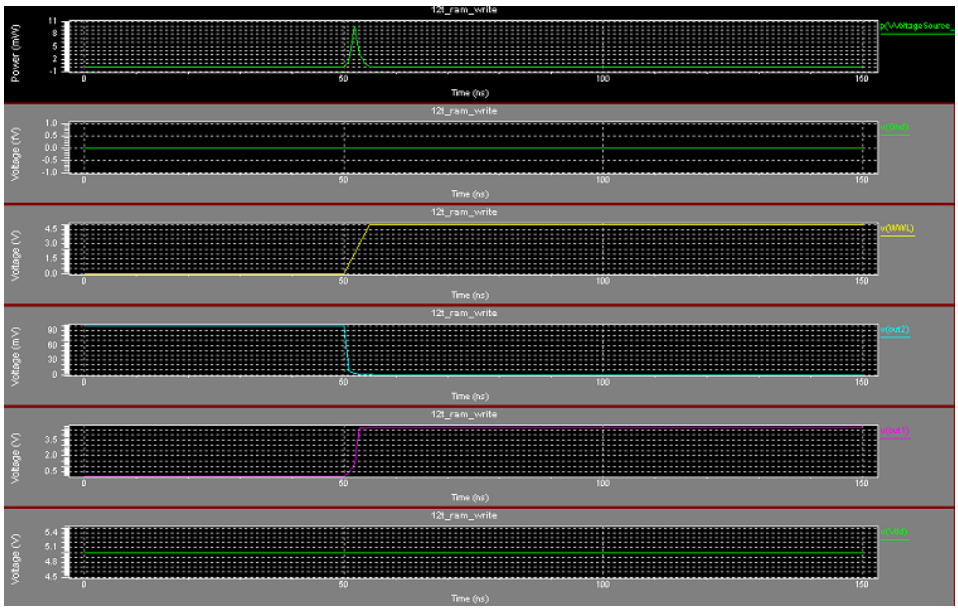

Fig.17 Simulation of 12t SRAM for write operation

IV. Results And Discussion

In this section power dissipation for separate read and write operation at different temperature is calculated and compared those with previous existing RAM cells. It is observed that power consumption of 12T SRAM is very less compared to other SRAM cells. Average power is calculated by formula P=V X I. Schematic simulations have been done at 50nm technology with the help of Tanner 13 EDA tool by using BSIM4 model.

Table3 shows the comparison of total power dissipation (dynamic power) for read operation at different temperatures for existing SRAM cells and proposed 12T SRAM cell.

Table4 shows the comparison of total power dissipation for write operation at different temperatures for existing SRAM cells and Proposed 12T SRAM cell. The proposed cell dissipates less power than other existing cells for write operation.

Table3. Power consumption readings of memory cells for read operation

Temperature (c)	6T SRAM	8T SRAM	9TSRAM	11T SRAM	12T SRAM
5	$1.24075x10^{-8}$	$1.5556 x10^{-8}$	$1.8151 x10^{-8}$	$4.4208 x10^{-7}$	$2.0626 x10^{-8}$
10	$1.3336x10^{-8}$	$1.6854 x10^{-8}$	$2.0225 x10^{-8}$	$4.912 x10^{-7}$	$2.2731 x10^{-8}$
15	$0.2217 x10^{-8}$	$1.8336 x10^{-8}$	$2.2459 x10^{-8}$	$5.462 x10^{-7}$	$2.5197 x10^{-8}$
20	$0.2216 x10^{-8}$	$2.0041 x10^{-8}$	$2.4863 x10^{-8}$	$6.081 x10^{-7}$	$2.8070 x10^{-8}$
25	$0.2215 x10^{-8}$	$2.2007 x10^{-8}$	$2.745 x10^{-8}$	$6.7825 x10^{-7}$	$3.1402 x10^{-8}$
30	$1.8755 x10^{-8}$	$2.4272 x10^{-8}$	$2.0232 x10^{-8}$	$7.5805 x10^{-7}$	$3.5246 x10^{-8}$
35	$2.0639 x10^{-8}$	$2.6875 x10^{-8}$	$3.3224 x10^{-8}$	$8.4915 x10^{-7}$	$3.9663 x10^{-8}$
40	$2.2781 x10^{-8}$	$2.9857 x10^{-8}$	$3.6446 x10^{-8}$	$9.534 x10^{-6}$	$4.4715 x10^{-8}$

Table 4. Power consumption readings of memory cells for write operation

Temperature (c)	6T SRAM	8T SRAM	9TSRAM	11T SRAM	12T SRAM
5	$1.8598 x10^{-6}$	$3.3892 x10^{-6}$	$4.6712 x10^{-6}$	$4.5074 x10^{-6}$	$1.9542 x10^{-8}$
10	$2.0097 x10^{-6}$	$3.6723 x10^{-6}$	$5.0695 x10^{-6}$	$4.8923 x10^{-6}$	$2.1167 x10^{-8}$
15	$2.1664 x10^{-6}$	$3.9692 x10^{-6}$	$5.488 x10^{-6}$	$5.297 x10^{-6}$	$2.3087 x10^{-8}$
20	$2.3297 x10^{-6}$	$4.2799 x10^{-6}$	$5.9275 x10^{-6}$	$5.721 x10^{-6}$	$2.5347 x10^{-8}$
25	$2.4996 x10^{-6}$	$4.6044 x10^{-6}$	$6.387 x10^{-6}$	$6.165 x10^{-6}$	$2.7996 x10^{-8}$
30	$2.6761 x10^{-6}$	$4.9628 x10^{-6}$	$6.868 x10^{-6}$	$6.629 x10^{-6}$	$3.1086 x10^{-8}$
35	$2.8592 x10^{-6}$	$5.295 x10^{-6}$	$7.3695 x10^{-6}$	$7.113 x10^{-6}$	$3.4669 x10^{-8}$
40	$3.0488 x10^{-6}$	$5.661 x10^{-6}$	$7.8925 x10^{-6}$	$7.6175 x10^{-6}$	$3.8799 x10^{-8}$

V. Conclusion

Low power is major issue in CMOS VLSI design. In this paper low power 12T BSIM4 SRAM has been proposed which dissipates lesser dynamic power compared to existing SRAM cell. Simulation has been done at different temperatures for total power dissipation. In proposed SRAM cell the virtual vdd concept reduces the dynamic power at different temperatures. Hence power efficiency with virtual vdd concept and shrinking technology file has been achieved in this paper. Proposed design with virtual vdd concept is a promising solution for low power designs.

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