Performance Comparison of Various Clock Gating Techniques

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Abstract: *Clock signal have been a great source of power dissipation in synchronous circuits because of high frequency and load. So , by using clock gating one can save power by reducing unnecessary switching activity inside the gated module. Here four gating methods are discussed and their power dissipation is compared. The most popular is synthesis-based, deriving clock enabling signals based on the logic of the underlying system. It unfortunately leaves the majority of the clock pulses driving the flip flops (FFs) redundant. A data driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called auto gated FFs (AGFF) is simple but yields relatively small power savings. Another novel method called Look Ahead Clock Gating (LACG) is presented, which combines all the three.It avoids the tight timing constraints of AGFF and data driven by allotting a full clock cycle for the computation of the enabling signals and their propagation.*
Keywords: *AGFF,LACG, Flip Flops, Clock Gating*

I. Introduction

The sequential circuits in a system are considered major contributors to the power dissipation since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. To distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the capacitance of the clock net. Recent studies indicate that the clock signals in digital computers consume a large (15–45%) percentage of the system power . Thus, the circuit power can be greatly reduced by reducing the clock power dissipation.

Most efforts for clock power reduction have focused on issues such as reduced voltage swings, buffer insertion, and clock routing . In many cases, switching of the clock causes a great deal of unnecessary gate activity. For that reason, circuits are being developed with controllable clocks. This means that from the master clock other clocks are derived which, based on certain conditions, can be slowed down or stopped completely with respect to the master clock. Obviously, this scheme results in power savings due to the following factors.

i. The load on the master clock is reduced and the number of required buffers in the clock tree is decreased. Therefore, the power dissipation of clock tree can be reduced.
ii. The flip flop receiving the derived clock is not triggered in idle cycles and the corresponding dynamic power dissipation is thus saved.
iii. The excitation function of the flip flop triggered by the derived clock may be simplified since it has a do not care condition in the cycle when the flip flop is not triggered by the derived clock.

1.1.Clock Gating

Clock gating is a well known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By ANDing the clock with a gate control signal, clock gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree.

Clock gating logic can be added into a design in a variety of ways:

i. Coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating).

ii. Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers.

II. Clock Gating Techniques

2.1.Synthesis Based

Synthesis based clock gating is the most widely used method by EDA tools. The utilization of the clock pulses, measured by data to clock toggling ratio, left after the employment of synthesis based gating may still be very low. Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying FFs depend on the data being processed. It is important to note that the entire dynamic power consumed by a system stems from the periods where modules' clock signals are enabled.

2.1.1.Drawback of Synthesis Based Method

The switching of a significant portion of the system's clock load is redundant, but consumes most of its power. This calls for other than synthesis based methods to stop the 97% redundant clock pulses. A very low data to clock toggling ratio was also reported in , where extensive power simulations of a wide variety of industrial designs showed average toggling ratios of 0.02 to 0.05. To address the above redundancy, a method called data driven clock gating was proposed for flip flops .

2.2 Data Driven Clock Gating

The data driven gating proposed is illustrated in Figure.1. A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate .Such data driven gating is used for a digital filter in an ultra low power design . A single ICG is amortized over k FFs. There is a clear tradeoff between the number of saved (disabled) clock pulses and the hardware overhead. With an increase in k, the hardware overhead decreases but so does the probability of disabling, obtained by ORing the k enable signals. Let the average toggling probability of a FF (also called activity factor) be denoted by p ($0 < p < 1$). Under the worst case assumption of independent FF toggling, and assuming a uniform physical clock tree structure, and the number k of jointly gated FFs for which the power savings are maximized is the solution of

$$(1 - P)^k \ln(1 - P)(c_{FF} + c_W) + c_{latch}/k^2 = 0 \quad (2.1)$$

where c_{FF} is the FF's clock input capacitance, c_W is the unit size wire capacitance, and c_{latch} is the latch capacitance including the wire capacitance of its clk input.
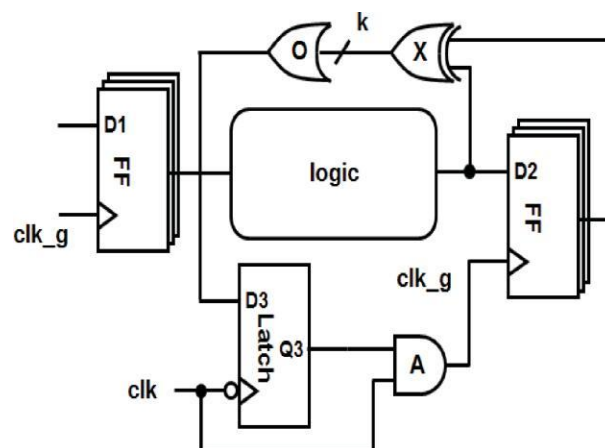

Figure 1: Practical data-driven clock gating

2.2.1 Drawback of Data Driven Method
      Data driven gating suffers from a very short time window where the gating circuitry can properly work.. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF. Such constraints may exclude 5%-10% of the FFs from being gated due to their presence on timing critical paths.The exclusion percentage increases with the increase of critical paths, a situation occurring by downsizing or turning transistors of non critical path to high threshold voltage (HVT) for further power savings.
      Another difficulty of data driven gating is its design methodology. To maximize the power savings, the FFs should be grouped such that their toggling is highly correlated. This requires running extensive simulations characterizing the typical applications expected by the end user. Those applications are in many cases unknown and the amount of redundant clock pulses may significantly increase for specific applications. Further more, IP providers who are delivering RTL code need to cast the gating circuitry per customer, which requires maintaining different versions of the same IP.

2.3 Autogated Flip flops
      The basic circuit used for LACG technique is Auto Gated Flip flop illustrated in Figure.2.The FF's master latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed. A significant power reduction was reported for register based small circuits, such as counters, where the input of each FF depends on the output of its predecessor in the register. AGFF can also be used for general logic.
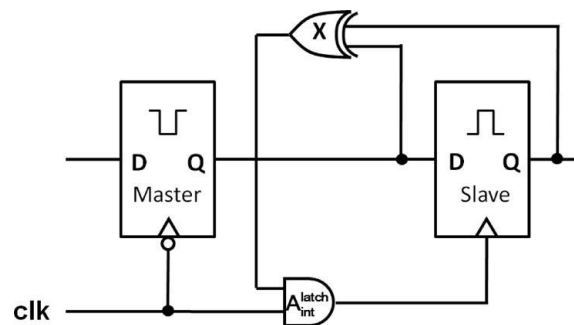

Figure 2: An autogated flip flop

2.3.1 Drawback of Autogated Flip flops
      There are two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

2.4. Look Ahead Clock Gating(LACG)
      Look Ahead Clock Gating computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. Similarly to data-driven gating, it is capable of stop-ping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gaters. Further more, unlike data driven gating whose optimization requires the knowledge of FF's data toggling vectors, LACG is independent of those. The embedding of LACG logic in the RTL functional code is uniquely defined and easily derived from the underlying logic, independently of the target application. This simplification is advantageous as it significantly simplifies the gating implementation.
      The basic circuit used for LACG is Auto Gated Flip Flop illustrated in Figure.2.LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in Figure 2 to generate clock enabling signals of other FFs in the system, whose data depend on that FF. There is a problem though. The XOR output is valid only during a narrow window of (t_{setup} , t_{ccq}) around the clock rising edge, where t_{setup} and t_{ccq} are the FF's setup time and clock to output contamination delay, respectively. After a t_{ccq} delay the XOR output is corrupted and turns eventually to zero. To be valid during the entire positive half cycle it must be latched as shown in Figure. 3(a). Figure. 3(b) is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input clk_g.Such gating involves another XOR and OR gates, useful for high clock switching probability. It is subsequently shown that clk_g probability is very low and it is therefore not further being gated.
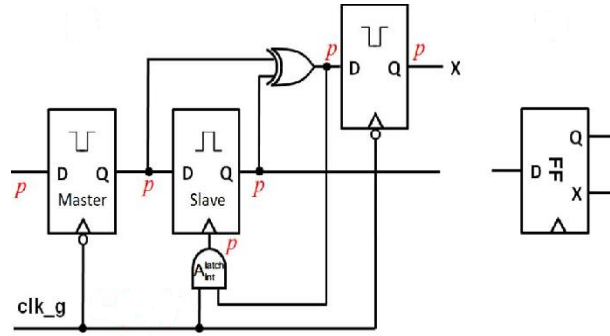
Figure 3: Enhanced AGFF with XOR output used for LACG.

Figure 4 illustrates how LACG works. We call FF$''$ target and FF$'$ source. A target FF depends on K > 1 source FFs. It is required that the logic driving a target FF does not have an input externally of the block. Let X(D$''$) denote the set of the XOR outputs of the source FFs, and denote by Q(D$''$) the set of their corresponding outputs.
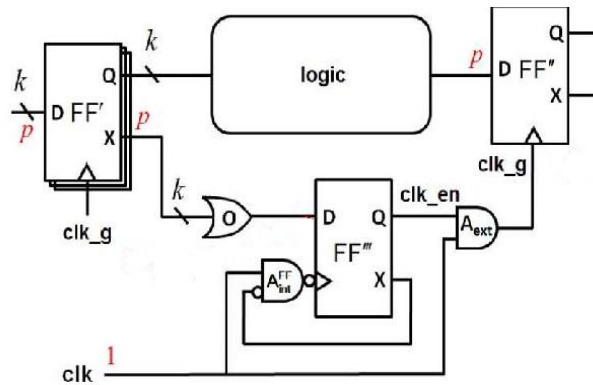

Figure 4: LACG of general logic

The source FFs can be found by a traversal of the logic paths from D$''$ back to Q(D$''$), which can be performed either in the RTL or the net-list descriptions of the underlying system. The logic tree with root D$''$ and leaves Q(D$''$) is sometimes called the logic cone of D$''$.

Let 't' and 't+1' be two successive clock cycles shown in Figure.4.3,where the time tics refer to the rising edge of the clock pulses. We use the notation t-0.5 and t+0.5 to denote the clock's preceding and succeeding falling edges, respectively. Clearly $\sum_{X(D'')} X(t)=0$,is a sufficient condition for FF$''$ not to change state at 't+1' , where the summation means logical OR operation. FF's clock pulse could therefore be disabled at 't+1' to save the switching power.

To generate the enabling signal obtained from data at 't' and ensure its validity at 't+1', an oppositely clocked FF is introduced as shown in Figure. 4. Upon the clock's falling edge at t + 0.5 there exists D$''$(t+0.5)=$\sum_{X(D'')}$X(t). Since FF$'''$ is oppositely clocked, there exists Q$'''$(t+0.5)=D$'''$(t+0.5)=$\sum_{X(D'')}$X(t). The signal Q$'''$ is stable during the time period [t+0.5 ,t+1] obtaining Q$'''$(t+1)= $\sum_{X(D'')}$X(t).The gater A$_{ext}$ can then appropriately gate the clock's rising edge at 't+1' which drives FF$''$.Using a FF for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating FF$'''$ as shown in Figure. 4

2.4.1.Advantage of LACG

Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gaters.

Furthermore, unlike data driven gating whose optimization requires the knowledge of FFs' data toggling vectors, LACG is independent of those. The embedding of LACG logic in the RTL functional code is

uniquely defined and easily derived from the underlying logic, independently of the target application. This simplification is advantageous as it significantly simplifies the gating implementation

III.   Simulation Results
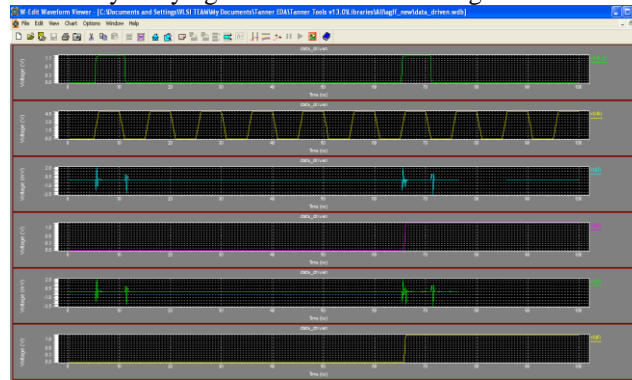The following results are obtained by carrying out the simulation using the EDA tool Tanner.
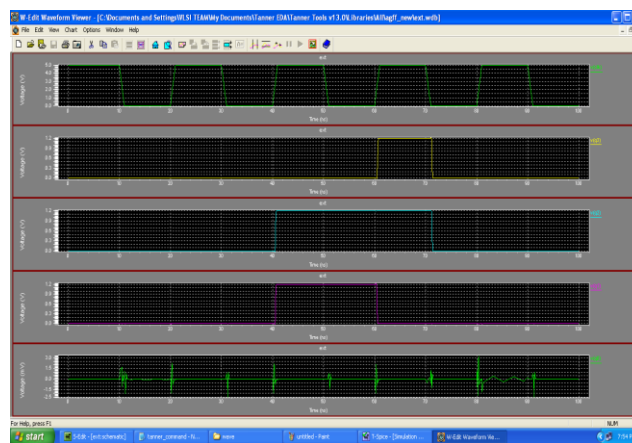

Figure 5: Output Waveform of Data Driven Clock Gating
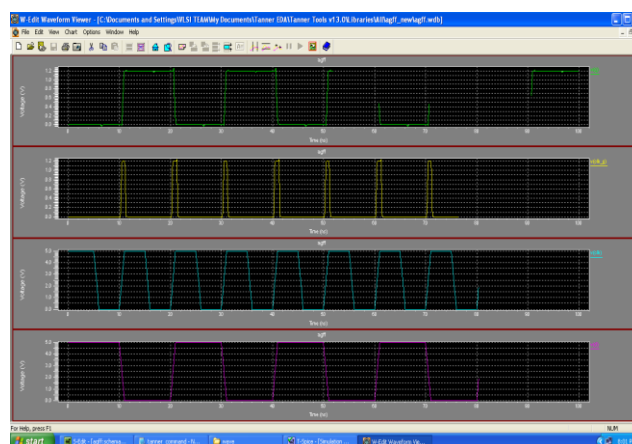

Figure 6 : Output Waveform with out clock gating logic
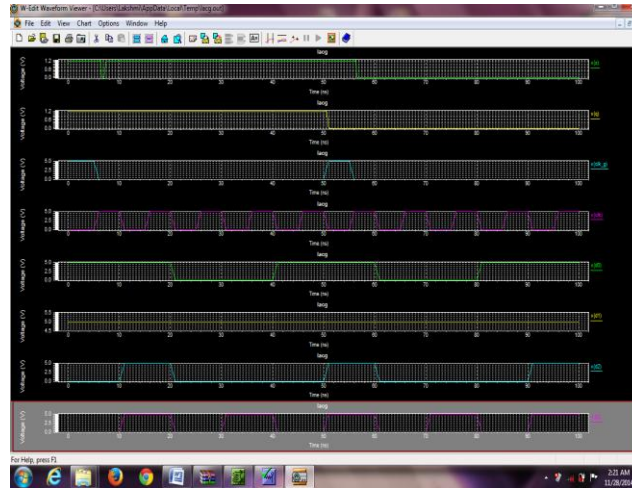

Figure 7 : Output Waveform of Autogated Flip flops

Figure 8: Output Waveform of Look Ahead Clock Gating

S.NO	CLOCK GATING TECHNIQUE	AVERAGE POWER CONSUMED (watts)
1	With out clock gating	5.3327e-008
2	Data driven method	4.1776e-008
3	Autogated flip flops	2.4605e-008
4	Look ahead clock gating	1.7539e-008

Table 1: Comparison of power dissipation in clock gating techniques

Hence from the above table it is observed that the Look Ahead Clock Gating dissipates less power compared to other techniques.

IV.   Conclusion

The Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gaters. Furthermore, unlike data driven gating whose optimization requires the knowledge of FF's data toggling vectors, LACG is independent of those and also it is independent of the target application. The power in LACG has been reduced to 50% than the autogated FF which consumes 50% less power than the data driven method.

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