

A Novel Low Power Energy Efficient SRAM Cell With Reduced Power Consumption using MTCMOS Technique

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Abstract: In modern high performance integrated circuits, maximum of the total active mode energy is consumed due to leakage current. SRAM cell array is main source of leakage current since majority of transistor are utilized for on-chip memory in today high performance microprocessor and system on chip designs. Therefore the design of low leakage SRAM is required. Reducing power dissipation, supply voltage, leakage currents, area of chip are the most important parameters in today's VLSI designs. But scaling of these parameters will lead to drastic increase in sub threshold leakage currents and power dissipation because of that performance of the design is degraded. So to overcome these issues it is better to concentrate on reduction of active leakage currents and dynamic power dissipation by using power reduction techniques. In this paper 9T SRAM (data retention p-gated) cell for low voltage and energy constrain application is analyzed with respect to power dissipation, area and delay. The analyzed design of 9T SRAM cell with MTCMOS technique has been proposed. Designed circuits are simulated in Microwind 3.1 VLSI CAD Tool in 90 and 65nm CMOS technology.

Keywords: CMOS, 6T SRAM cell, 8T SRAM cell, 9T SRAM cell, MTCMOS, Low Power Consumption.

I. Introduction

Development of digital Integrated Circuits is challenged by high power consumption and greater threshold leakages. Higher clock speed combination with greater integration functionality and smaller process geometries contributed to significant growth in power density. Scaling improves functionality and density of transistors on a chip. Scaling helps to increase operation speed and performance of IC designs. As voltages scale down with geometries, V_{th} - threshold voltages must also decrease to gain the performance advantages of new technology, but leakage current increases exponentially.

Low power and high-stability have been the main issues of SRAM designs as the demand of the portable electronic market constantly urges for less power-hungry architectures [1]. Many techniques have been introduced to fulfill this requirement such as scaling the supply voltage, using Multi threshold CMOS process to minimize the leakage, dividing the SRAM macro into multiple sub-macros to enhance its stability and to reduce dynamic power. The second challenge in designing a robust SRAM is to ensure a reasonable noise margin, which is normally measured by the Static Noise Margin (SNM).[2]. According to, these design factors degrade when threshold voltage variation increases and are also linearly dependent on the reduction of the supply voltage. As a result, it is extremely difficult to maintain the cell stability as technology enters less than 100 nm regime. Several more-than-6T SRAM cell designs are given in [3], to improve the stability and power dissipation. In these papers separate Read and Write ports are employed and hence the cell's SNM can be optimized.

Sub threshold leakage current is much larger than the other leakage current and is calculated by using the following equation.

$$I_{DS} = K (1 - e^{-V_{DS}/V_T}) e^{(V_{GS} - V_T + \alpha V_{DS})/\alpha V_T}$$

Technique used for minimization of static and dynamic power dissipations in SRAM cell during write/read operation is MTCMOS. MTCMOS technology provides low leakage and high performance operation by utilizing high speed, low threshold voltage (V_{thL}) transistors during active mode and low leakage, high threshold voltage (V_{thH}) transistors during sleep mode. This technology, also called as power gating, the wake up latency and power plane integrity are key issues. Several researchers have proposed methods for optimal sizing of sleep transistors in a given circuit to meet a performance constraint.

In this paper a novel 9T MTCMOS SRAM cell is proposed.[8]. A charge recycling technique is used to minimize the leakage currents and static energy dissipation during the mode transitions. The total power dissipations at different temperatures and supply voltages for assessing stability at different pullup ratios have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

This paper mainly focuses on reduction of power consumption at higher performance with MTCMOS technique. Section-II describes the design of conventional 1-bit SRAM cells (existing cells)[9]. Section-III describes the design of Proposed MTCMOS SRAM cell. Section-IV presents the simulation results of proposed SRAM cell. Section-V concludes this paper.

II. Conventional SRAM

A. Conventional 6T SRAM cell:

Fig. 1 shows the circuit diagram of a conventional SRAM cell. Word line (WL) is used for enabling the access transistors T2 and T5 for write operations [3]. Bit lines BL and BL bar are used to store the data and its compliment. For writing operation, one bit line is high and the other bit line is low. For writing “0”, BL is low and BL bar is high. When the word line (WL) is asserted high, transistors T2 and T5 are ON and any charge stored in the BL goes through T2-T3 path to ground. Due to zero value on Q bar, the transistor T4 is ON and T6 is OFF. So the charge is stored at Q bar line. Similarly in the write “1” operation, BL is high and BL bar is low, due to this T6 is ON and the charge stored on Q bar is discharged through the T5-T6 path and due to this low value on the Q bar , T1 is ON and T3 is OFF, so the charge is stored on the Q.

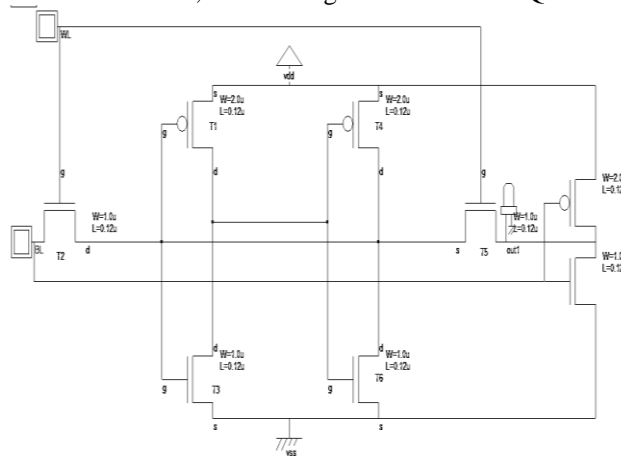


Fig 1. Conventional 6T SRAM Cell.

Before the read operation of “1” at Q (for example) begins, BL and BL bar are pre-charged to as high as V_{dd} . When the WL is selected, the access transistors T2 and T5 are turned ON. Because of the pull-up transistor T1 ON and pull down transistor T3 OFF, voltage of BL will be nearly V_{dd} . On the other side, current will flow from the pre-charged BL bar to ground, thus discharging BL bar line through T5-T6 path to ground; T4 being OFF. Thus, a differential voltage develops between BL and BL bar lines. This small potential difference between the bit lines is sensed and amplified by the sense amplifier at the data output

B. Conventional 8T SRAM cell:

8T SRAM cell [4] is shown in Figure 2. This cell uses the same 6T SRAM structure for the writing operation. For reading, it uses a separate bit line, RBL with RWL as its control signal. During writing, the PMOS and NMOS transistors of the inverters can be maintained at the minimum width as the read operation is separated. The RBL is read according to the value stored at the storage nodes when RWL is high.

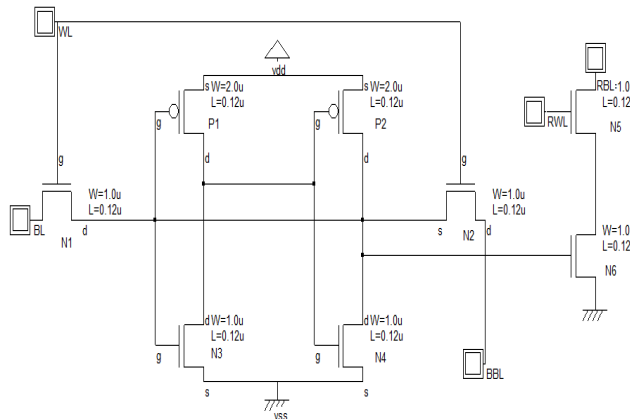


Fig2. Conventional 8T SRAM Cell.

C. Conventional 9T SRAM cell:

The 9T SRAM [8] is shown in Fig. 3. “Write” occurs just as in the 6T SRAM cell. “Read” occurs separately through N5, N6 and N7 controlled by the Read Signal RD going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line and it can be minimized by placing sleep transistors on bit line which was explained in section- III.

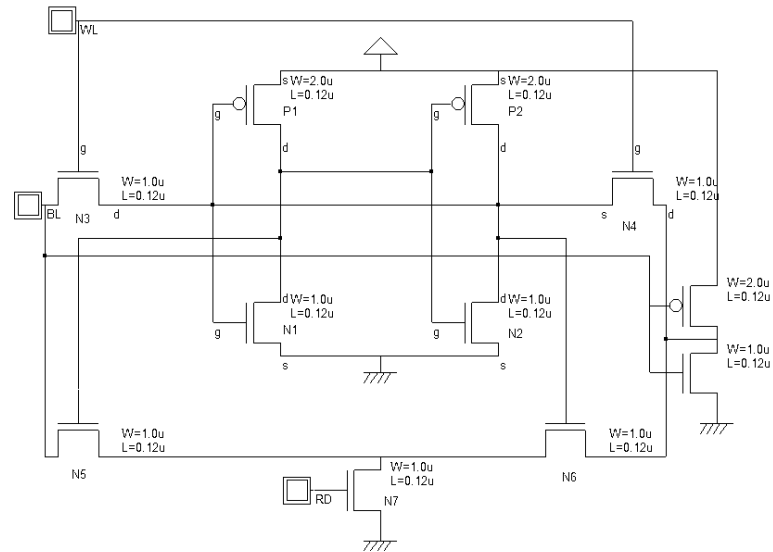


Fig 3. Conventional 9T SRAM Cell.

III. Proposed MTCMOS SRAM Cell

Low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. This technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit. Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. The low-threshold (V_{tl}) transistors which have high performance are used to reduce the propagation delay in the critical path. High-threshold (V_{th}) transistors which have less power consumption are used to reduce the power consumption in the shortest path.

The multi threshold CMOS technology has two main parts. First, “active” and “sleep” operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. These apply on between the low threshold voltage (low-Vt) gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as “power gating”. Schematic of power gating technique is shown in below Fig. 4. And transistor level circuit is shown in Fig. 5 [8].

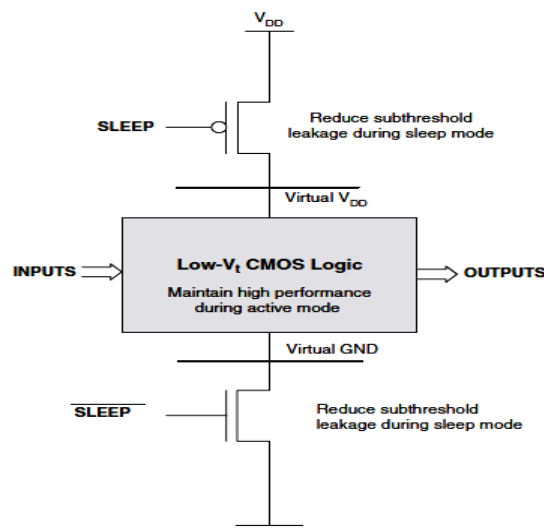


Fig 4. MTCMOS Technique.

Operation of 9T MTCMOS SRAM cell is same as conventional 9T SRAM cell as mentioned in section II – C, there it is having large power dissipation because of high bit line capacitance due to more switching transitions at bit line node and it can be reduced by placing high threshold transistors (pmos & nmos) between supply and ground, so that the unwanted and more transitions can be decreased by controlling switching transistors (V_{th}) which are placed between power supply and ground.[5],[6].

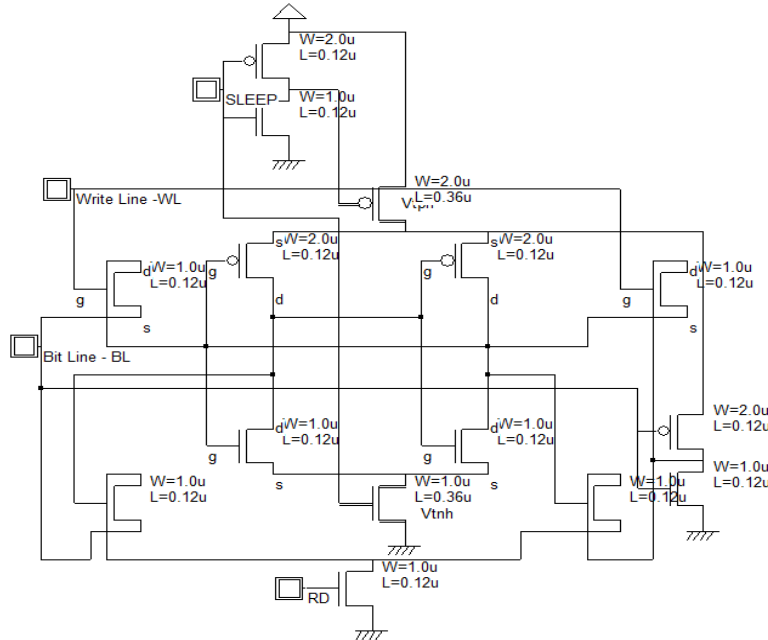


Fig.5 Proposed MTCMOS SRAM Cell.

IV. Simulation Results

In this section, the total write power dissipations at different voltage levels and static noise margins (SNM) are calculated and the simulation results are compared to those of other SRAM cells. Analog and schematic simulations have been done in 65nm environment with the help of Microwind 3.1 by using BSIMM4 model.[10].

A. Power Dissipation Analysis:

Table I shows the comparison of total power dissipations (static power dissipation plus dynamic power dissipation together) of existing SRAM cells and the proposed SRAM cell for write operations in 90nm and Table II shows results in 65nm. The proposed cell dissipates lesser power than the other existing SRAM cells even at higher temperatures.

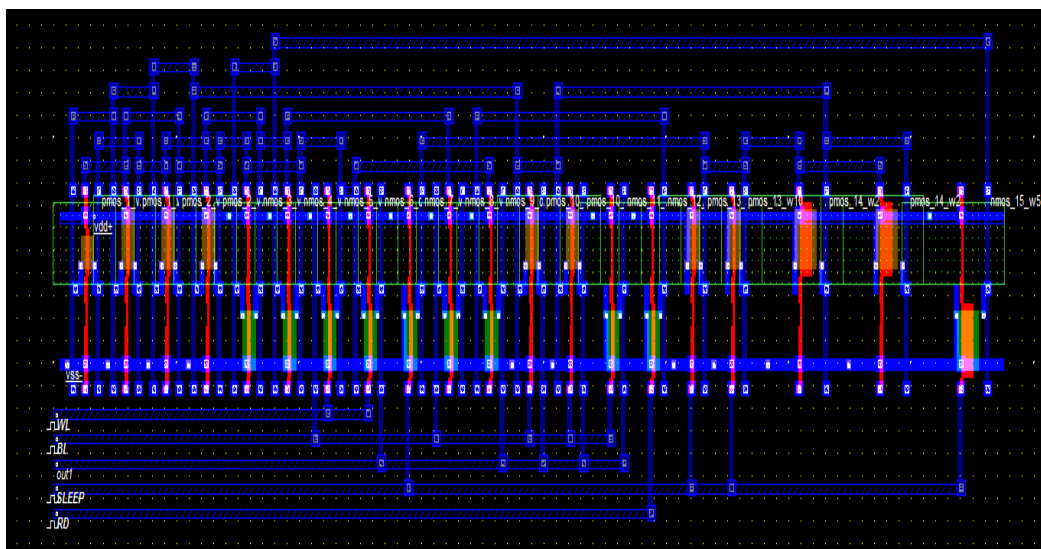


Fig.6 Layout of Proposed MTCMOS SRAM Cell.

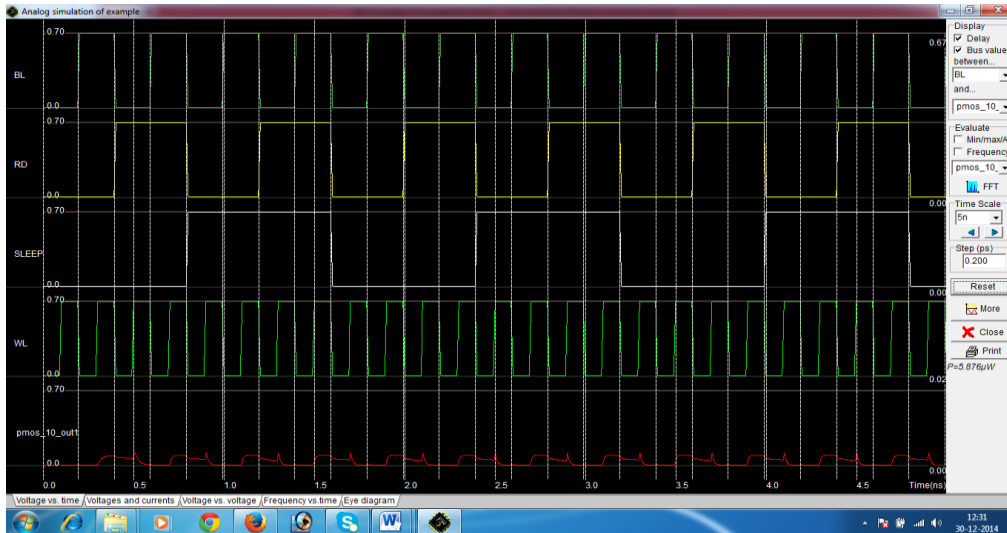


Fig7. Waveform of Proposed 9T MTCMOS SRAM Cell (V vs T).

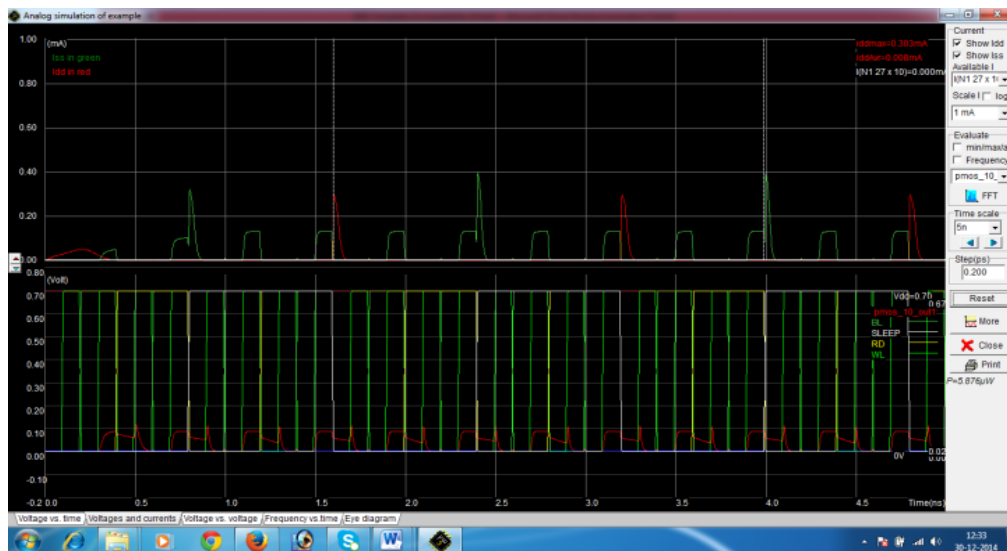


Fig.8 Waveform Of Proposed 9T MTCMOS SRAM Cell (V Vs I).

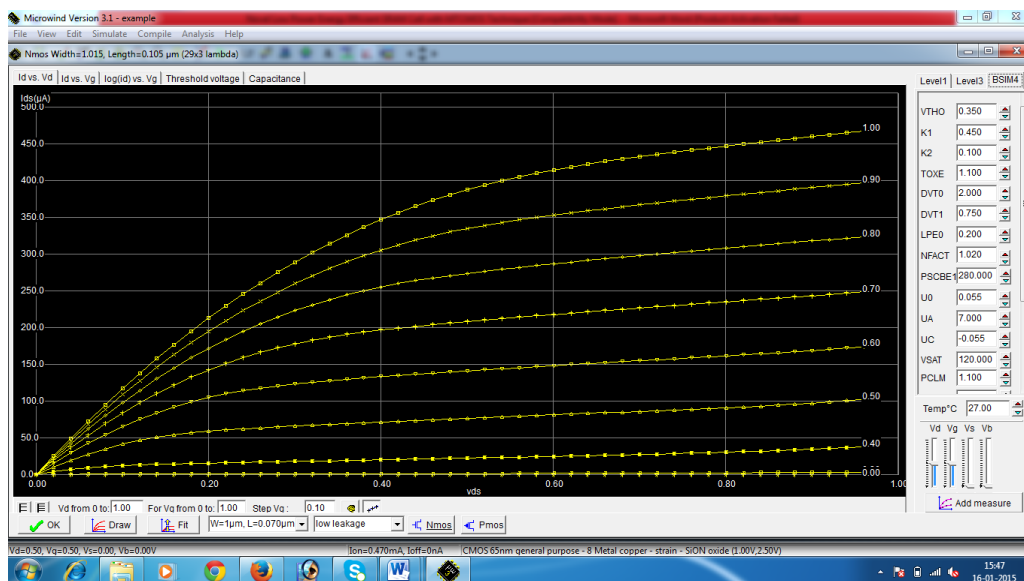


Fig9. I_d/V_d Characteristics Of Nmos Devices In Low Leakage Mode At Room Temperature.

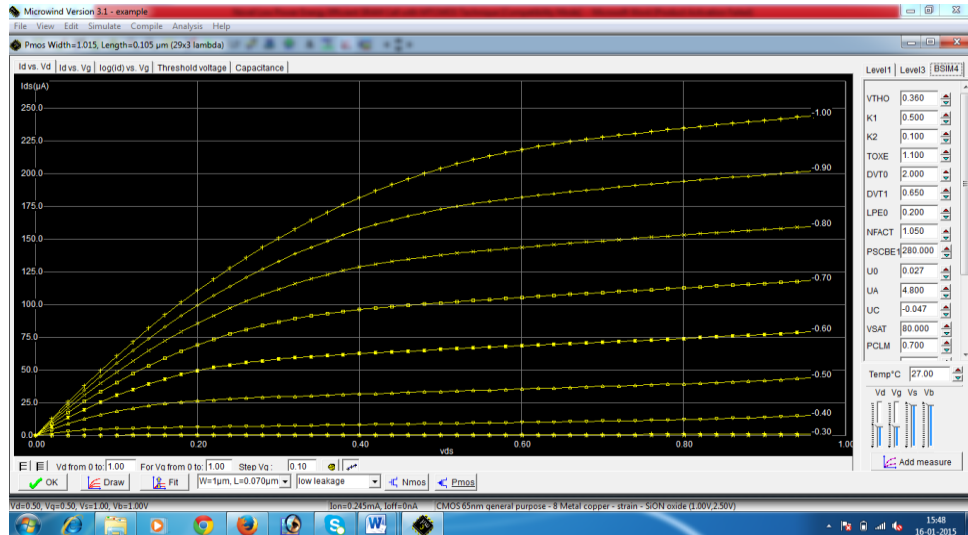


Fig10. I_d/V_d Characteristics Of Pmos Devices In Low Leakage Mode At Room Temperature.

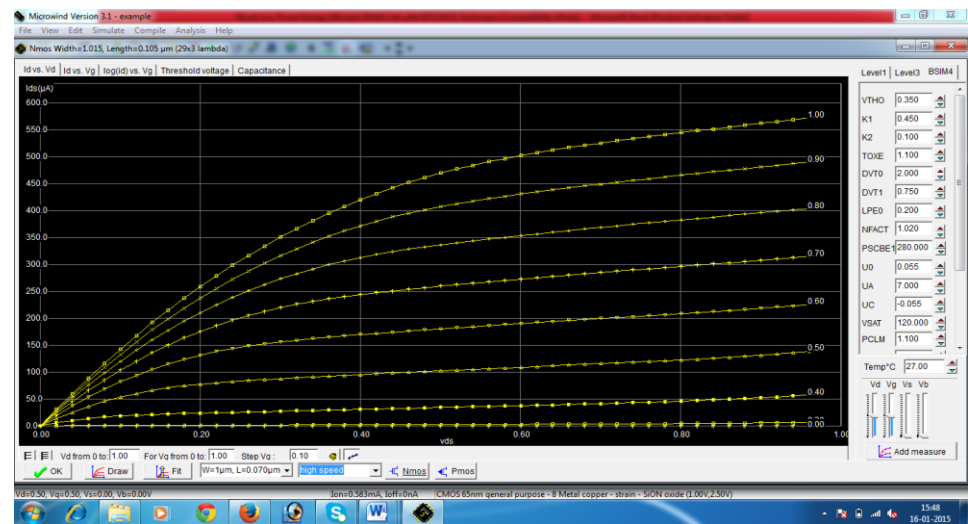


Fig11. I_d/V_d Characteristics Of Nmos Devices In High Speed Mode At Room Temperature.

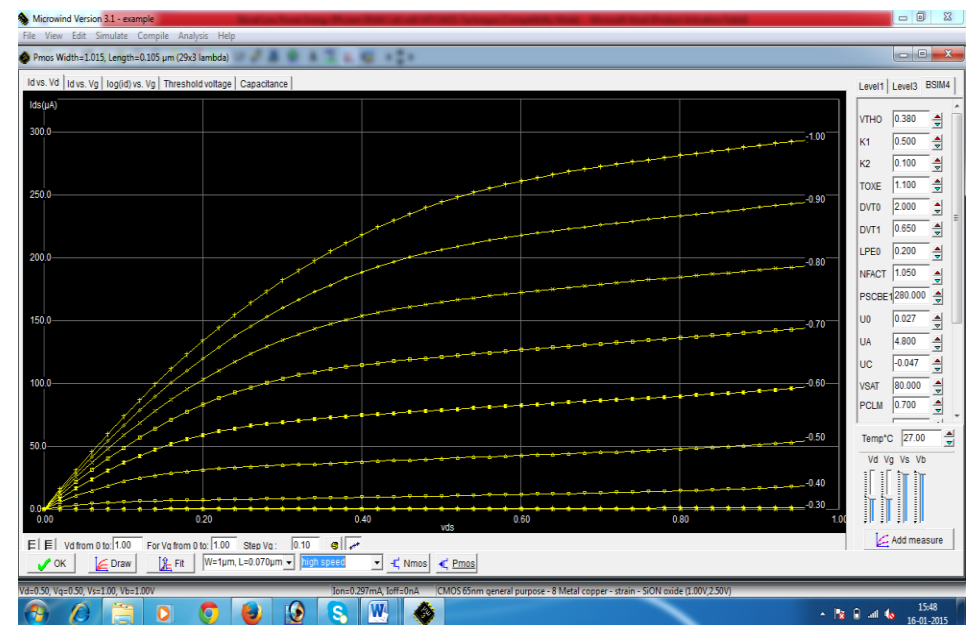


Fig12. I_d/V_d Characteristics Of Pmos Devices In High Speed Mode At Room Temperature.

Table I. Simulation Results of Different Types of SRAM Cells in 90NM/27°C

TECHNIQUES	AREA (μm ²)	POWER in (μw)	DELAY in (ps)	PDP VALUE (μw X ns)
Conventional 6T SRAM CELL	180	254	300	76.20
Conventional 8T SRAM CELL	210	256	340	87.04
Conventional 9T SRAM CELL	220	263	330	86.79
Proposed MTCMOS SRAM CELL	360	88.22	475	41.90

Table II. Simulation Results of Different Types of SRAM Cells in 65NM/27°C

TECHNIQUES	AREA (μm ²)	POWER in (μw)	DELAY in (ps)	PDP VALUE (μw X ns)
Conventional 6T SRAM CELL	112	41.47	228	9.455
Conventional 8T SRAM CELL	128	41.58	262	10.89
Conventional 9T SRAM CELL	136	42.88	240	10.29
Proposed MTCMOS SRAM CELL	252	5.876	370	2.174

Table III. Transistors Required For Implementing SRAM Cell

No.of MOS Transistors	Pmos	Nmos	Total
Conventional 6T SRAM CELL	3	5	8
Conventional 8T SRAM CELL	3	7	10
Conventional 9T SRAM CELL	3	8	11
9T MTCMOS SRAM CELL	5	10	15

Table IV. Power Consumption of 9T MTCMOS SRAM Cell at Various Voltage Levels in 65nm at 27°C

9T MTCMOS SRAM CELL	POWER in (μw)
0.7 V	5.876
1.2 V	218.0
1.8 V	749.0
2.5 V	1584.0
3.3 V	2635.0
5.0 V	5199.0

B. Noise Analysis:

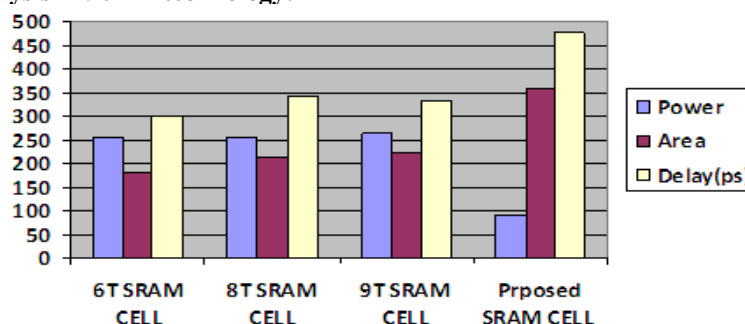
Here Output of 9T MTCMOS SRAM cell is analysed by adding noise at input. Table.V gives the analysis report between power consumption and noise at various noise levels in 65 nm technology.

Table V. Noise vs Power consumption analysis of 9T MTCMOS SRAM cell in 65nm technology

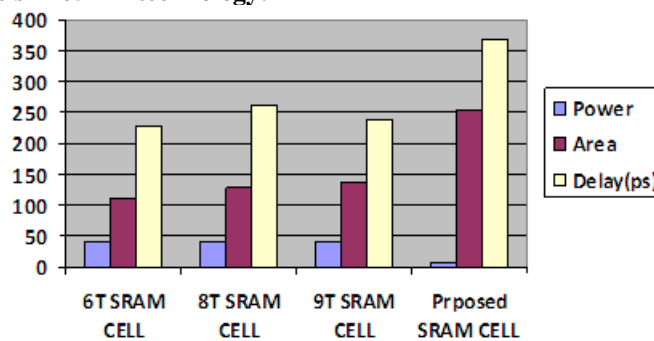
Noise Level in (mv)	POWER in (μw) at VDD=0.7v
10	5.876
20	5.878
30	5.888
40	5.921
50	6.031
60	6.253
70	6.707
80	7.341
90	8.222
100	9.377

From the above table V it is observed that after 50mv of noise input, output starts affecting with noise. Hence the noise margin for the proposed SRAM cell is 50mv.

C. Graphical Analysis in 90 nm technology:



D. Graphical Analysis in 65 nm technology:



V. Conclusion

In this paper, reduction in power consumption which leads to reduction in leakage current and power dissipation as well as Power Delay product is analyzed for conventional and modified 1-bit SRAM cell using Microwind / Dsch tool in 90nm and 65nm technologies. It is found that total power consumption of proposed design with MTCMOS is reduced when compared to other SRAM cells. Hence the proposed SRAM cell with MTCMOS is Energy Efficient as it's PDP value is less when compared to other conventional designs. Future work is carrying out in designing 32Kb RAM with the proposed model.

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